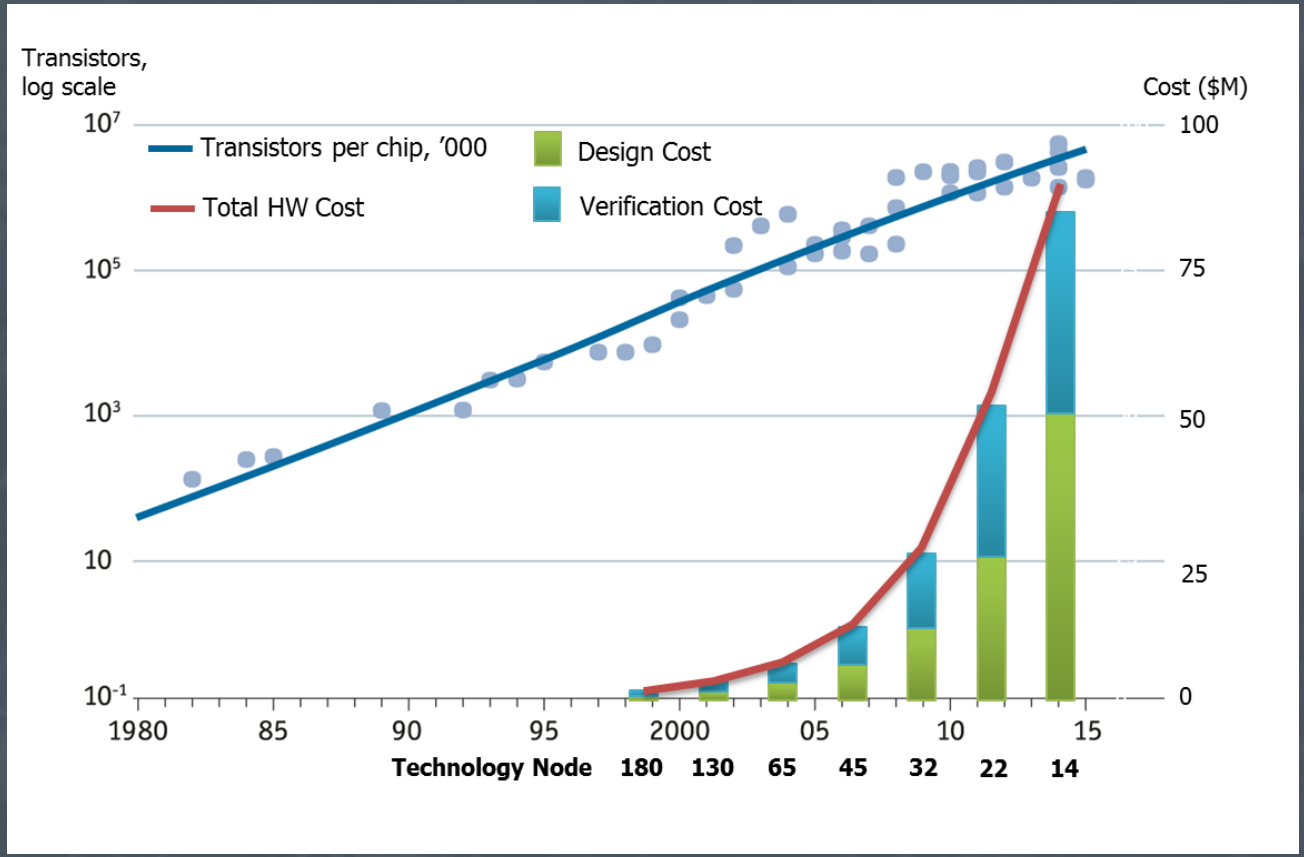
# JAY LEWIS

**DEPUTY DIRECTOR**
DARPA/MTO

THE ELECTRONICS RESURGENCE INITIATIVE

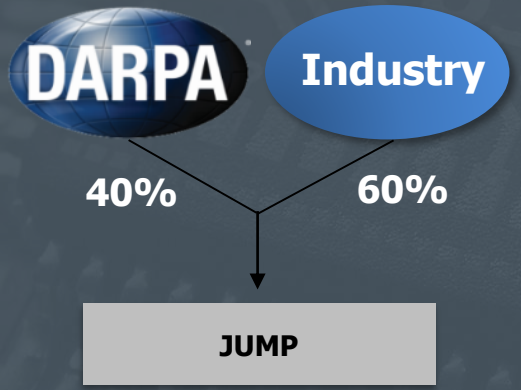
# ERI Kickoff and Page 3 Team Announcement

Dr. Jay Lewis



# Joint University Microelectronics Program (JUMP)

High-risk, high-payoff research that addresses existing and emerging challenges in microelectronic technologies

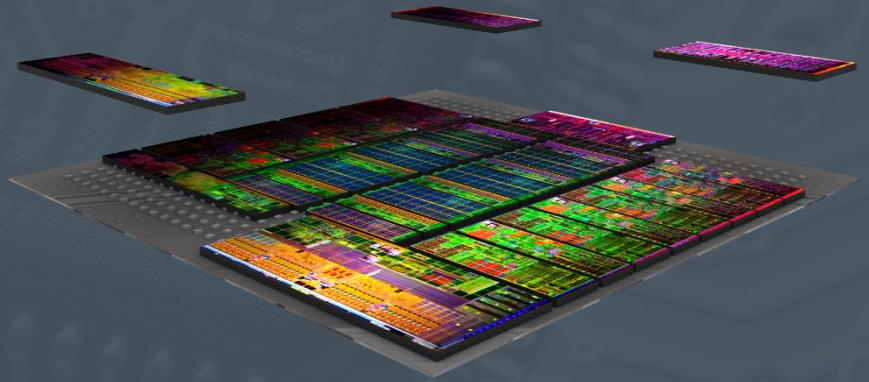



- 6 University Centers
- ~$200M over 5 years
- >500 graduate students

| | | | | |
|---|---|---|---|---|
| **Lockheed Martin** | **Micron** | **Intel** | **Analog Devices** | **IBM** |
| **Raytheon** | **TSMC** | **Northrop Grumman** | **ARM** | **Samsung** |
| **EMD Performance Materials** | | | | |

# Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)

Modular electronic systems that can leverage the best of DoD and commercial designs and technology



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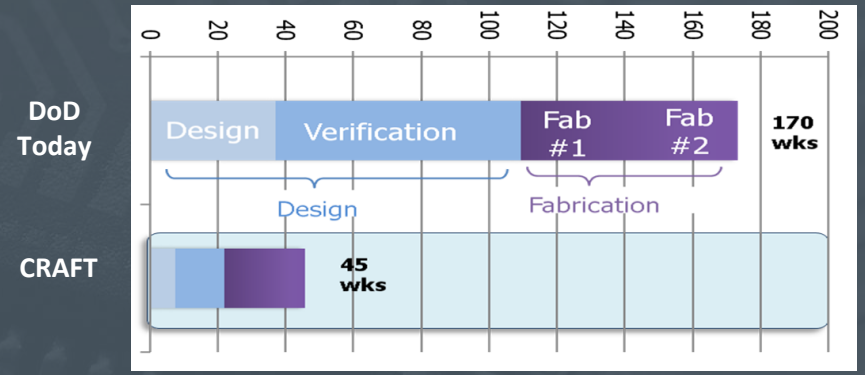
|---|---|---|---|---|
| **Georgia Tech** | **Cadence** | **Micross** | **Intel** | **Lockheed Martin** |
| **NC State** | **Synopsys** | **Intrinsix** | **General Electric** | **Boeing** |
| **University of Michigan** | **NIST** | **Jariet Technologies** | **Raytheon** | **Northrop Grumman** |
| **Ferric Semiconductor** | | | **On Semiconductor** | |

# Circuit Realization at Faster Timescales (CRAFT)

Dramatic reduction in circuit-design time, and ease of porting between technologies



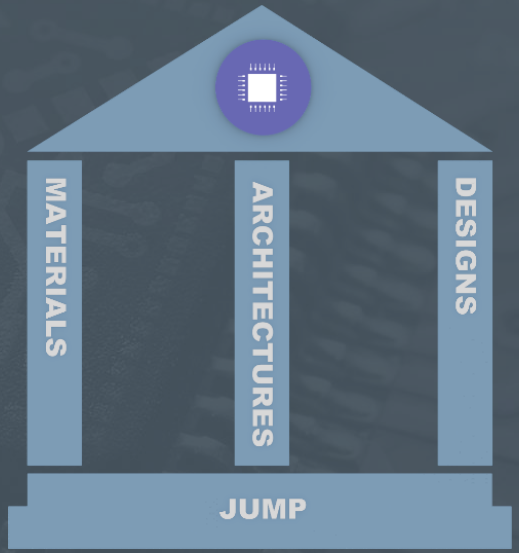

Chip Design and Fabrication Time (weeks)

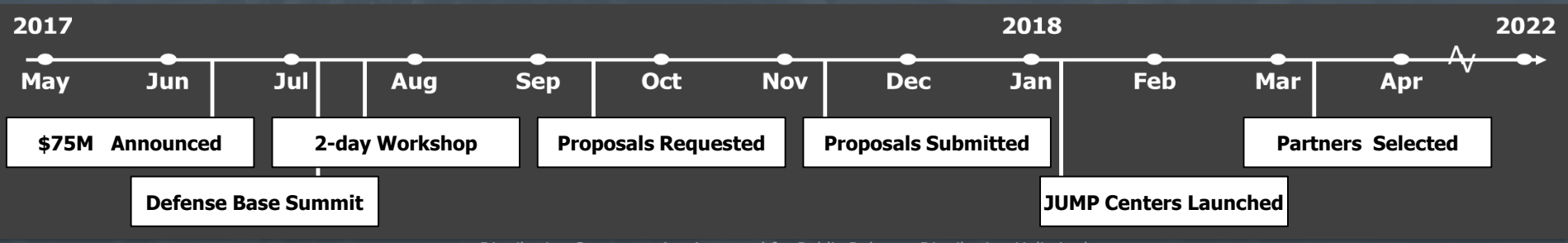
**NVIDIA** **Cadence** **Northrop Grumman** **Army Research Lab** **Boeing**

**Harvard University** **University of California - Berkeley**

**Carnegie Mellon University** **University of Southern California**

# 2025 – 2030
# National Electronics Capability



# Three Dimensional System on Chip (3DSoC)

Technical Area 1: A 3D monolithic manufacturing process that will be utilized to build DoD and commercial SOCs

Technical Area 2: EDA design tools that optimize 3-dimensional circuits

# Three Dimensional System on Chip (3DSoC)

Technical Area 1: A 3D monolithic manufacturing process that will be utilized to build DoD and commercial SOCs
Technical Area 2: EDA design tools that optimize 3-dimensional circuits

**TA1** **MIT**

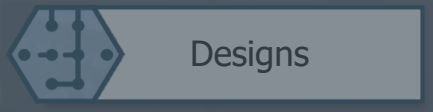
*Refined RRAM and CNFET processes for commercial fabrication of an integrated, monolithic 3D SoC*

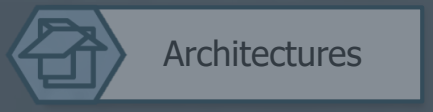
**Dr. Max Shulaker**

Revolutionizing Computing Systems through Dense and Fine Grained Monolithic 3D Integration

$61M

Partners: Skywater, Stanford University, Raymor


# Three Dimensional System on Chip (3DSoC)

Technical Area 1: A 3D monolithic manufacturing process that will be utilized to build DoD and commercial SOCs

Technical Area 2: EDA design tools that optimize 3-dimensional circuits

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**TA2**

**Georgia Tech**

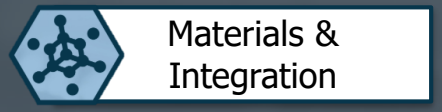
*Optimized EDA software for complex, high-performance monolithic 3D SoCs*

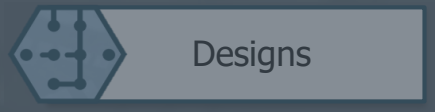
**Dr. Sung Kyu Lim**

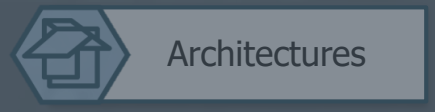
RTL-to-GDS Tools and Methodologies for Sequential Integration of Monolithic 3D ICs

$3.1M

Partner: Duke University



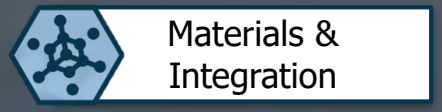



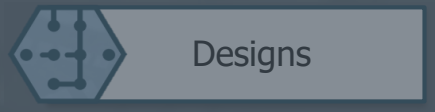



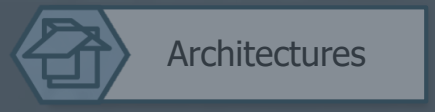

# Foundations Required for Novel Compute (FRANC)

Technical Area 1: New material and component technologies that enable novel compute topologies

Technical Area 2: Circuits prototypes and architectures that leverage unique components and functions

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**TA1**

**Applied Materials**

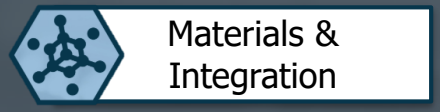
*New correlated electronic multi-level memory devices with robust Mott transition*

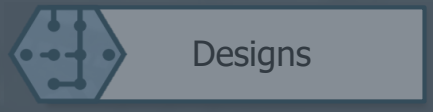
**Dr. David Thompson**

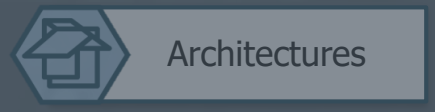
Synapses and Neurons using Correlated Electron Devices

$6.7M

Partners: ARM, Symetrix, University of Colorado, University of British Columbia

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Technical Area 1: New material and component technologies that enable novel compute topologies
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**TA1** **Univ. of Minnesota**

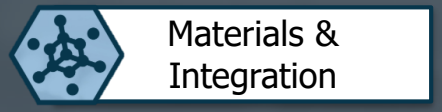
*High-density magnetic memory devices with synthetic antiferromagnetic free layers for fast switching speed with low voltage and energy*

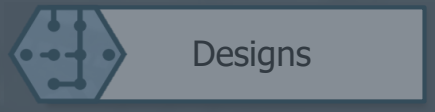
**Dr. Jian-Ping Wang**

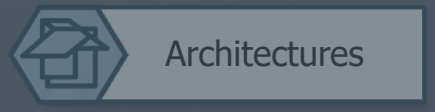
Advanced MTJs for computation in and near random access memory

$0.8M

Partners: University of Arizona, NIST

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Technical Area 1: New material and component technologies that enable novel compute topologies

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**TA2**

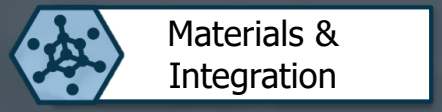
**HRL Laboratories**

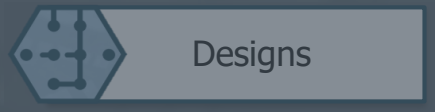
*New active and passive memristor devices for neuromorphic functions and computation*

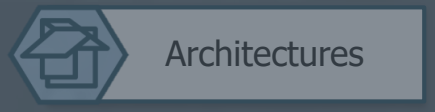
**Dr. Wei Yi**

Scalable, Energy-Efficient, And High-Throughput All-Memristor Neuromorphic Processor

$3.4M

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Technical Area 1: New material and component technologies that enable novel compute topologies
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**TA2**

**Univ. of Illinois - UC**

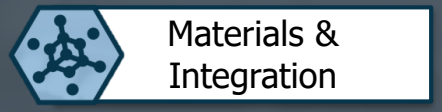
*Energy-efficient in-memory computing with non-volatile memory*

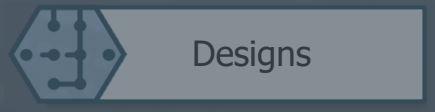
**Dr. Naresh Shanbhag**

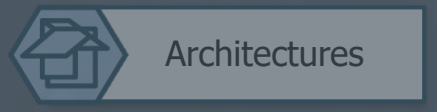
MRAM-based Deep In-memory Architectures

$8.3M

Partners: Princeton University, GlobalFoundries, Raytheon




# Foundations Required for Novel Compute (FRANC)

Technical Area 1: New material and component technologies that enable novel compute topologies

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---

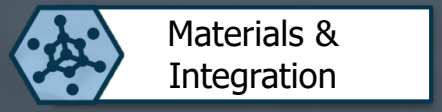
**TA2** | **Univ. of California - LA**

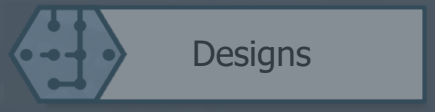
*Energy-efficient spintronics-based stochastic computing system with non-volatile magnetic memory*

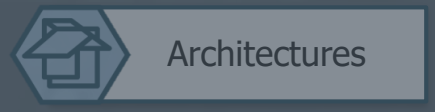
**Dr. Sudhakar Pamarti**

Spintronic Stochastic Dataflow Computing

$1.9M

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Technical Area 1: New material and component technologies that enable novel compute topologies
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**TA2** **Ferric Semiconductor**

*Integrated magnetic devices for efficient power converters*

**Dr. Noah Sturcken**

Integrated Power Management for Novel Compute

$3.1M

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

Technical Area 2: A system generator that is intent-driven and correct by construction

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Technical Area 1: No human in the loop layout of complex mixed signal circuits

Technical Area 2: A system generator that is intent-driven and correct by construction

---

**TA1** **Univ. of Minnesota**

*Open source layout generator for analog circuits through the use of template-drive designs and machine learning*

**Dr. Sachin Sapatnekar**

ALIGN: Analog Layout, Intelligently Generated from Netlists

$5.3M

Partners: Intel, Texas A&M University

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

Technical Area 2: A system generator that is intent-driven and correct by construction

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**TA1**

**Univ. of Illinois - UC**

*Open source massively parallel EDA infrastructure and static timing analysis engine*

**Dr. Martin Wong**

OpenTimer and DtCraft

$1.7M

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

Technical Area 2: A system generator that is intent-driven and correct by construction

**TA1** **Purdue University**

*First principle physics based extraction flow for high PCBs, packages, and System-On-Chips*

**Dr. Dan Jiao**

Rapid Modeling and Analysis Framework for Full-Chip/Package/Board Layout and Parasitic-Driven and Variations-Aware Analog and Digital Circuit Layout Synthesis

$1.3M

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

Technical Area 2: A system generator that is intent-driven and correct by construction

**TA1**

**Univ. of Texas - Austin**

*Machine learning-based software for analog layout constraint generation, placement, and routing that leverages human-expert constraints derived from existing analog layouts*

**Dr. David Pan**

DR2CR: An Intent Driven and Machine Intelligence Based Fully Automated Analog IC Synthesis System from Draft to Craft

$1.7M

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Technical Area 1: No human in the loop layout of complex mixed signal circuits

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**TA1**

**Yale University**

*Develop an open-source EDA flow for asynchronous circuits*

**Dr. Rajit Manohar**

IDEAL: an Intelligent Design Environment for Asynchronous Logic

$1.2M

Partners: University of California-Berkeley, University of Texas-Austin, Sandia National Labs

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

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**TA1**

**Princeton University**

*Develop open source high impact digital circuit, analog circuit, board and package validation test cases and evaluate the IDEA design flow*

**Dr. David Wentzlaff**

ORDER: Open-source Rooted Design Experts with Repute

$2.8M

Partner: University of Washington

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

Technical Area 2: A system generator that is intent-driven and correct by construction

**TA1**

**University of Utah**

*Open source logic synthesis leveraging logic optimization engines and a machine-learning-based logic synthesis technique based on input circuit topology*

**Dr. Pierre-Emmanuel Gaillardon**

A Learning-Based Oracle for Automatic Logic Optimization

$1.0M

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

Technical Area 2: A system generator that is intent-driven and correct by construction

**TA1**

**Univ. of California - SD**

*Open source layout generator for digital circuits, packages, and boards through the use of extreme partitioning, cloud computing, and machine learning*

**Dr. Andrew Kahng**

OpenROAD: Foundations and Realization of Open, Accessible Design

$11.3M

Partners: Qualcomm, ARM, University of Minnesota, Brown University, University of Michigan, University of Illinois-Urbana Champaign, University of Texas-Dallas

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

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**TA1/2** **Cadence**

*A no human in the loop layout generator for analog, package, and board design*

**Dr. David White**

MAGESTIC: Machine Learning-driven Automatic Generation of Electronic Systems through Intelligent Collaboration

$24.1M

Partners: NVIDIA, University of California-Berkeley, University of Texas-Austin, Carnegie Mellon University

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

Technical Area 2: A system generator that is intent-driven and correct by construction

**TA2** **University of Michigan**

*Automated SoC synthesis tool for both analog and digital components from a user intent-based description*

**Dr. David Wentzloff**

Fully-Autonomous SoC Synthesis using Customizable Cell-Based Synthesizable Analog Circuits

$6.4M

Partners: ARM, University of Virginia

# Intelligent Design of Electronic Assets (IDEA)

Technical Area 1: No human in the loop layout of complex mixed signal circuits

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**TA2** **Northrop Grumman**

*An open source system generator, open parts database and circuit optimizer to enable automatic design of boards and packages based on user design intent*

**Mr. Dan D'Orlando**

Generative User-Intent Design of Electronics (GUIDE)

$8.7M

Partner: JITX

# Posh Open Source Hardware (POSH)

Technical Area 1: Automated signoff-quality verification of circuits of unknown origin

Technical Area 2: Establish IP to seed a nascent open source repository

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Technical Area 1: Automated signoff-quality verification of circuits of unknown origin

Technical Area 2: Establish IP to seed a nascent open source repository

**TA1** **Xilinx**

*An open-source approach for fast, mixed-accuracy co-simulation that allows hardware and software to be co-developed, debugged, and verified*

**Mr. Edgar Iglesias**

Xilinx mixed simulation proposal

$1.2M

Partner: GreenSoCs, FEIMTECH AB

# Posh Open Source Hardware (POSH)

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**TA1** **Synopsys**

*An emulation platform for high-performance analog mixed signal functional verification with transistor-level accuracy*

**Mr. Oleg Raikhman**

Mixed-Signal SoC Emulation Technology

$6.1M

Partners: Lockheed Martin, Analog Devices, Analog Circuit Works

# Posh Open Source Hardware (POSH)

Technical Area 1: Automated signoff-quality verification of circuits of unknown origin
Technical Area 2: Establish IP to seed a nascent open source repository

**TA1** **Sandia Nat'l Labs**

*Massively parallel distributed open source simulation tools*

**Dr. Eric Keiter**

AMS Verification Technologies and Flow for enabling POSH SoCs

$6.9M

Partners: Yale University, University of California-Berkeley

# Posh Open Source Hardware (POSH)

Technical Area 1: Automated signoff-quality verification of circuits of unknown origin

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**TA1/2** **Stanford University**

*Open source model checkers and instruction-level abstractions for arbitrary hardware and mixed-signal models for formal verification of analog IP blocks*

**Dr. Clark Barrett**

Upscale: Scaling Up Formal Tools for POSH Open Source Hardware

$5.9M

Partner: Princeton University

# Posh Open Source Hardware (POSH)

Technical Area 1: Automated signoff-quality verification of circuits of unknown origin

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**TA2** **Univ. of Washington**

*PDK-independent topology description language for the delivery of open source mixed signal IP modules portable from 180nm to 14nm technology nodes*

**Dr. Richard C. J. Shi**

RAIL: Resilient Analog Instance Language Enabled Open Source Mixed-Signal Circuits

$2.5M

# Posh Open Source Hardware (POSH)

Technical Area 1: Automated signoff-quality verification of circuits of unknown origin

Technical Area 2: Establish IP to seed a nascent open source repository

**TA2** **Univ. of Washington**

*Higher performance open source 64-bit RISC-V multicore processor*

**Dr. Michael Taylor**

WABOSH: Washington and BU do Open Source Hardware

$2.7M

Partner: Boston University

# Posh Open Source Hardware (POSH)

Technical Area 1: Automated signoff-quality verification of circuits of unknown origin

Technical Area 2: Establish IP to seed a nascent open source repository

**TA2** **Princeton University**

*Open-source FPGA fabric and scalable coherence memory system for creation of an open source hardware ecosystem*

**Dr. David Wentzlaff**

CIFER: Coherent Interconnect and FPGA Enabling Reuse

$1.8M

Partner: Cornell University

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**TA2** | **Univ. of Southern CA**

*High-performance open-source analog circuits*

**Dr. Tony Levi**

Automated AMS IP generator for CMOS technologies

$6.0M

Partner: GlobalFoundries

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Technical Area 2: Establish IP to seed a nascent open source repository

**TA2** **University of Utah**

*Open-source FPGA generation framework*

**Dr. Pierre-Emmanuel Gaillardon**

An Automatic IP Generator for Customizable FPGA Architectures

$0.9M

# Posh Open Source Hardware (POSH)

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**TA2** **Brown University**

*Open-source circuits and software for thermal, voltage, and process sensors, employing an exploratory solver based on a distributed set of die sensors*

**Dr. Sherief Reda**

A SW/HW Sensory-Rich Monitoring System for SoC Designs

$0.6M

# Posh Open Source Hardware (POSH)

Technical Area 1: Automated signoff-quality verification of circuits of unknown origin

Technical Area 2: Establish IP to seed a nascent open source repository

**TA2**

**Le Wiz**

*High-quality open-source implementations of Ethernet controllers*

**Mr. Chinh Le**

Ethernet Controller Open Source IP Cores

$0.6M

# Software Defined Hardware (SDH)

Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning

Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

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Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning
Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

**TA1**

**Qualcomm**

*Dynamically optimizable data path for multi-core systems*

**Mr. Shekhar Borkar**

Qameleon: Software Defined Processor for Data Analytics

$2.0M

# Software Defined Hardware (SDH)

Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning
Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

**TA1**

**Intel**

*High throughput compute near memory and interconnect networks*

**Dr. Joshua Fryman**

Spatial Memory Organization for Reconfigurable Systems (SMOReS)

$4.5M

# Software Defined Hardware (SDH)

Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning

Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

**TA2** **Georgia Tech**

*Automatically discover and generate parameterized kernels for hardware and software co-optimization*

**Dr. Vivek Sarkar**

DDARING: Dynamic Data-Aware Reconfiguration, Integration and Generation

$4.5M

Partners: University of Illinois at Urbana-Champaign, University of Michigan, University of Southern California

# Software Defined Hardware (SDH)

Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning

Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

**TA2** **Systems & Technology Research**

*Data dependent Just-in-Time hardware/software compilation*

**Dr. Brad Gaynor**

MITCHELL

$5.5M

Partners: Northeastern University, Purdue University

# Software Defined Hardware (SDH)

Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning

Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

**TA1/2** **NVIDIA**

*Reconfigurable compute arrays with explicit data orchestration*

**Dr. Stephen Keckler**

SYMPHONY: Orchestrating Sparse and Dense Data for Efficient Computation

$22.7M

Partners: Massachusetts Institute of Technology, University of Illinois at Urbana-Champaign, University of California-Davis

# Software Defined Hardware (SDH)

Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning
Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

**TA1/2** **Univ. of Washington**

*Polymorphic hybrid ASIC/FPGA architectures*

**Dr. Michael Taylor**

HammerBlade: Continuous Synthesis of Polymorphic Hardware/Software

$9.0M

Partners: Cornell University, Dini Group, Xilinx

# Software Defined Hardware (SDH)

Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning

Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

**TA1/2** **Princeton University**

*Specialized and decoupled data compute and data supply programming for malleable tile-based computation*

**Dr. Margaret Martonosi**

DECADES: Deeply-Customized Accelerator-Oriented Data Supply Systems Synthesis

$5.8M

Partner: Columbia University

# Software Defined Hardware (SDH)

Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning
Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

**TA1/2** **University of Michigan**

*Fast, low energy interconnect for reconfigurable compute arrays*

**Dr. Ron Dreslinski**

Transmuter: A Reconfigurable Computer

$9.0M

Partners: ARM, Arizona State University, University of Edinburgh

# Software Defined Hardware (SDH)

Technical Area 1: Runtime reconfigurable processors for data analytics and machine learning
Technical Area 2: Programming languages and compilers that jointly optimize hardware and software

**TA1/2** **Stanford University**

*Hybrid configurable arrays coupled with on-the-fly compiler optimization*

**Dr. Kunle Olukotun**

Plasticine: A Universal Data Analytics Accelerator

$8.0M

Partner: SambaNova Systems

# Domain-Specific System on Chip (DSSoC)

Technical Area 1: Design-time specialization, with run-time allocation of heterogeneous processors for better mapping of software to hardware

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Technical Area 1: Design-time specialization, with run-time allocation of heterogeneous processors for better mapping of software to hardware

**TA1**

**Stanford University**

*Visual computing program will use agile design techniques to enable application experts to develop ideas quickly for an optimized SoC for visual computing*

**Dr. Mark Horowitz**

Aha: Visual Computing

$6.4M

# Domain-Specific System on Chip (DSSoC)

Technical Area 1: Design-time specialization, with run-time allocation of heterogeneous processors for better mapping of software to hardware

**TA1**

**Arizona State Univ.**

*Heterogeneous processors with specialization to support multifunction RF systems that require dramatically increased processing flexibility at low power*

**Dr. Daniel Bliss**

Domain-Focused Advanced Software-Reconfigurable Heterogeneous System on Chip (DASH-SoC)

$17.4M

Partners: University of Michigan, University of Arizona, Carnegie Mellon University, General Dynamics, ARM, EpiSyS

# Domain-Specific System on Chip (DSSoC)

Technical Area 1: Design-time specialization, with run-time allocation of heterogeneous processors for better mapping of software to hardware

**TA1**

**IBM**

*Quickly design and implement an easily programmed domain-specific SoC for real-time cognitive decision engines within smart connected vehicles*

**Dr. Pradip Bose**

EPOCHS: Efficient Programmability of Cognitive Heterogeneous Systems

$14.7M

Partners: Columbia University, Harvard University, University of Illinois at Urbana-Champaign

# Domain-Specific System on Chip (DSSoC)

Technical Area 1: Design-time specialization, with run-time allocation of heterogeneous processors for better mapping of software to hardware

**TA1** **Oak Ridge Nat'l Lab**

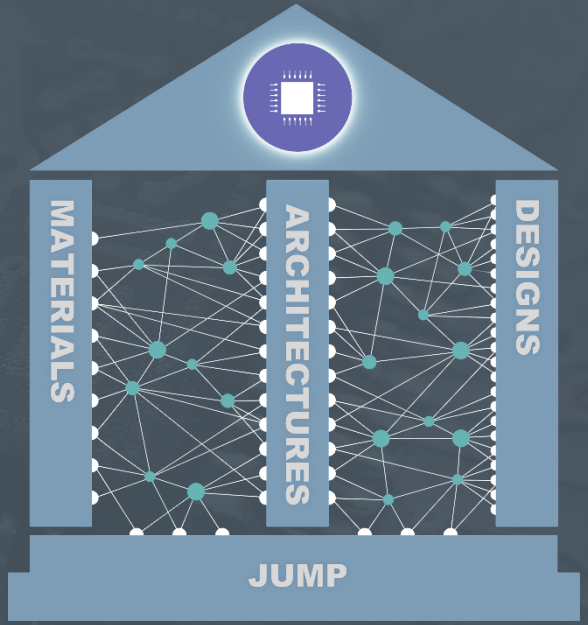
*New tools for performance modeling and quantitative analysis of domains to enable co-design of system-on-chip specialization*

**Dr. Jeffrey Vetter**

Cosmic Castle

$6.0M

# 2025 – 2030
# National Electronics Capability




# ERI ELECTRONICS RESURGENCE INITIATIVE

## SUMMIT

**2018** | SAN FRANCISCO, CA | **JULY 23-25**