



TOM BECKLEY

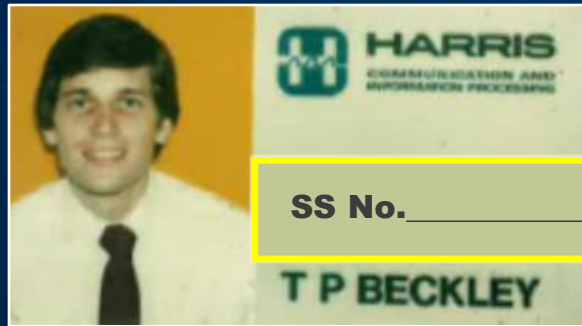
SENIOR VICE PRESIDENT
CADENCE DESIGN SYSTEMS

New Commercial DoD Partnership Models

Cadence System Design Enablement

Tom Beckley, Senior VP – R&D, Custom IC, IC packaging and PCB
DARPA ERI Summit
July 2018

A long history with US Government: DoD, DARPA, NASA, ...



SS No. _____

Not secure:
Employee ID #



cādence

1978

1981

1990

1998

2000

2004

Recent



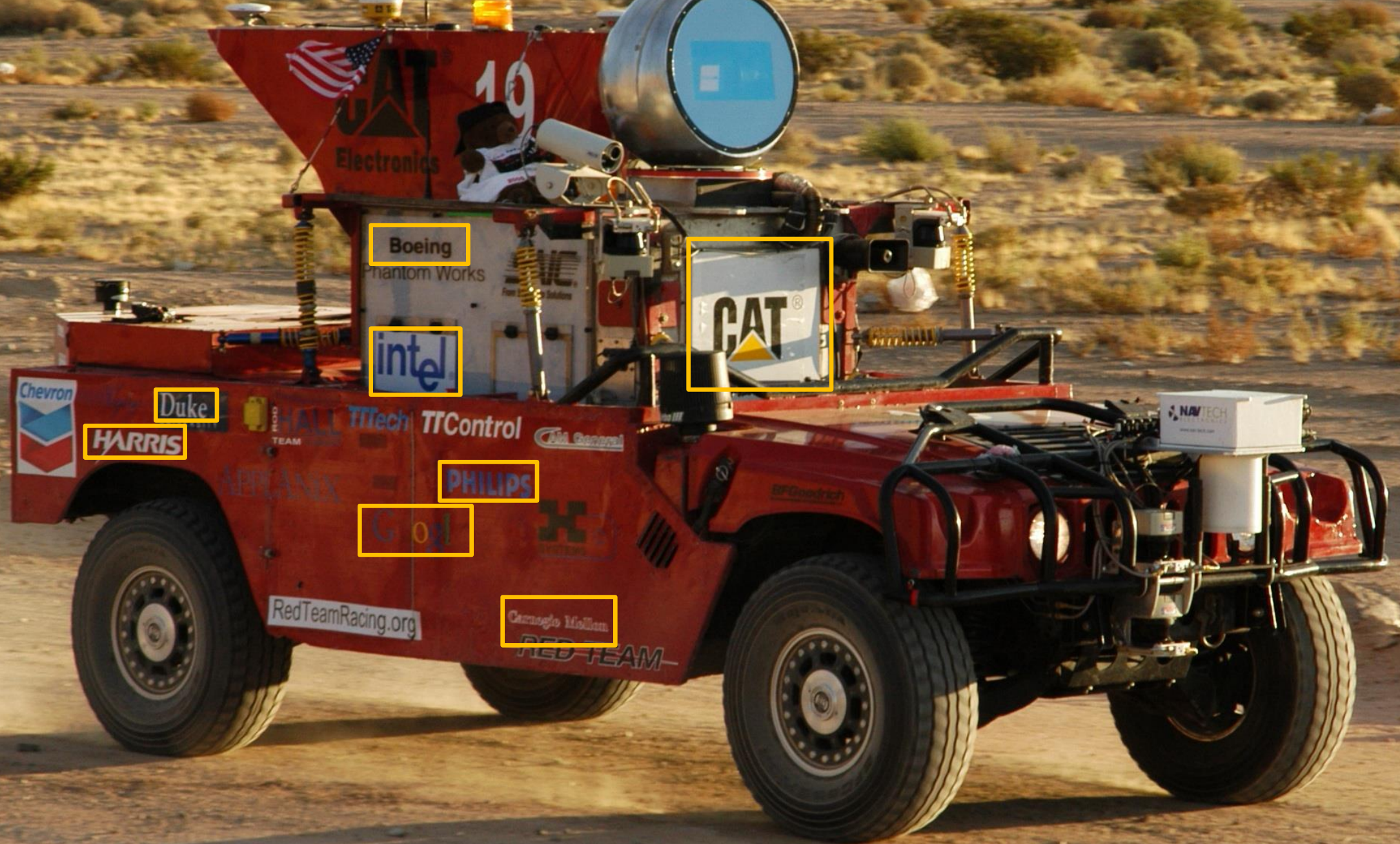
CRAFT
CHIPS
ERI

Tough
enough?

Try it
without
the driver.



DARPA Grand Challenge 2005



Boeing

Phantom Works

intel

CAT

Duke

HARRIS

HALL

TTTech

TTControl

General

PHILIPS

Google

RedTeamRacing.org

Carnegie Mellon

RED TEAM

NAV TECH

Cadence Overview

Commitment to Innovation



#38



7,200+
employees



4,400+ R&D engineers
1,500+ field engineers



26 global
development centers



Broad portfolio of
solutions-based products



20 new products in
the past 3 years;
50+ new IP products



40% of revenue
invested in
R&D



1686 patents
worldwide

Industry 4.0 ↔ Smart Product World ↔ Fourth Technology Revolution

With its Highest Growth Rate in 14 Years, the Global Semiconductor Industry Topped \$429 Billion in 2017, IHS Markit Says

Samsung edged out Intel, to become the new semiconductor industry leader BusinessWire 3/28/18

Non-Traditional Chips Gaining Steam

Flexible hybrid electronics are showing up in a variety of markets where electronics never existed before.

MARCH 15TH, 2018 - BY: JEFF DORSCH SEMICONDUCTOR ENGINEERING

Chipmakers bet on the 'big bang' of artificial intelligence

Tim Bradshaw in Los Angeles NOVEMBER 19, 2017 *Financial Times*

Engineering in the Twilight of Moore's Law

It's all about finding and riding the big waves

By Robert W. Lucky 15 Feb 2018 *IEEE Spectrum*

Moore's Law Is Dying -- So Where Are Its Heirs?

By Radoslav Danilak 9 Mar 2018 *Forbes Magazine*

The first real 5G wireless standard is official

The final technical details of the 5G NR will be available later this week when the full standard specifications are released (the documents will be available on the [3GPP portal](#)). For now, we know it will cover wireless bands from 600MHz all the way up to millimeter wave signals in the 50GHz range. Sprint is making sure everyone knows its 2.5GHz band is [included in 5G NR](#), which makes it the largest holder of sub-6GHz 5G spectrum.

12/21/17 Ryan Whitwam *Android Police sourcing Qualcomm*

DARPA lays out cash-splash to defibrillate Moore's Law

Electronics resurgence program gets US\$75 million more for 2018

By Richard Chirgwin 14 Sep 2017 *The Register*

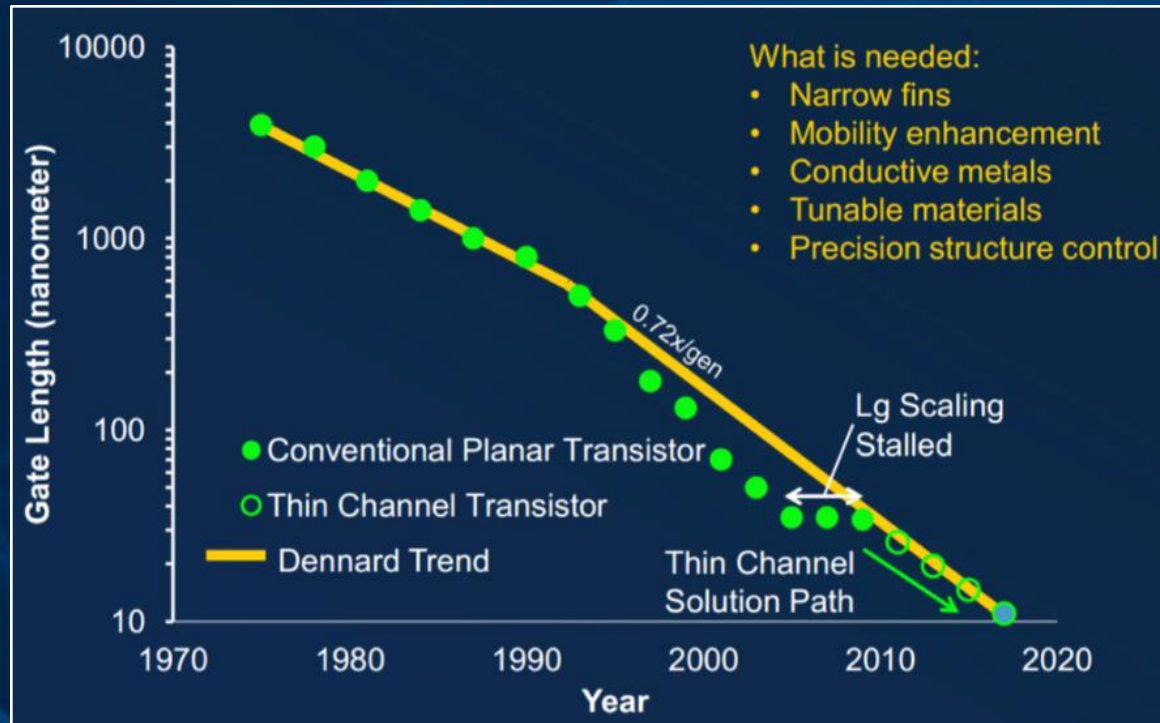
New Technology Revolution Unfolds

Impacting DoD, IC and System Companies

- Fusion of electrical, mechanical, sensors, RF, software, and Cloud
- Leverage research into commercial solutions using unique partnerships
- Mining deep data using machine learning and AI
- Security, safety, reliability paramount
- Semi/Systems boundaries morphing; China aggressively investing



Amidst Continuous Technology Disruption



Beyond Moore's Law



Additive Manufacturing & Robotics

System Design Enablement & Industry 4.0



Mobile



Automotive



IoT



Cloud/Data Center



Medical



5G



Robotics



Aero/Defense

Systems Integration



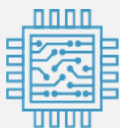
System analysis * Hardware/Software verification * Software applications

Package and Board



PCB design * Package design * Analysis * Mechanical/PLM integration

Chip/IC



Design and implementation * IP/SoC verification * Software drivers



Intellectual Property



Security

Expanding Collaborations

Partnering for System Design Enablement

Cadence Collaboration Platform-Based

Design flow integration seamlessly within the

San Jose, Calif., 06 Dec 2018

Cadence Design Systems Inc.

To improve productivity, of the Virtuoso Analog Design and frequency-domain modeling designed to account for integration with the Virtuoso parameterization for fast challenges as photonic capabilities.

Arrow Electronics Development Engineers

Centennial, Colo. and San Jose, Calif., 06 Dec 2018

Arrow Electronics (NYSE: ARW) announced a collaboration with Cadence Design Systems to accelerate the pace of development and cheaper.

As part of the collaboration, Cadence's OrCAD® suite of printed circuit board (PCB) design tools, including online component and reference design, can help engineers design and ensure that their designs have lifecycles consistent with the product.

The collaboration also allows teams to add the OrCAD® suite of design tools to their existing OrCAD design tools.

Cadence SoC and Hosted Design

SAN JOSE, Calif., 06 Dec 2018

Cadence Design Systems Inc. announced a complete hosted end-to-end Internet of Things (IoT) offering accelerates next-generation Subsystem for Cortex-A72 and ARMv8.2 implementation solutions.

To further lower barriers to entry, Cadence's program to provide to customers the ARM IoT Subsystem solution a designer may use their IoT applications, including package and DesignSense software-as-a-service methodologies. With access to tools without

Cadence Design Systems and NI Announce Collaboration to Simplify Next-Generation Semiconductor and RF Development

AUSTIN, Texas, and SAN JOSE, Calif., 22 May 2018

Highlights:

- Cadence and NI collaborate to improve the overall semiconductor development and test process, reducing design cycle time and improving quality of results for next-generation wireless, automotive and mobile products
- Cadence launches comprehensive, new Virtuoso RF Solution, enabling engineers to design, implement and analyze RF modules and RFICs from within the Virtuoso custom IC design platform
- Unique EM simulation integration to support NI AWR AXIEM 3D planar EM software and Cadence Sigrity PowerSI 3D EM Extraction Option
- Cadence and NI jointly working to deliver common transistor models to ensure consistent simulation behavior between NI AWR Microwave Office circuit design software and the Cadence Spectre simulation platform

Cadence Design Systems, Inc. (NASDAQ: CDNS) and NI (NASDAQ: NATI) today announced a broad-ranging collaboration to improve the overall semiconductor development and test process of next-generation wireless, automotive and mobile integrated circuits (ICs) and modules. To meet customers' needs for a streamlined and comprehensive solution, Cadence and NI have pursued projects that integrate key

Media Contacts

For more information, please contact:

Cadence Newsroom
408.944.7039
newsroom@cadence.com

Share

[Facebook](#) [Twitter](#) [LinkedIn](#) [Email](#)

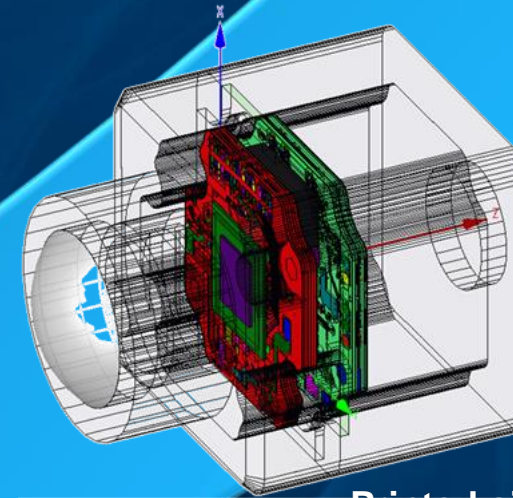


More to come...

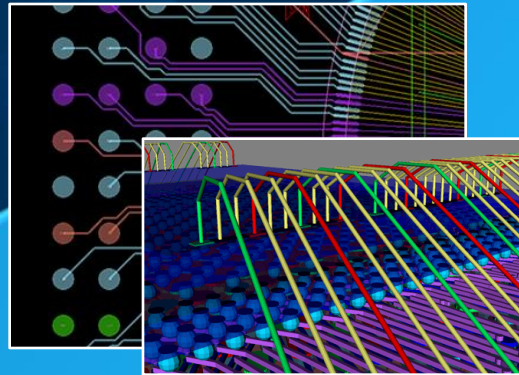
Enabling complex system design

Integrating IP, IC, package, PCB, and analysis

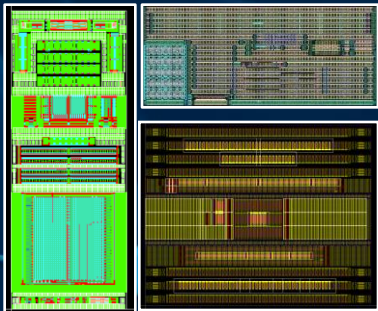
- “More than Moore” transforming
- Designing, analyzing, and verifying multi-die, multi-technology, complex systems
- Automating design using Machine Learning/AI



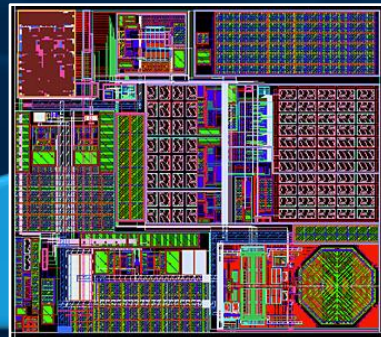
Printed circuit board



Chip packaging



IP



Integrated circuit

5G Changes Everything

- Intersection of cloud computing, big data analytics, and AI
- Backbone of information systems
- Capacity, connectivity, latency, long battery life, security, and reliability
- 5G RF system complexity is exponentially increasing

40X faster than 4G, with up to 1M connections per m²

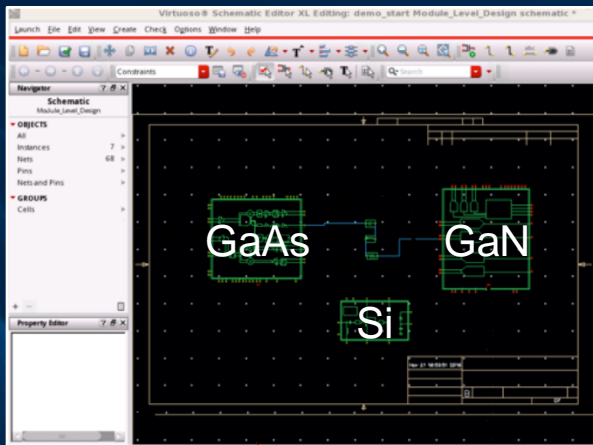


5G “New Radio” / Wireless Design Technologies

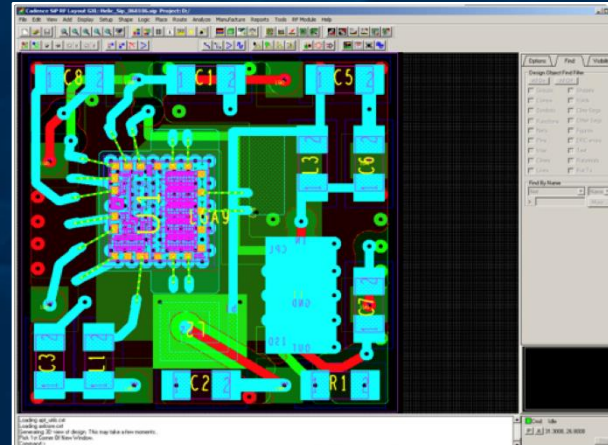
Wireless is a rapidly emerging opportunity for suppliers



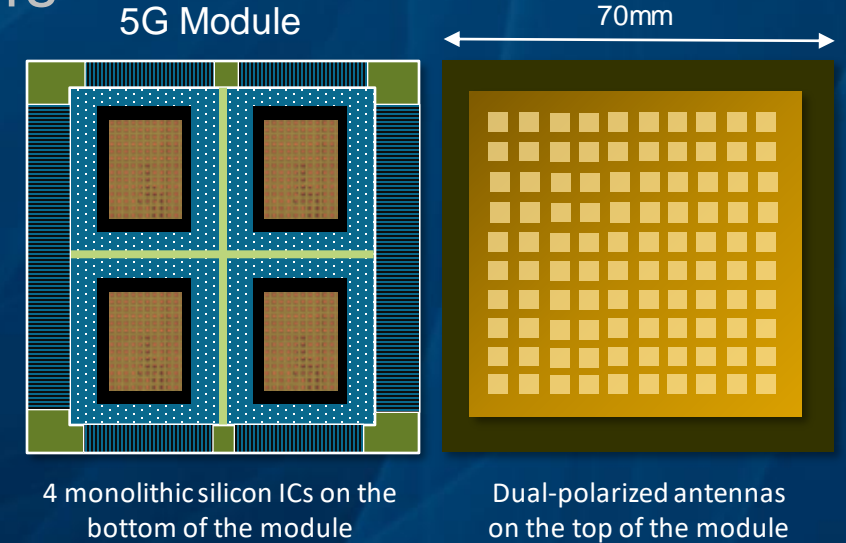
- Must integrate analog, RF, optical, and advanced packaging – including wafer level
- Exponential design complexity
- Complex RF and microwave systems



Single schematic – ICs & package mixed process technologies



Allegro® module / package



GaN

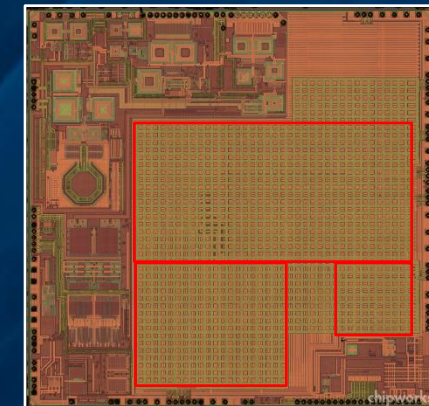
WiFi or Bluetooth IC

Analog

5mm

Digital

Radio + MAC
+ Baseband
Low-Noise
Amplifier (Rx)
Power
Management
Unit
Power
Amplifier (Tx)



Low-Energy
Processor
On-Chip
Memory

Digital
Baseband

Sensor I/O:
UART, SPI, I2C,
26 GPIO

Picture ©Chipworks

Robotic Systems



	Industrial robots/100 workers	Labor-cost savings (%, 2025)
 Korea	      	33%
 Singapore	    	25%
 Japan	  	25%
 Germany	  	21%
 USA	 	22%
 Taiwan	 	22%
	World Average 0.75	World Average 16%



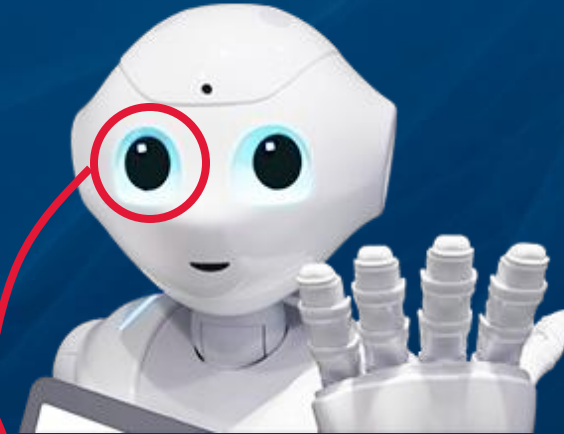
Global market industrial and non-industrial robots from 2016 to 2022 (\$B)

Source World Robotics 2017 Source Boston Consulting Group

Spatial Perception Camera Module



Chassis 1
with lens



Chassis 2
with Ethernet Cable-out

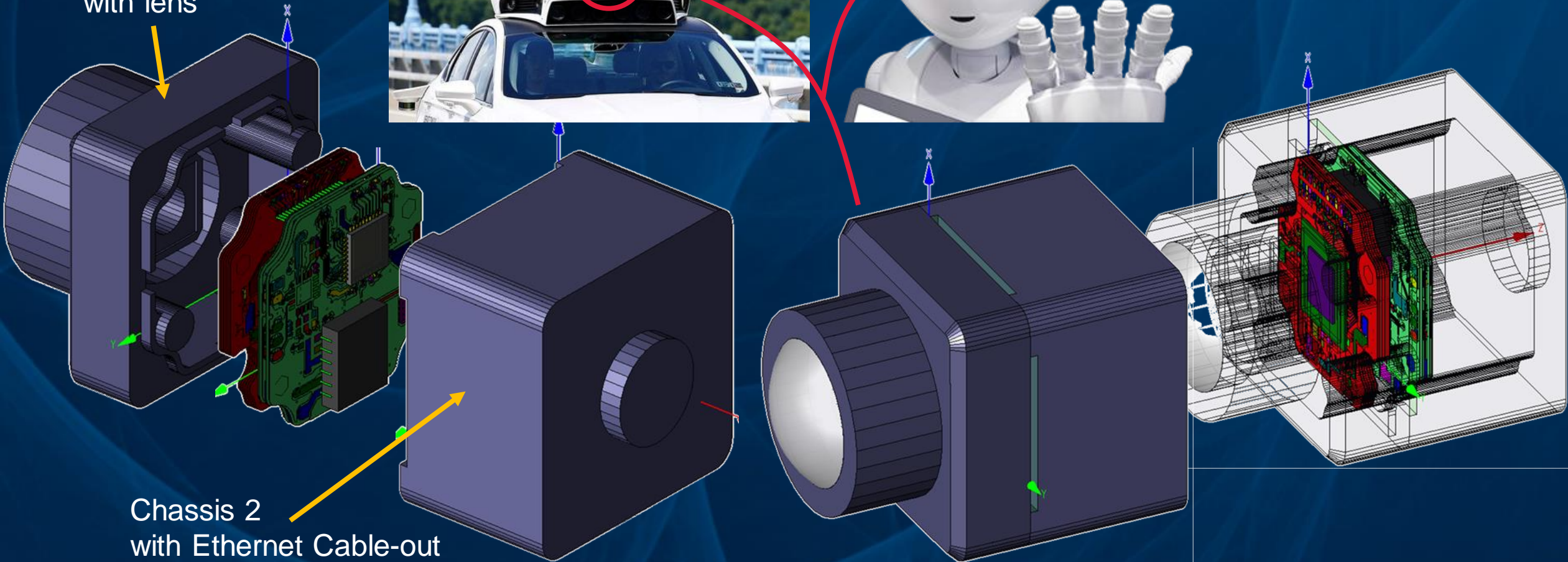
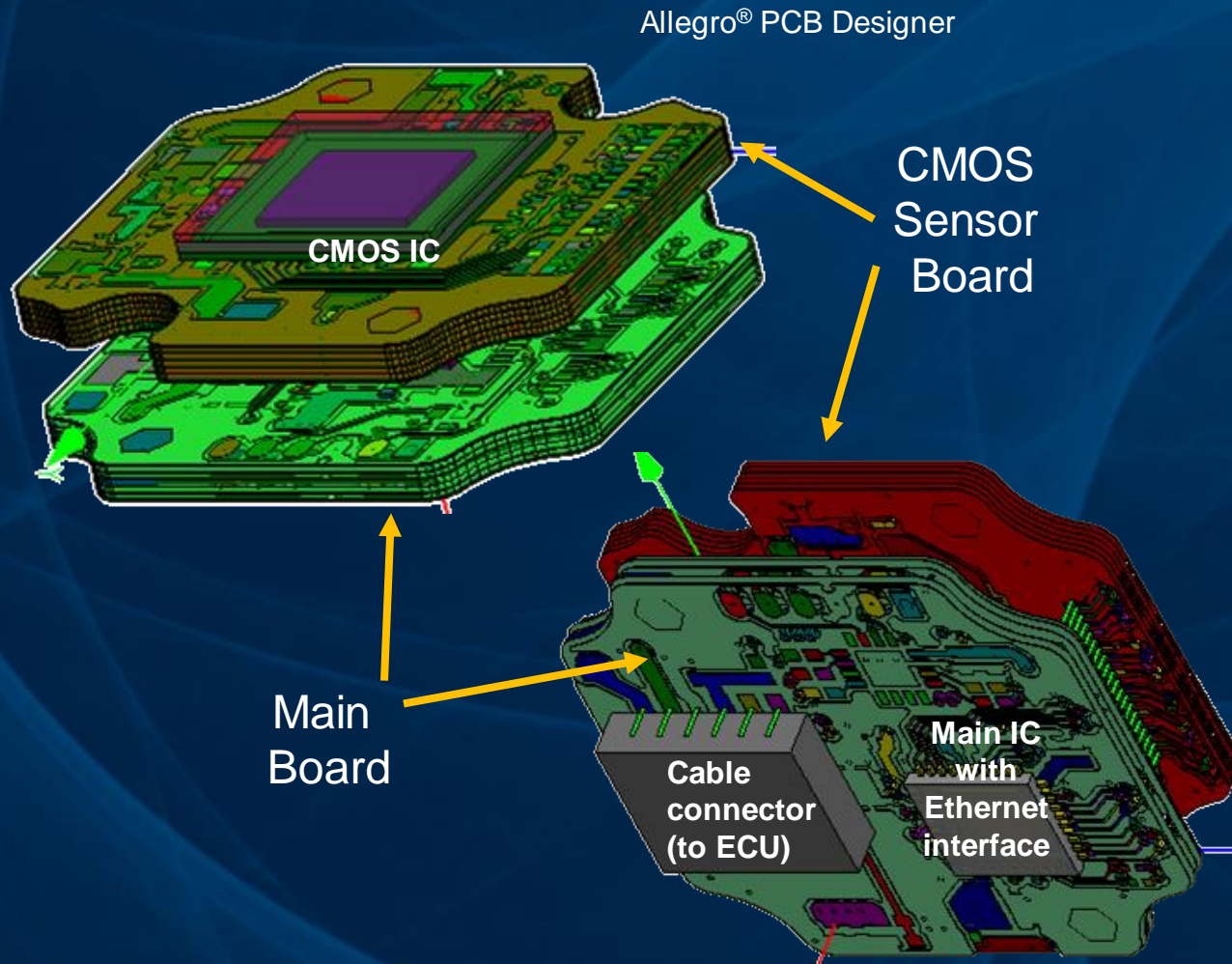
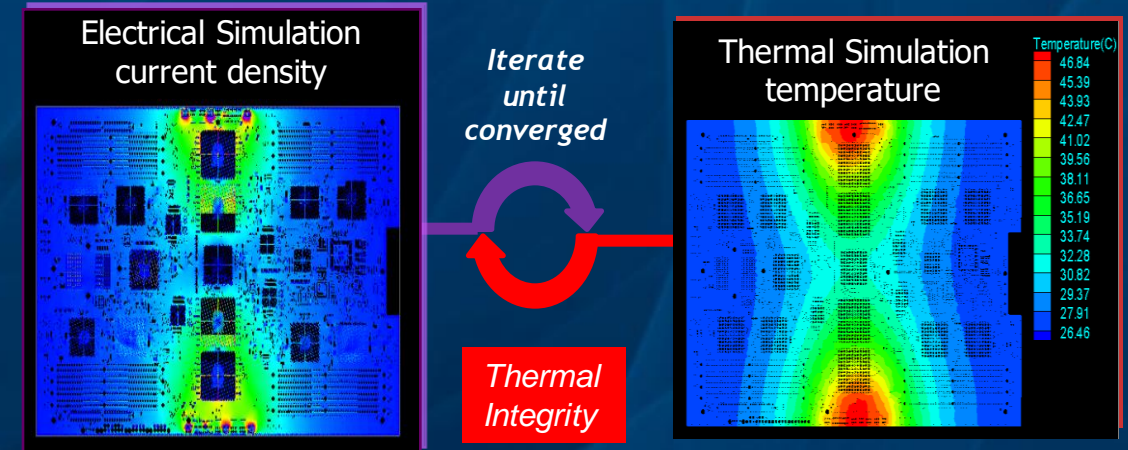


Image Sensor

Design, analysis, integrity

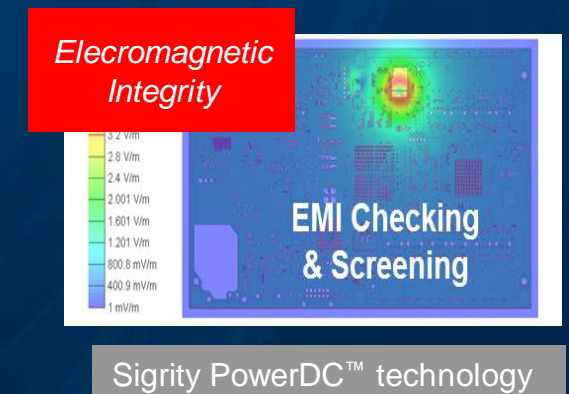
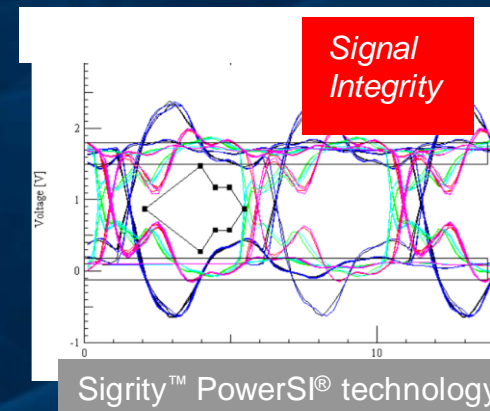


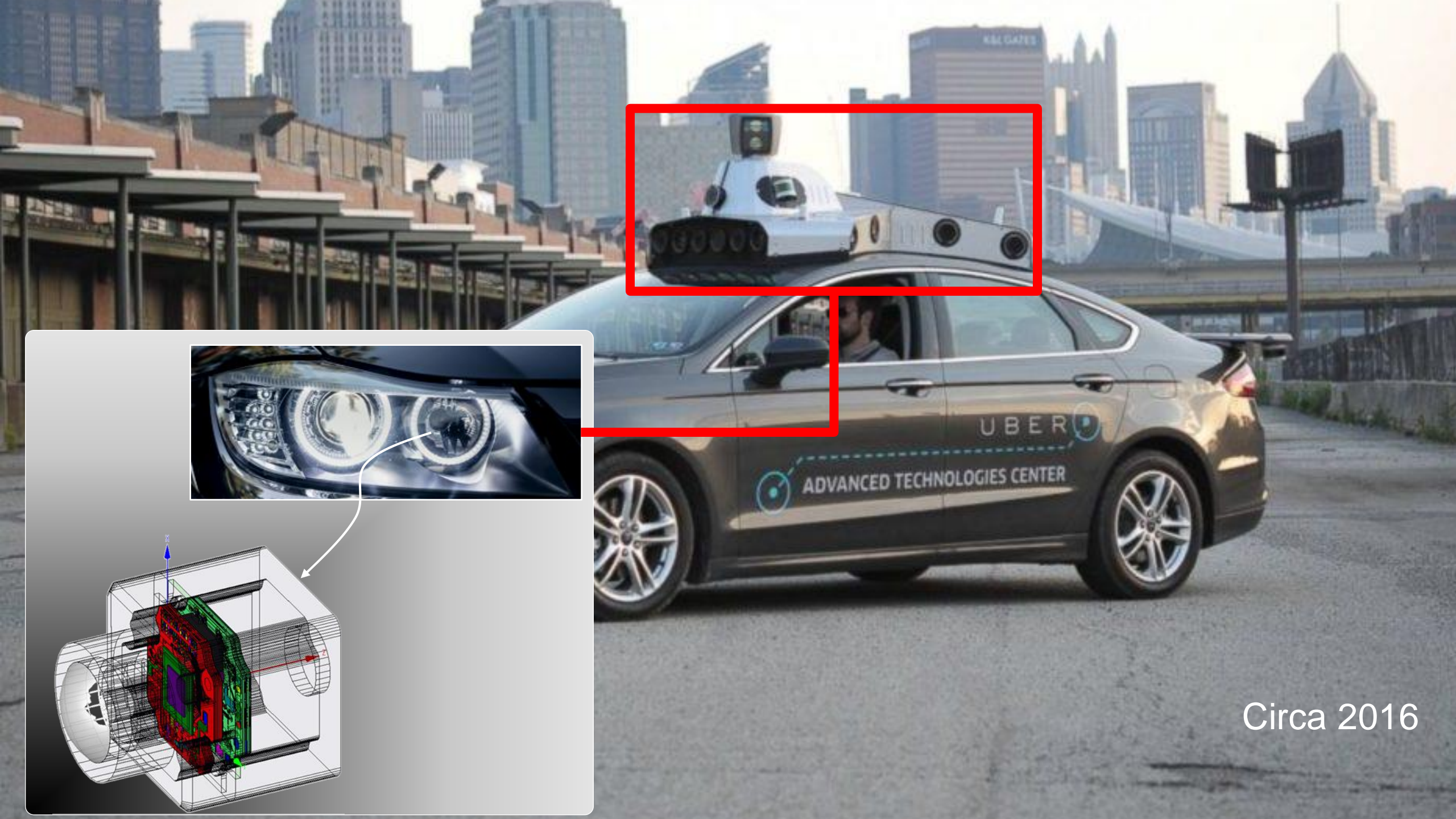
Sigrity PowerDC™ technology



- Resistance increases with temperature
- Component leakage power dissipation increases with temperature

- Copper (Joule) heating
- Component heating





Circa 2016

Autonomous Vehicles

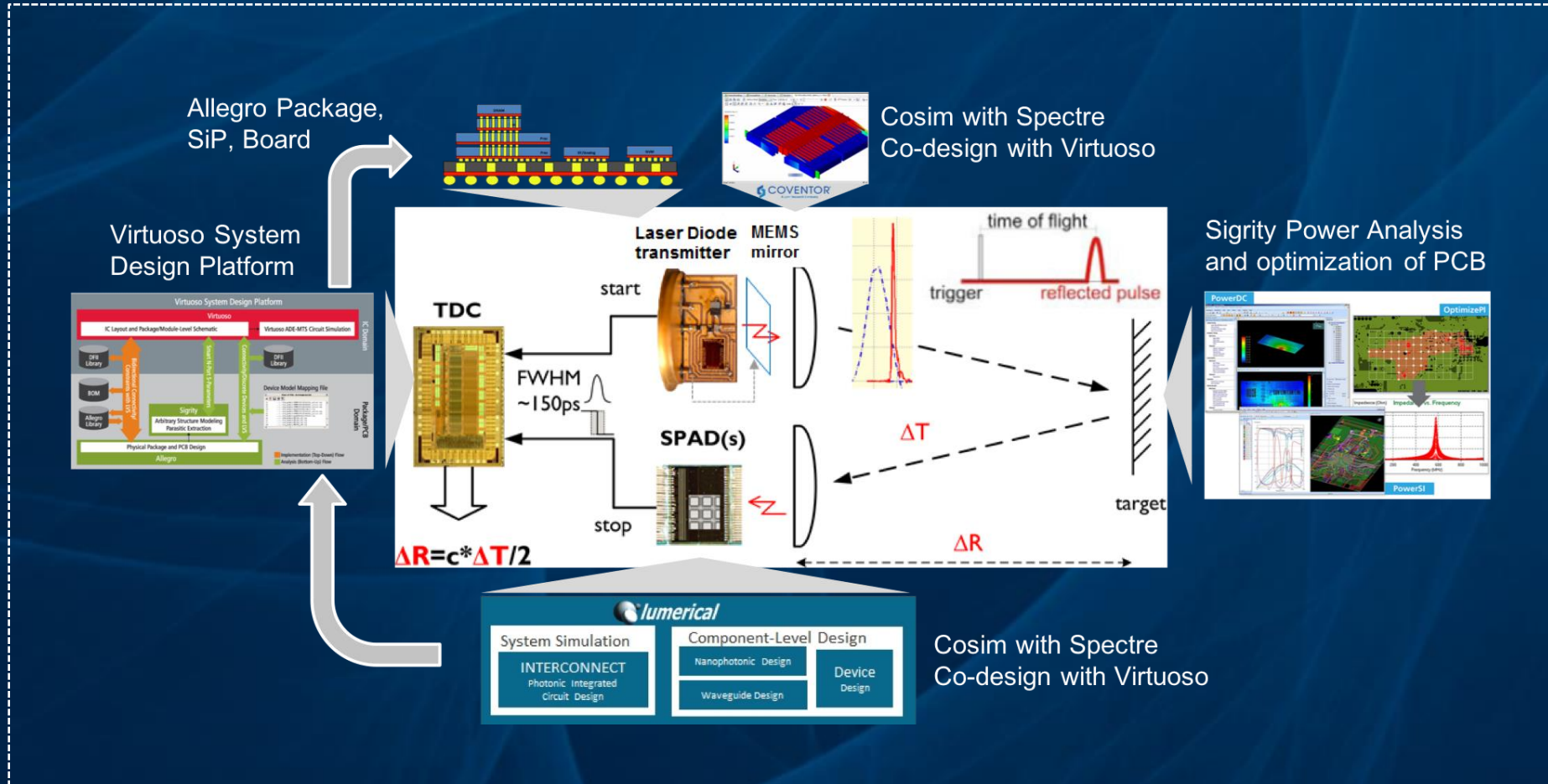
Pulsed time-of-flight Lidar system



  system design including beamforming algorithm toolkit



System design



2018 National Defense Strategy

“Platform electronics and software must be designed for routine replacement instead of static configurations that last more than a decade...deliver performance at the speed of relevance.”

Virtuoso Liberate

Recent Cadence DARPA Collaborations

Modus

Virtuoso Schematic Editor

Sigrity

— IP reuse through 2.5D Modular Design

Tempus Timing Signoff Solution

Innovus

Virtuoso Layout Suite

Genus

— Worlds smallest IC

Palladium Dynamic Power Analysis

Quantus

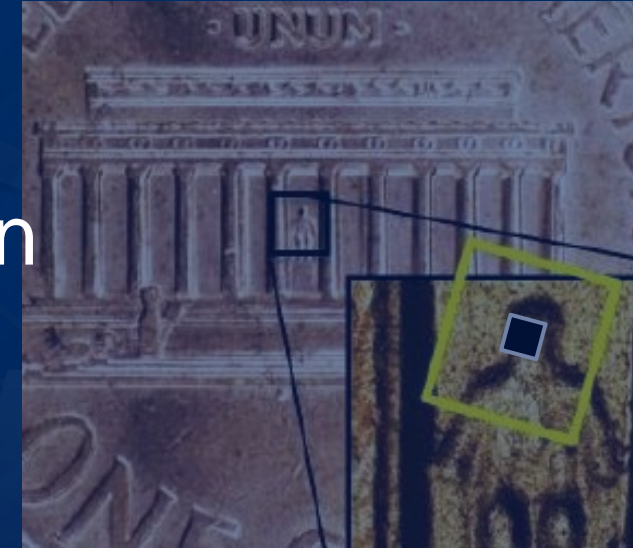
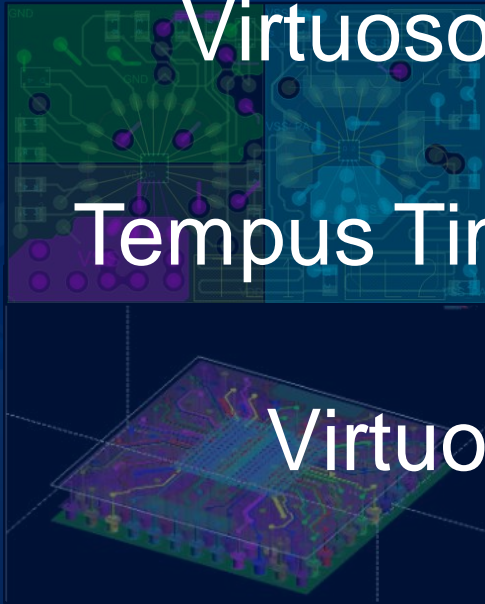
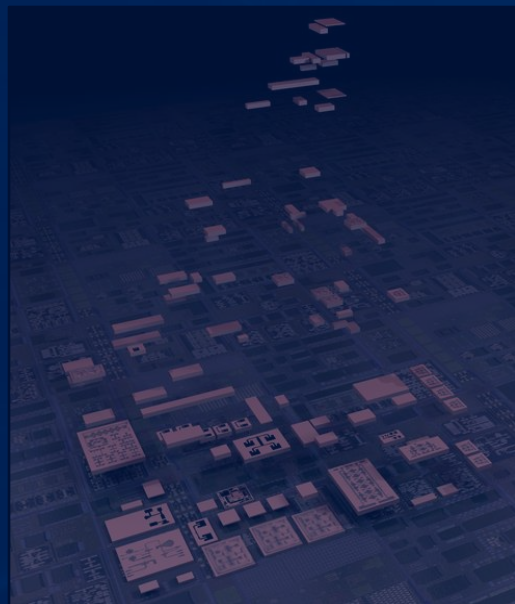
Achieved 4x reduction in Power and Area over prior generation

JasperGold

Xcelium

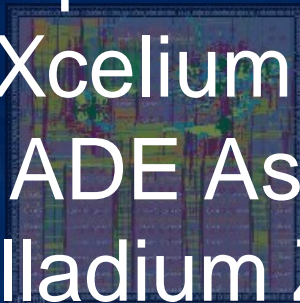
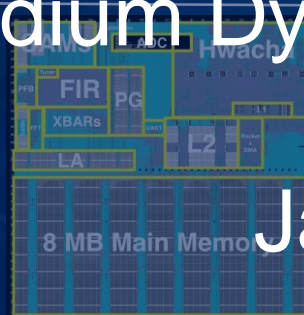
Virtuoso ADE Assembler

Palladium Z1



CRAFT

- Collaboration aimed at reducing DoD SOC design and verification time by 10x




SPADE

- Advanced security techniques focused on DoD system requirements

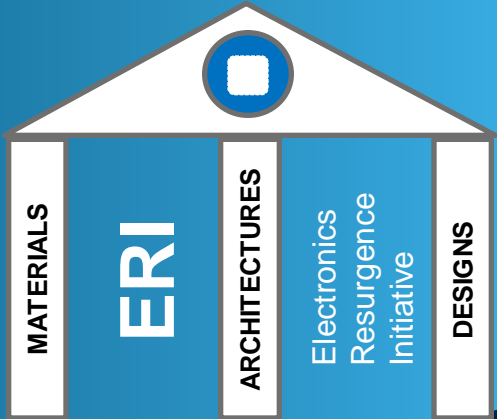
Commercial DoD Partnership Model

Collaboration across government, academia and technology leaders



ERI Proposal
(intelligent chip, package and board design)

2025-2030
NATIONAL ELECTRONICS CAPABILITY

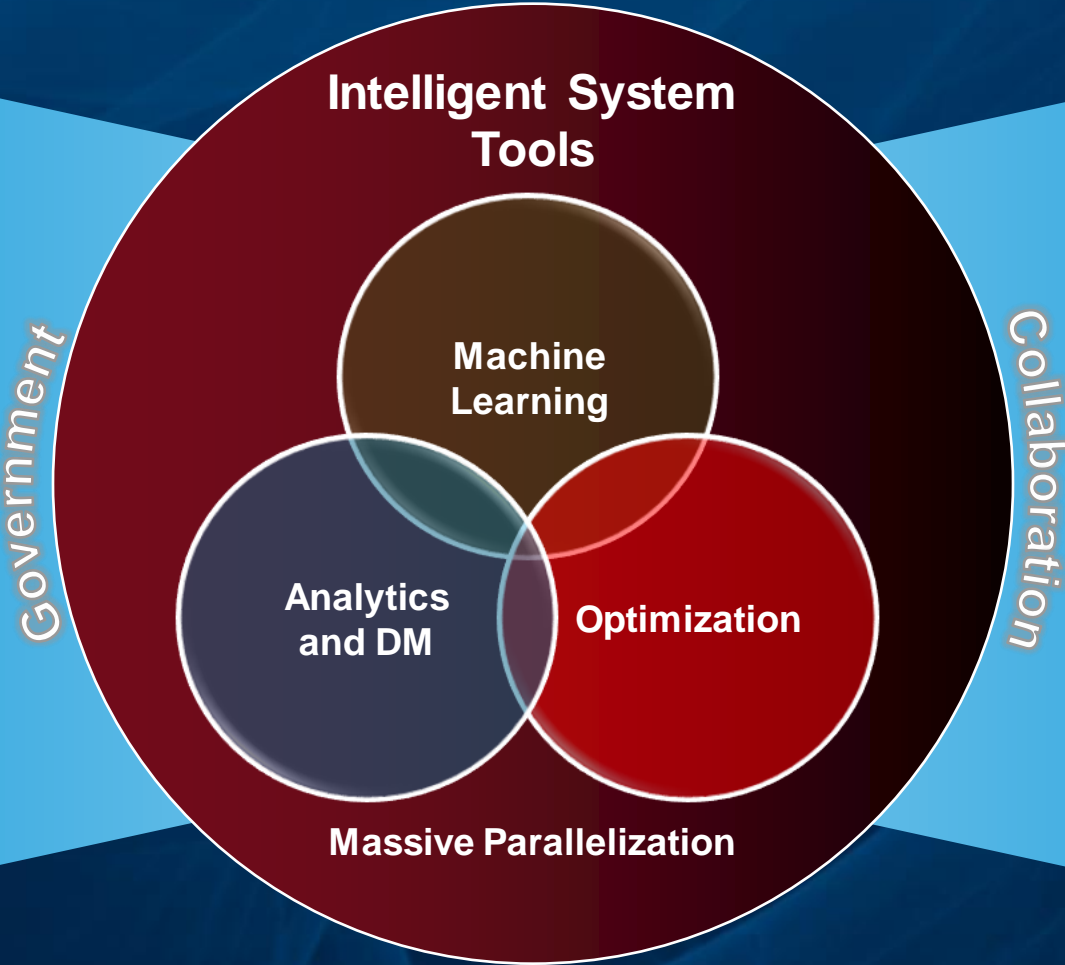



ERI

MATERIALS | ARCHITECTURES | DESIGNS

Electronics Resurgence Initiative

JUMP + Traditional Programs






Carnegie Mellon University

+

cādence®

+

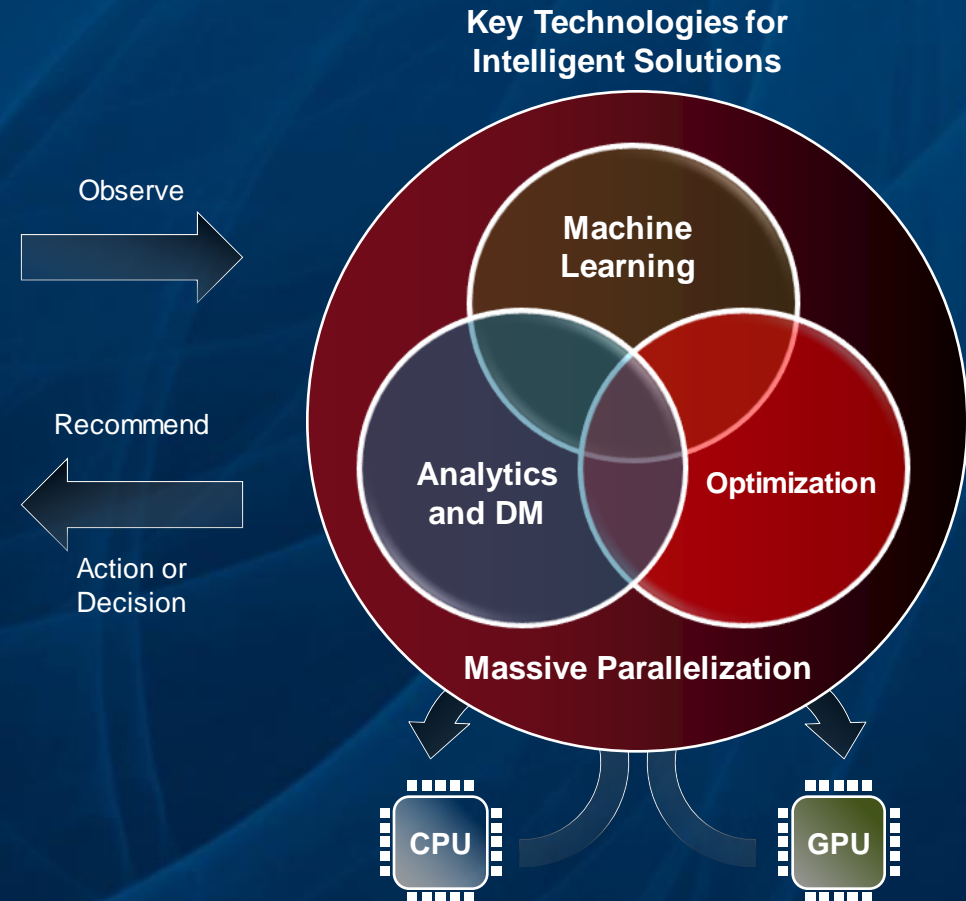
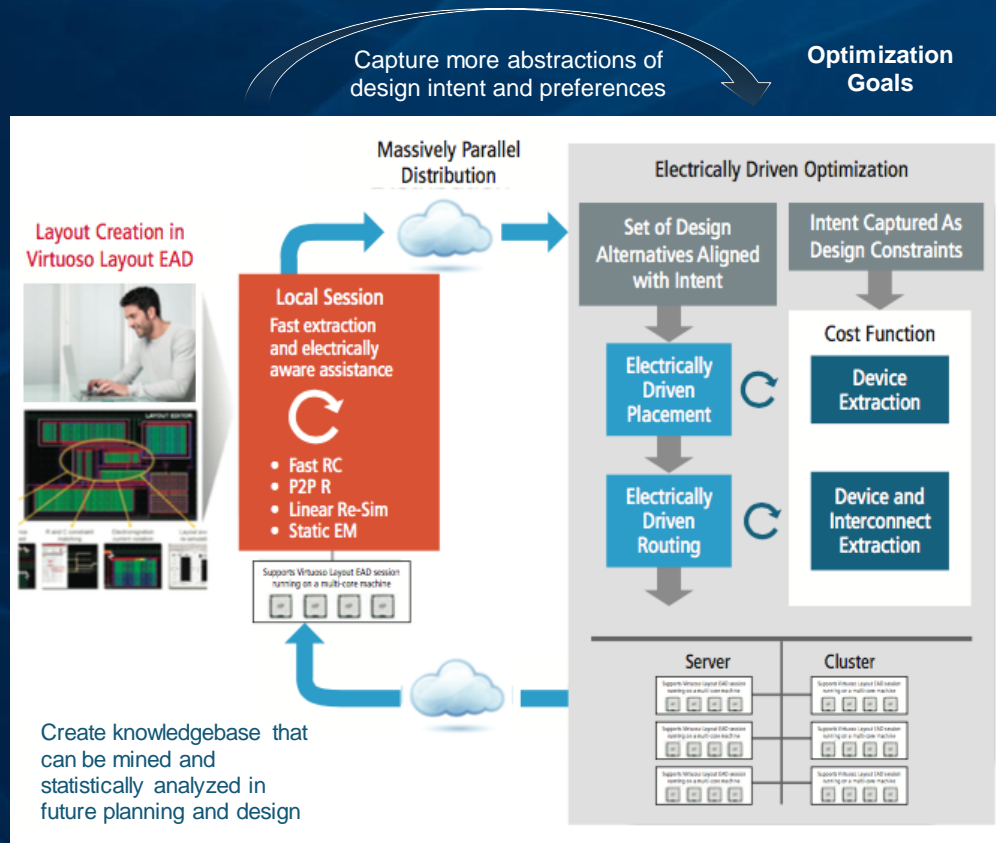


AUTOMATION

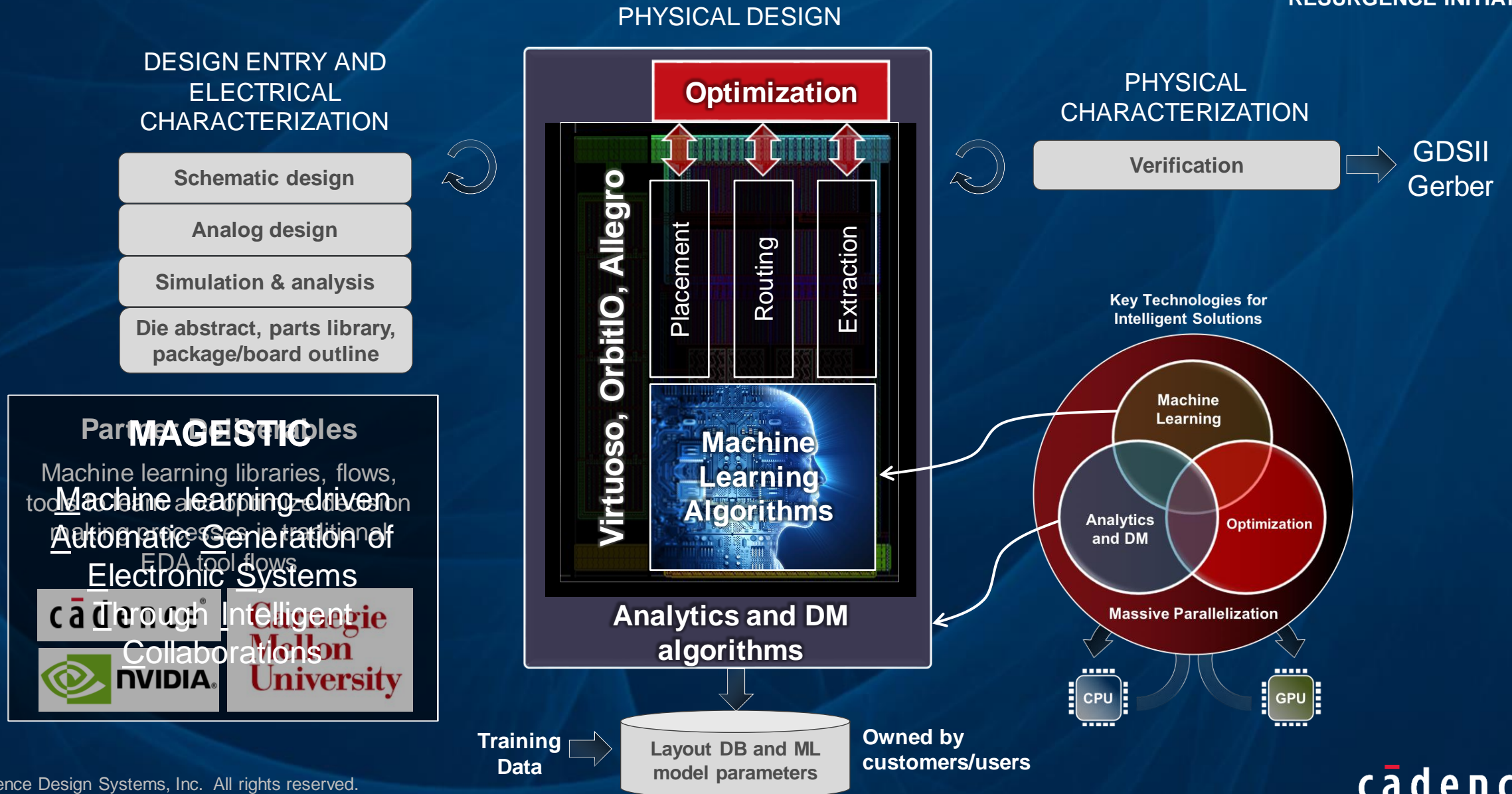
nvidia

Intelligent Design and Optimization

Addressing the Uncertainty of Design Intent



MAGESTIC: Analog Block/SoC/Pkg/PCB Automation



Industry 4.0 Teaming / Innovating: Govt, Industry & Academia

Advanced
Research Projects

**CRAFT, ACT,
CHIPS, SPADE,
SHIELD, REIMAGINE,**



**Carnegie
Mellon
University**

cā d e n c e[®]
**System Design
Enablement**



Integrated chip,
package, PCB, and
system

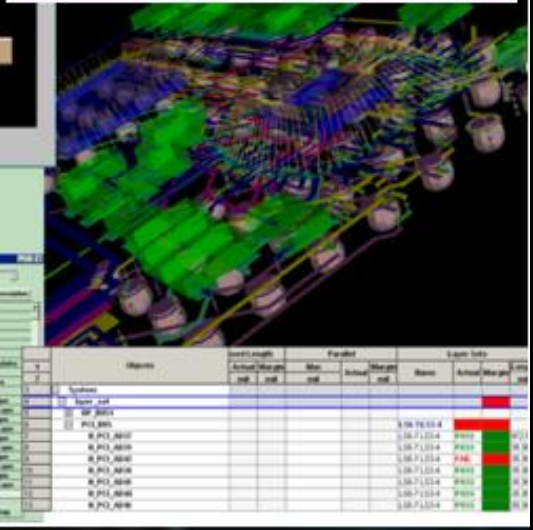
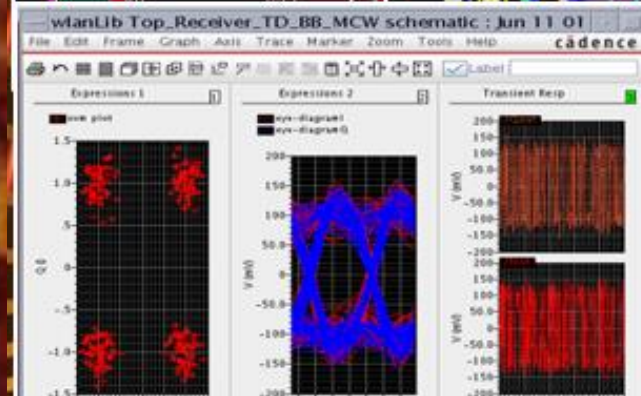
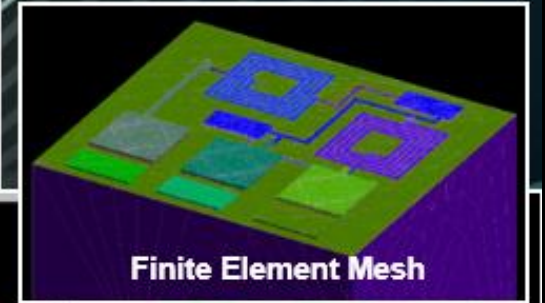
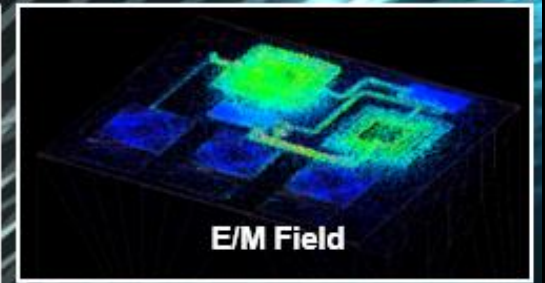
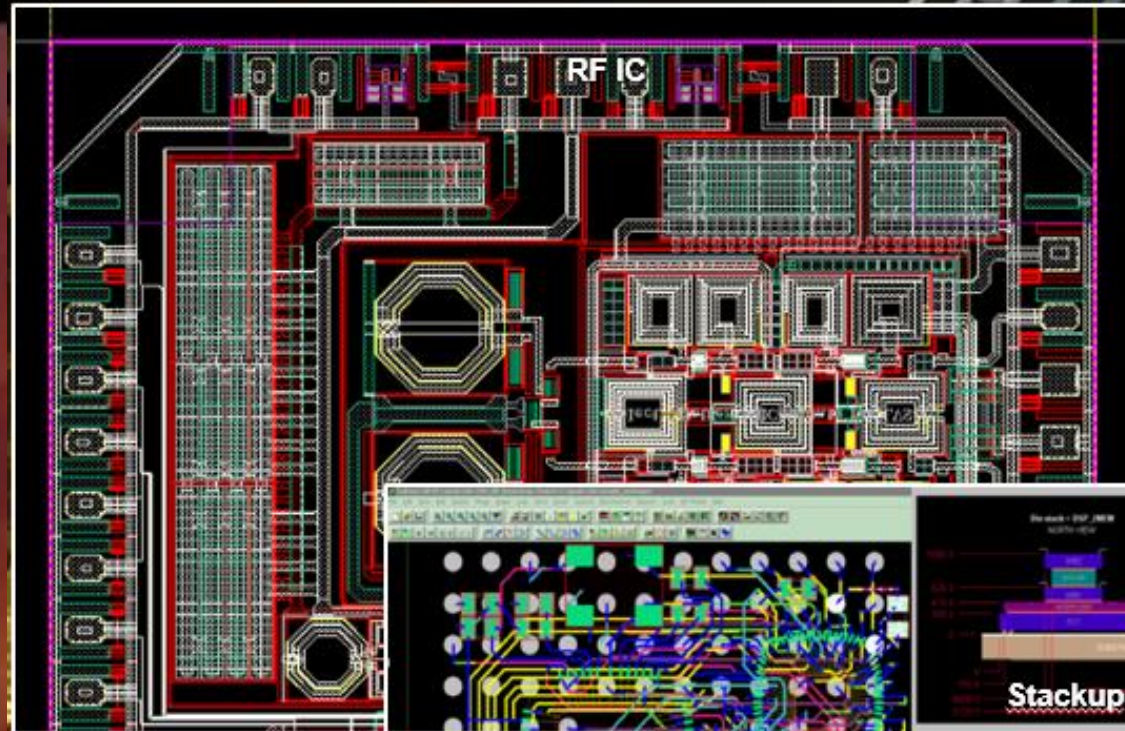
System modeling and
analysis

RF / photonics /
mixed-signal

SI/PI, fault simulation
& thermal analysis

Tough
enough?

Try it
without
the engineer.



DARPA ERI GRAND CHALLENGE 2018



Thanks!



ERI **ELECTRONICS RESURGENCE INITIATIVE**

S U M M I T

2018 | SAN FRANCISCO, CA | **JULY 23-25**