MIKE MAYBERRY

CTO AND MANAGING DIRECTOR
INTEL LABS

THE FUTURE IS SO BRIGHT

THE ERA OF HETEROGENEOUS COMPUTE

MIKE MAYBERRY
CTO AND MANAGING DIRECTOR OF INTEL LABS

Copyright © 2018 Intel Corporation

Legal Information

This presentation contains the general insights and opinions of Intel Corporation ("Intel"). The information in this presentation is provided for information only and is not to be relied upon for any other purpose than educational. Statements in this document that refer to Intel's plans and expectations for the quarter, the year, and the future, are forward-looking statements that involve a number of risks and uncertainties. A detailed discussion of the factors that could affect Intel's results and plans is included in Intel's SEC filings, including the annual report on Form 10-K.

Any forecasts of goods and services needed for Intel's operations are provided for discussion purposes only. Intel will have no liability to make any purchase in connection with forecasts published in this document. Intel accepts no duty to update this presentation based on more current information. Intel is not liable for any damages, direct or indirect, consequential or otherwise, that may arise, directly or indirectly, from the use or misuse of the information in this presentation. Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Learn more at intel.com, or from the OEM or retailer.

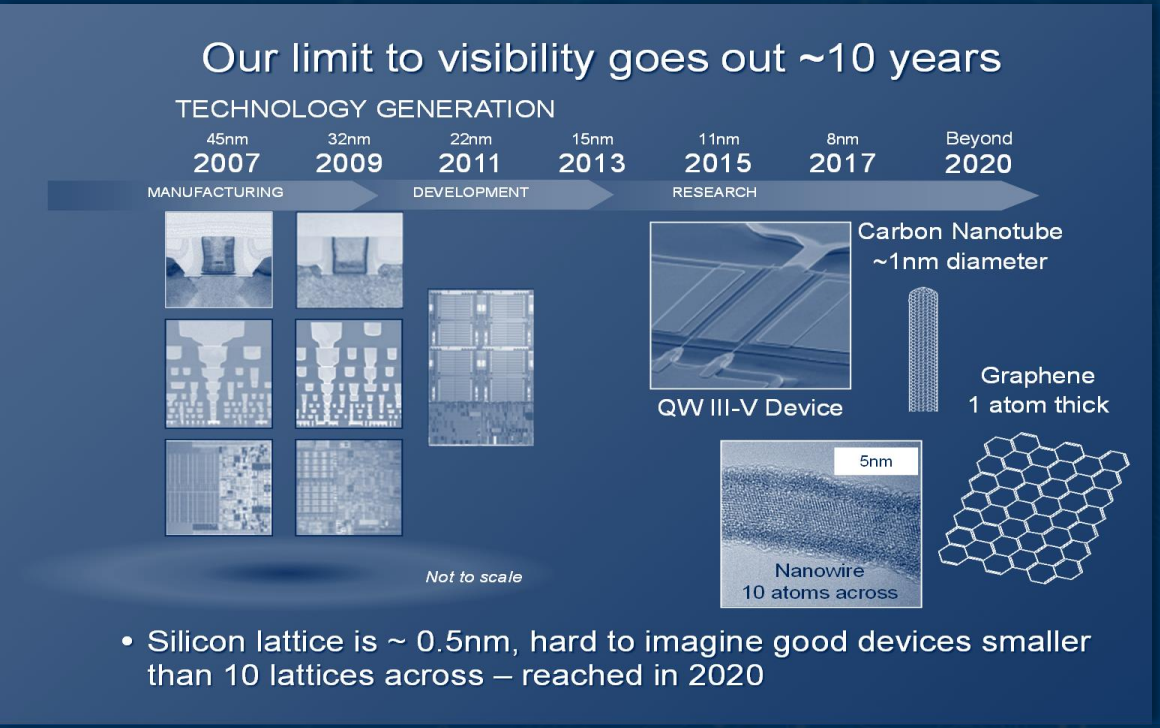
Copyright © 2018 Intel Corporation.

Intel, the Intel logo, are trademarks of Intel Corporation in the U.S. and/or other countries.

*Other names and brands may be claimed as the property of others

A BRIEF LOOK BACK …

~10 Years Ago Research Focus



80% of internal research projects involved novel materials

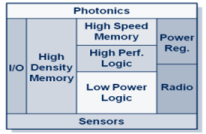
The remainder used chemistry for dimensional control

~5 YEARS AGO RESEARCH FOCUS

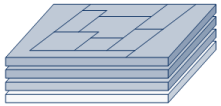
Four Thrusts along with CMOS Scaling

Heterogeneous System Integration

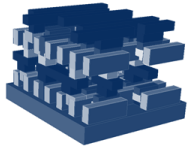
2D Integration (SoC)



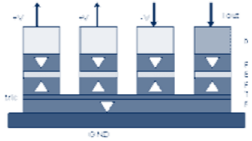
3D Integration (SiP)



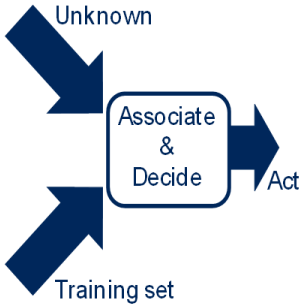
3D Process and Design



Novel Functions



Novel Data Processing Architectures



The new Moore's Law is the center column

New product directions in physical integration and architecture

PAST RESEARCH MESSAGES

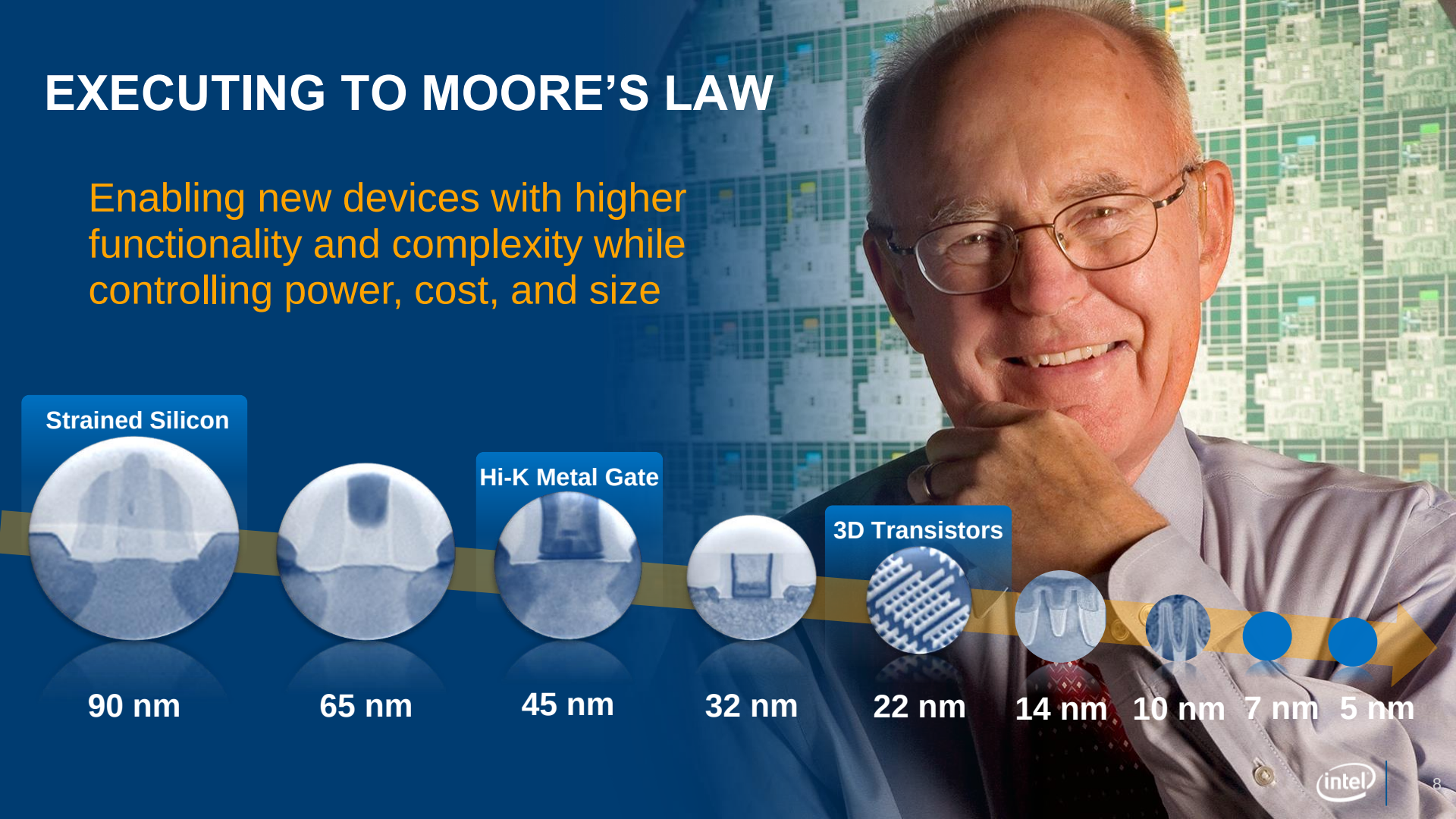
Scaling research is increasingly about materials, precision and control limit us more than physics

New opportunities are arising from increasing integration, architectures, and connectivity

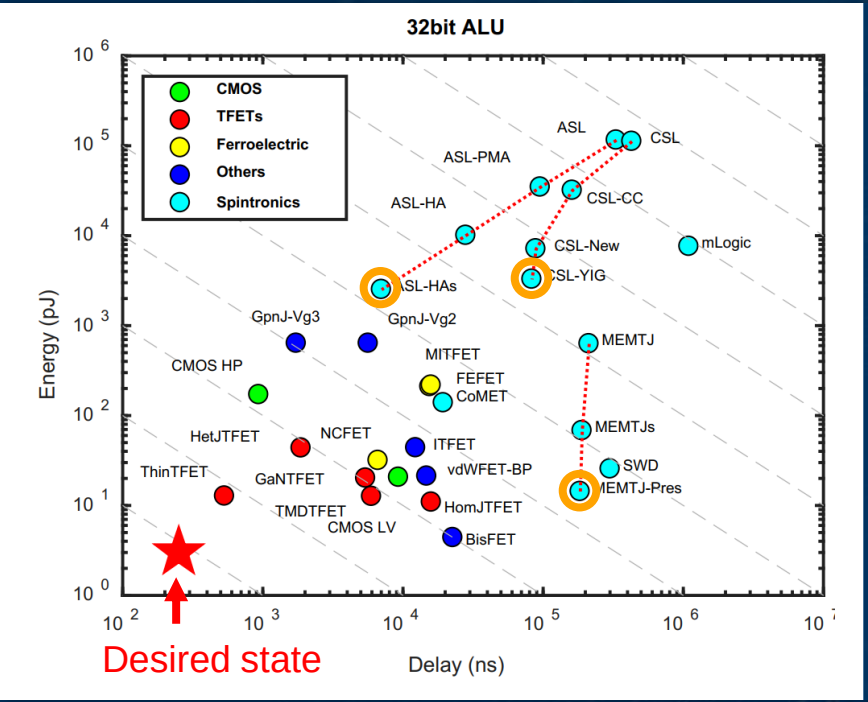
Moore's Law continues but is evolving

EXECUTING TO MOORE'S LAW

Enabling new devices with higher functionality and complexity while controlling power, cost, and size



A MEASURE OF PROGRESS – MORE AND BETTER OPTIONS



Improved efficiency of switching

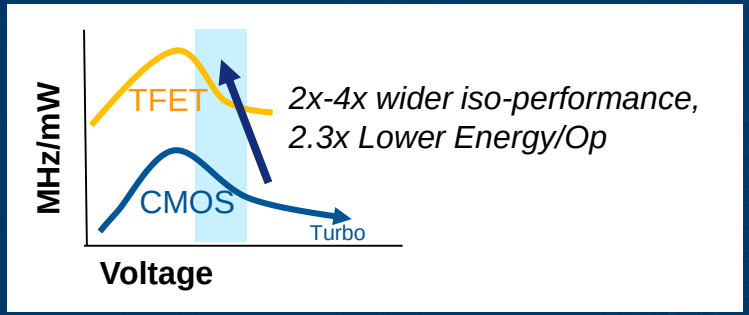
Electronic interconnects

Better understanding of logic circuits

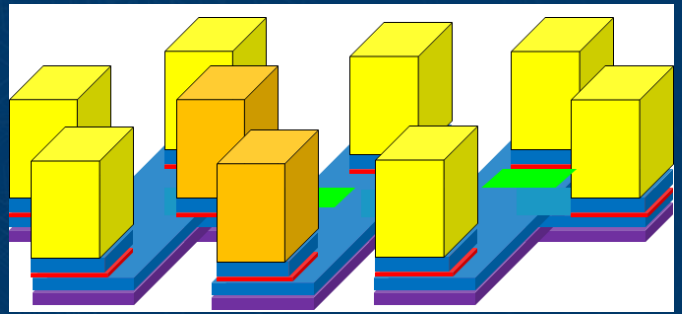
ENABLED BY ACADEMIC-INDUSTRY-GOVERNMENT

Source: C. Pan; A. Naeemi. "An Expanded Benchmarking of Beyond-CMOS Devices Based on Boolean and Neuromorphic Representative Circuits" IEEE Jan 2018
10.1109/JXCDC.2018.2793536

KEY FOCUS AREAS



Steep Threshold
and Nonvolatile
for ultra low power



Novel logic
to enable dense compute

TECHNOLOGY THAT CAN STACK

JOINT UNIVERSITY MICROELECTRONICS PROGRAM

SRC JUMP

RF to THz Sensors and Communications

UC/Santa Barbara
Mark Rodwell

ComSenTer

Distributed Computing and Networking

CMU
Anthony Rowe

CONIX

Cognitive Computing

Purdue
Kaushik Roy

C-BRIC
Center for Brain Inspired Computing

Intelligent Memory and Storage

U/Virginia
Kevin Skadron

CRISP
Center for Research in Intelligent Storage and Processing in Memory

Advanced Architecture and Algorithms

U/Michigan
Valeria Bertacco

ada
Applications Driving Architectures

Advanced Devices, Packaging, and Materials

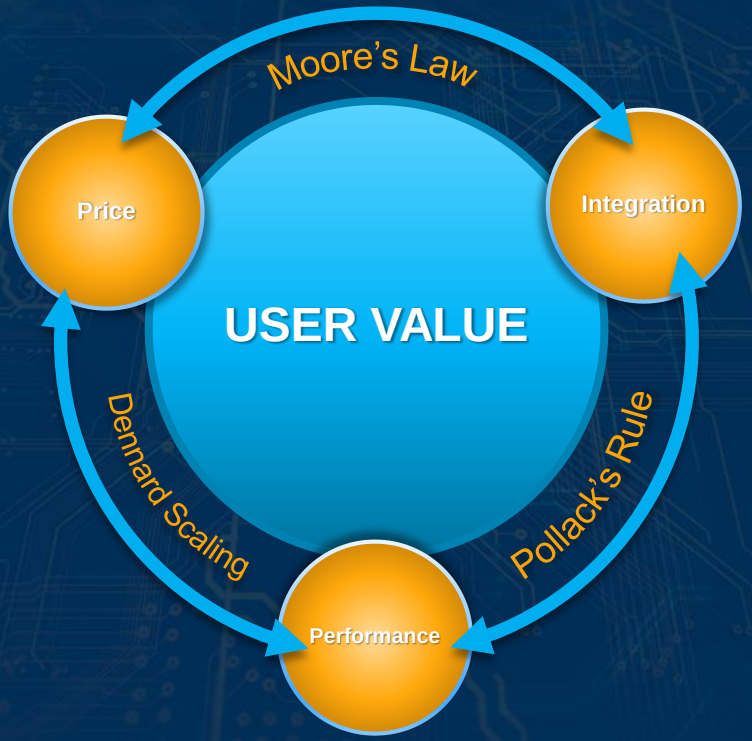
Notre Dame
Suman Datta

ASCENT

COMMUNITIES OF INNOVATION

*Other names and brands may be claimed as the property of others.

ECONOMICS TRUMPS TECHNOLOGY



REAL WORLD EXAMPLE

MICRON AND INTEL EXTEND THEIR LEADERSHIP IN 3D NAND FLASH MEMORY

Announce Qualification of Industry's First 4 bits/cell 3D NAND and Development of 96-Layer 3D NAND Structure

News Highlights

- Intel-Micron delivers the 1st commercially available 1Tb – 4bits/cell (QLC) die in the history of semiconductors
- Qualification of 4bits/cell 3D NAND on 64 layer 2nd Gen 3D NAND has been completed. 4bits/cell (QLC) provides 33% higher density compared to 3bits/cell (TLC)
- 3rd Generation 3D NAND uses 96 layers to maintain cost/density leadership
- 3rd Generation 3D NAND enables the industry's highest Gb/mm2 areal density

BOISE, Idaho and SANTA CLARA, Calif., May 21, 2018 – Micron Technology Inc. and Intel Corporation today announced production and shipment of the industry's first 4bits/cell 3D NAND technology. Leveraging a proven 64-layer structure, the new 4bits/cell NAND technology achieves 1 terabit (Tb) density per die, the world's highest-density flash memory.

Latency technology solutions known

Economics hinder realization

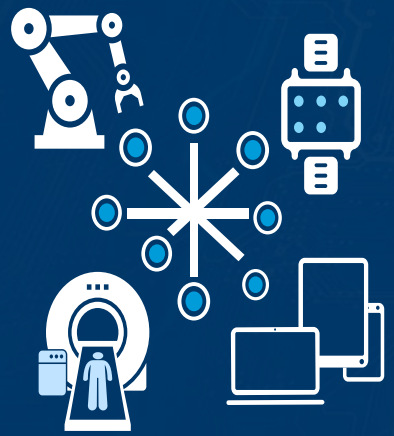
3D NAND is hard technology

Economics favor realization

PARTNERSHIPS CAN OFFSET ECONOMICS

MULTIPLE POSSIBLE FUTURES

Devices



Ambient

Cloud Computing

INDUSTRY WILL DELIVER

Higher integration, lower cost per function

Means to manufacture at scale – precision and control

Support for emerging workloads – once market size large enough

Continued power reduction for portable devices

Compute at scale

… but not all possible technologies

A USEFUL METAPHOR – OCEANS AND ISLANDS

Ocean represents big market general purpose

Islands represents specific purpose products

The ocean performance level rises over time

Their job is to be sufficiently better than the ocean

Why not use both?

RECONFIGURABLE COMPUTE

Intel FPGAs

Program goals

- AI algorithms are rapidly evolving and compute needs to evolve as well
- Enabling new algorithms and workloads that perform best on Intel platforms with FPGA
- Large-scale software frameworks are being developed and will drive the apps of tomorrow

COMMON HETEROGENEOUS INTEGRATION AND IP REUSE STRATEGIES (CHIPS)

Chiplet Library

14 nm

Cores	I/O	FPGA

10 nm

Cores	I/O	FPGA

Partners

Comms	I/O	Memory	Accelerator

Chiplets with different process nodes and system functions

Decouples ASIC / FPGA / Analog / RF design cycles

Program Goals

- Establish common interfaces
- Establish modular design flows
- Propose a System in Package CAD flow
- Create pre-validated chiplets
- Develop new business models
- Demonstrate 3X reduction in NRE and TTM

"The current system lacks the agility needed to adapt to new paradigms"

- DOD Advisory Panel Report, May 2017

OPPORTUNITIES FROM COLLABORATIONS

ACTIVELY ENGAGING MORE MEMBERS

Establish and demonstrate common interface standards

Announcing today

Enable the assembly of systems from modular IP blocks compliant

Demonstrate reusability of the modular IP blocks via rapid design iteration

*Other names and brands may be claimed as the property of others.

INTEGRATED AND OPTIMIZED STACK

ACCELERATOR OFFLOAD MODEL	System Administrator
SYSTEM SOFTWARE (OS & VMM)	Security
IA / IA-X Virtual ISA	Programmer
CPU, IAL, XPU PEs HARDWARE ARCHITECTURE	Hardware — **CHIPS focus**

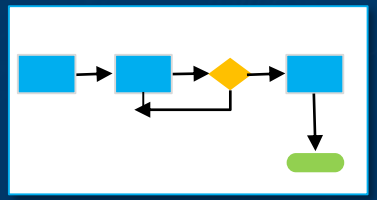
THINKING DIFFERENTLY

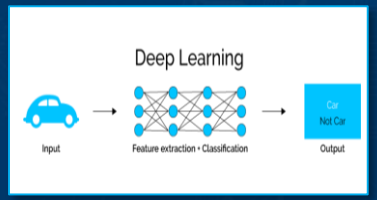
Conventional
- Known procedures
- Generate answers

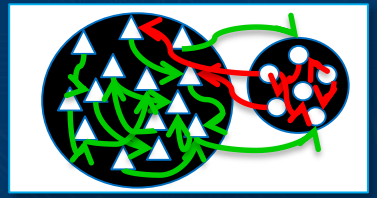
Deep learning
- Known answers
- Generate procedures with training

Neuromorphic
- Many procedures
- Adapt the answer with reinforcement

Quantum
- Answers superimposed
- Select and measure the answer







SUMMARY

System thinking, not just components

Moore's Law evolution
materials, novel devices and 3D are key

Commercial markets will find solutions, partnerships and heterogeneity will open possibilities

THE FUTURE IS BRIGHT

WHAT CAN WE INVENT WITH YOU?

Microsystems Technology Office

ERI ELECTRONICS RESURGENCE INITIATIVE

SUMMIT

2018 | SAN FRANCISCO, CA | **JULY 23-25**