NAVIGATING THE PERFECT STORM
ENABLING THE A.I. ERA

Gary Dickerson
President and CEO, Applied Materials
“Data is to this century what oil was to the last one: a driver of growth and change”

- The Economist
DATA GENERATION

IoT and Industry 4.0 driving an explosion of data

DATA STORAGE

More data needs to be processed and stored - Storage alone is not sufficient or economical

COMPUTE

New compute models to turn data into value

New compute architectures to process data at edge and in cloud at right performance / watt
Explosion of Data Generation

**INFLECTION YEAR**
Data generated by machines > humans

- **2017**
  - Machines: 1.5ZB (53%)
  - Humans: <10% (44%)

- **2018E**
  - Machines: 2ZB
  - Humans: <10%

- **2022E**
  - Machines: >10ZB
  - Humans: <10%

**SOURCE:** Applied Materials model based on forecasts published by Cisco, Intel, Western Digital
ACCELERATION OF A.I. FUELED BY

1. Very large, accessible **data** sets
2. Affordable **high performance computing** to turn data to $$$

MACHINE LEARNING = relentless classification of data to make determinations or predictions

SOURCE: Historic references based on New Street Research, May 2018
A.I. WORKLOADS NEED

A lot of memory
(because there’s a lot of data)

Parallel computing
(for throughput)

Extremely high logic ⇄ memory bandwidth

Sequential computing
General purpose
Good at many things

✓ Parallel computing
✓ Designed for throughput
✓ Great at specialized tasks
A.I. – BIG DATA DRIVING A RENAISSANCE OF HARDWARE DEVELOPMENT AND INVESTMENT

NOVEL HPC
- Quantum
- Synaptic

IN MEMORY COMPUTE
- Analog
- Memristor
- ReRAM/PCM

NEW MEMORIES
- MRAM
- ReRAM/CeRAM
- PRAM
- CeRAM
- FeRAM

NEAR MEMORIES
- DDR
- HBM (High bandwidth memory)
- Flash

ACCELERATORS
- TPU
- GPU
- ASICs
- FPGAs
1,000x

IMPROVEMENT IN COMPUTE PERFORMANCE / WATT NEEDED

SOURCE: DARPA, Intel, NVIDIA, A.I. startups
A.I. NEEDS EDGE AND CLOUD INNOVATIONS...

**STORAGE**
abundant low cost, high performance, low power data storage

+ **HPC**
orders of magnitude improvement in performance, energy efficiency and cost

WHILE AT THE SAME TIME...

**MOORE’S LAW CHALLENGED**
as classic 2D feature shrink slows

THE PERFECT STORM

OR

THE PERFECT OPPORTUNITY?
1965: MOORE’S THESIS BASED ON FIVE DATA POINTS
~1975: ESTIMATE UPDATED TO ‘DOUBLING EVERY 2 YEARS’

SOURCE: Electronics, Volme 38, Number 8, April 19, 1965
Projection Held For 40 Years...

Recent data points suggest

-2x more every 5 years

1970 - 2010

$\sqrt[40]{1,000,000} \approx 1.413$

$(1.413)^2$ more every 2 years

-2x more every 2 years

CLASSIC 2D FEATURE SCALING SLOWING

SOURCE: University of Wisconsin
PERFORMANCE IMPROVEMENTS OVER TIME
(VS. VAX-11/780)

- **1978**: 25% per year
- **1986**: 52% per year
- **2003**: 23% per year
- **2011**: 12% per year
- **2015**: 3.5% per year
- **2018**: 0%

End of Dennard Scaling
End of Moore's Law
Limits of parallelism of Amdahl's Law


TIME BETWEEN LOGIC NODES IN YEARS

<table>
<thead>
<tr>
<th>Node Size</th>
<th>Years</th>
</tr>
</thead>
<tbody>
<tr>
<td>45 to 32nm</td>
<td>1.8</td>
</tr>
<tr>
<td>32 to 22nm</td>
<td>2</td>
</tr>
<tr>
<td>22 to 14nm</td>
<td>2.5</td>
</tr>
<tr>
<td>14 to 10nm</td>
<td>&gt;4</td>
</tr>
</tbody>
</table>

SOURCE: Bernstein
In the Past…

MOORE'S LAW

RELATIVE COST/COMPONENT

1962

1965

1970

COMPONENT PER IC

10^5

10^4

10^3

10^2

10^1

1

10

100

1000

10000

100000

POWER

PERFORMANCE

AREA-COST

PPAC

ENABLED BY

“Classic” 2D feature shrinking

+ materials engineering to improve power and performance
In the Future...

ENABLED BY

- New architectures
- New structures / 3D
- New materials
- New ways to shrink
- Advanced packaging

FOUNDATION IS MATERIALS ENGINEERING
3D NAND shows power of architecture inflections

Extended NAND cost roadmap by >10 years + better device

Speed 2x

Endurance 10x

Power efficiency 2x

NUMBER OF CRITICAL ELECTRONS IN NAND CELL
Future 2D shrink is not only limited by resolution, but also **PLACEMENT ERRORS**

State of the art A.I. chip can have up to **100B vias**

Can be addressed by self-aligned structures
MATERIALS-BASED APPROACHES CAN ELIMINATE PLACEMENT ERRORS

Example: ‘Multicolor’ = Fully self-aligned multi-material patterning
ADVANCED PACKAGING
Can Optimize System Level Performance

3x
Logic ↔ DRAM bandwidth performance

50%
Power savings per bit

System on Chip to System on Package
Integration of chiplets provides **time**, **cost** and **yield** benefits

SOURCES: Intel, GLOBALFOUNDRIES
New architectures
New structures / 3D
New materials
New ways to shrink
Advanced packaging

KEY ISSUES =
Complexity ↑
Integration challenges ↑↑
Time to market ↑↑↑

NEW PLAYBOOK NEEDED FOR
CONNECTIVITY + SPEED
"Von Neumann" mindset vs. "Neuromorphic" mindset

TODAY: Serial / compartmentalized interaction between key parts of eco-system

OPPORTUNITY: Parallel development to get powerful tools to designers faster

CONNECTIVITY TO ACCELERATE INNOVATION
A.I. – Big Data Era = the biggest opportunity of our lifetimes

UNLOCKED BY

Hardware renaissance

Materials innovation to enable new architectures, structures, ways to shrink and packaging approaches

New eco-system playbook to drive connectivity and speed