M0N0: A sub-threshold microcontroller for near-zero-power sensor applications

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Driving Applications: Near Zero Power RF and Sensor Operations (N-ZERO)

The Challenge

DARPA's N-ZERO program poses the challenge to design always-on sensors and wakeup radios with 10nW power consumption. Very interesting prototype chips are now being demonstrated that meet the extremely difficult target and provide a smart wakeup source to a microcontroller (MCU).

For system designers seeking to make use of N-ZERO sensors, there is a stark choice to be made when it comes to selecting a commercial MCU. To use an easily programmable and performant 32b MCU with leakage power which swamps the new sensor? Or to use an 8b MCU with comparable leakage power but poor active power and performance?

COTS MCU examples	SiLabs EFM32ZG108	SiLabs C8051F91x
Processor	32b ARM Cortex-M0+	8b 8051 compatible
Shutdown Power	60nW	10nW
Active Power	2.7mA @ 24MHz	3.8mA @ 24MHz
Peak Performance	21.6M 32b instructions/second (Dhrystone benchmark)	3-25M 8b instructions/second (peak, no branches)

M0N0 seeks to plug this gap, marrying ultra low leakage with 32b performance and programmability at greater active power efficiency.

What additional system functionality could this enable?

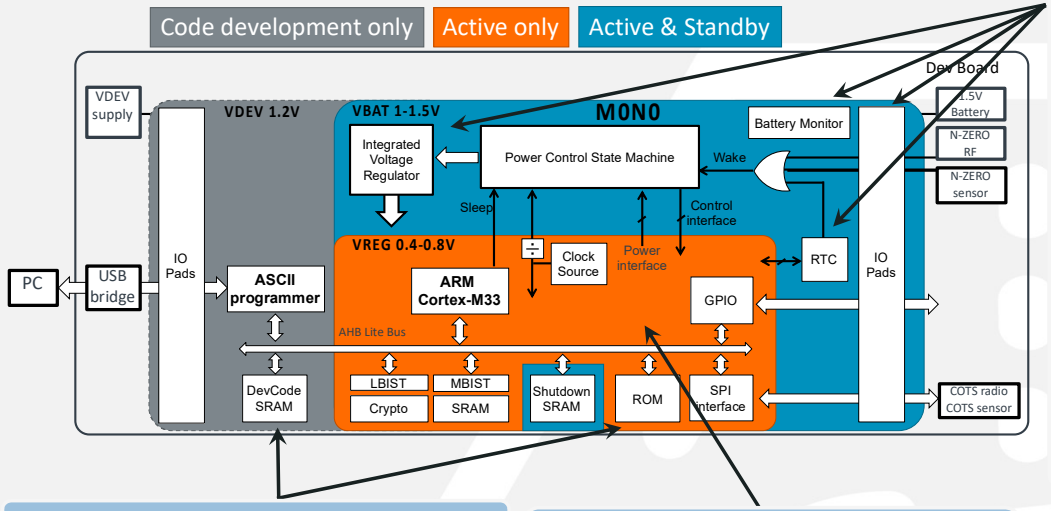
- Allow digital sensor fusion in addition to analog fusion
- Filter false alarms from 1/hour to 1/day or less, reducing radio activity and extending battery life
- Preserve some (judicious) sensor history and adapt to environment
- On real alarms, communicate historical context as well as immediate
- Provide periodic self-test to ensure node is operational

Project Outputs

The M0N0 project intends to deliver an optimized MCU with HW/SW environment enabling government contractors to develop new applications and to have new chips fabricated for government use. For application-specific feasibility studies to be conducted in parallel to the M0N0 project, we will release regularly updated data sheets describing system performance, memory capacity, etc. Some specific outputs are:

- Projected data sheets towards the final system
- Demo board and testchip implementing an example application
- Development board and infrastructure for new software development
- Chip generator to via-program ROMs with new software

The photo below shows the chip 1 test board, providing full testability of prototype circuits. Final demo and development boards are expected to be simpler.



Highly efficient integrated analog for 10nW shutdown

The 10nW shutdown power budget for the chip is very challenging and will require careful optimization or elimination of any always-on components. Once the digital sub-system is thoroughly power-gated, most of the leakage is from analog/mixed-signal components. From the start of the project, a tight budget has been set for each block.

Analog/mixed-signal block shutdown targets

- 10x IO pads on VBAT - 1nW
- Real-time clock, disabled or sub-kHz – 1nW
- Integrated voltage regulator, including VREG leakage – 3nW
- Battery monitor – 1nW

Digital block shutdown targets

- Power control state machine – 2nW
- Shutdown SRAM retaining 4KB – 2nW

Two circuits chips were designed for silicon validation of these crucial building blocks, with key results shown below.

ROM for code, RAM for development

Non-volatile memories such as embedded flash have excellent flexibility but large power due to high voltage charge pumps and complex sensing schemes. M0N0 uses ROM as it is inherently more efficient and can also be designed to scale with logic to optimally efficient sub-threshold voltages.

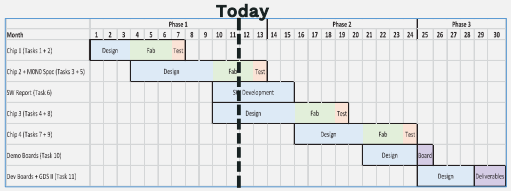
The drawback is that the code is fixed at manufacturing time. To enable development of new code, M0N0 includes a dense SRAM which can hold work-in-progress software while it is tested, debugged and verified. Once completed, a new chip layout can be generated (without the use of EDA tools), using a chip generator licensed from Arm.

Specifications (Subject to Change)

- Processor: Arm Cortex-M33 with DSP extensions (no FPU)
- Battery voltage: 1-1.5V primary alkaline
- Functional temperature range: 0-85C
- Shutdown power: 10nW at 25C (IVR disabled and 4KB retention in Shutdown SRAM)
- ROM capacity: 128kB
- RAM capacity: 16kB active + 4kB shutdown
- Shutdown RAM breakeven time: 1s for full 4kB transfer
- Interfaces: SPI with up to 3 chip selects or up to 5 GPIO
- Performance: 0.5-50MHz
- Active power: 10uW-2mW

} Under SW control – slower is more efficient

Today

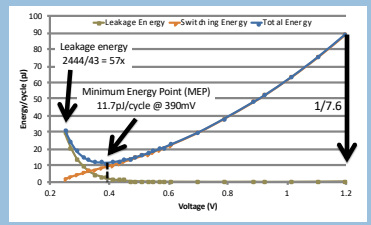


Sub-threshold operation for 10uW active power

Operating digital sub-systems below their threshold voltage has been shown in prior ARM work to increase energy efficiency by up to 10x. Once circuit challenges such as SRAM design and temperature variability are overcome, the next challenge is to deliver a range of performance/power points without undue burden to software.

M0N0 will remove the need for software to specify a regulator mode or voltage/frequency pair from a characterized lookup table – as is common for DVFS in mobile systems. The real requirement is for the hardware to deliver a guaranteed application-specific minimum performance. This can be done using our automatically scaling system clock source, as feedback to the voltage regulator. This also has the benefit of reduced regulator power in voltage comparators.

The figure below shows measured results from a first generation sub-threshold chip designed by Arm Research and published at ISSCC in 2015.



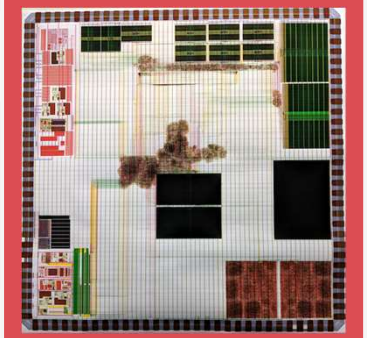
Key Results

From chip 1 (taped out November 2017)

- Achieved 50% lower leakage in new ESD clamps for equivalent protection of 2kV HBM and 400V CDM
- ROMs operating correctly below 300mV
- AMS blocks such as references functioning correctly, will be included in battery monitor and voltage regulator

To be improved further on chip 2 (May 2018)

- ROM read speed
- Shutdown SRAM leakage



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