



Sub-10µm Pitch 3D Integration Technology for Adaptive Focal Plane Array Imagers

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Micros Components

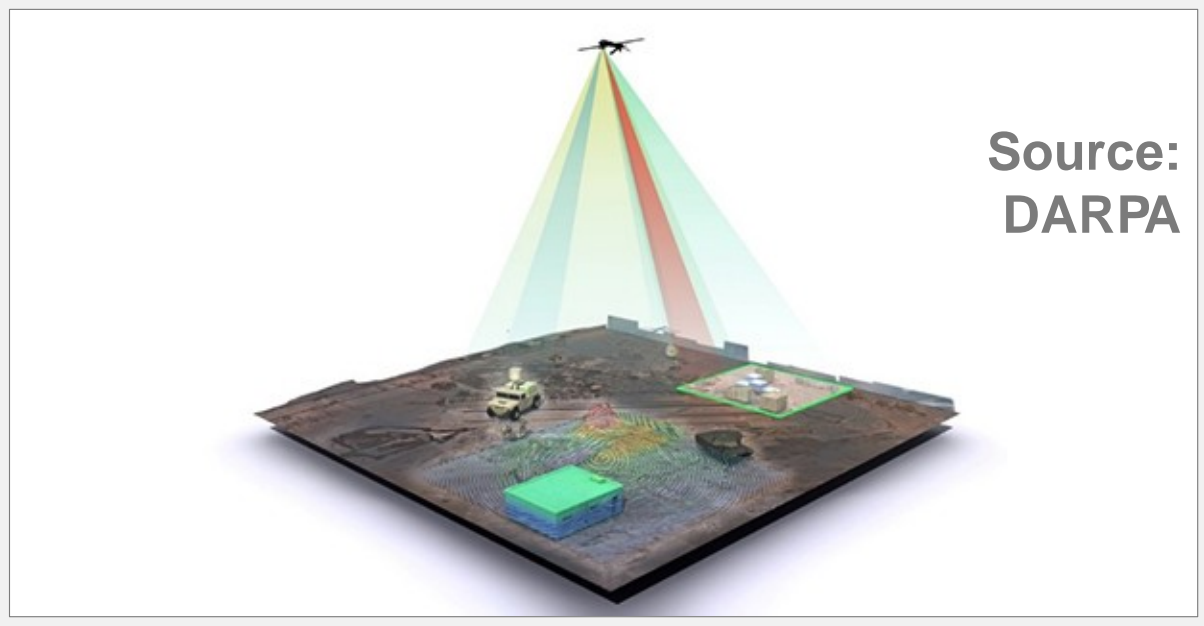


Driving Applications: Reconfigurable Imaging (Relmagine)

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

Relmagine Program Focus:

Smart, reconfigurable imagers which can adapt to collect the ideal type of sensor data for a given situation.



Source: DARPA

3D-Enabled Smart Pixels:

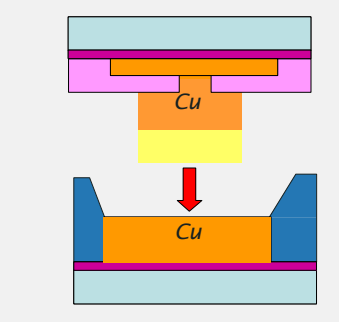
- Advanced 2-layer 3D readout IC (ROIC): Analog layer with integrated digital processing at pixel level

Unique 3D Integration Requirements:

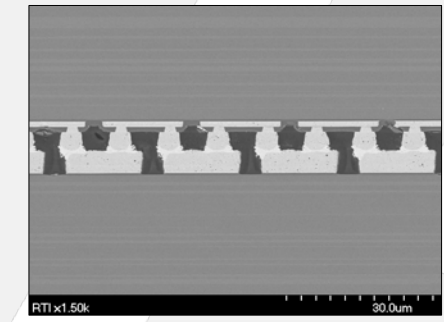
- Fine pitch 3D** interconnects:
 - 12 µm pixel size
 - Sub-10 µm pitch bumps & TSVs
- High I/O:** >1M pixel interconnects
- Large die:** up to 20 mm / side
- Advanced CMOS:** to 14 nm node
- Vacuum package** compatibility
- Temperature extremes:**
 - Cryo (cooled) operation
 - Thermal gradients in stack (due to ROIC power dissipation)
- 3-layer, heterogeneous integration**
 - Digital ROIC, Analog ROIC, detector layer

3D approach: Cu/Sn SLID bonding

- Plated Cu/Sn & Cu micro-bumps
- Thermocompression (TC) bonding
- ~1 µm alignment accuracy
- Solid-liquid interdiffusion (SLID), Cu₃Sn intermetallic bond interface
- High-strength, stable to >600°C

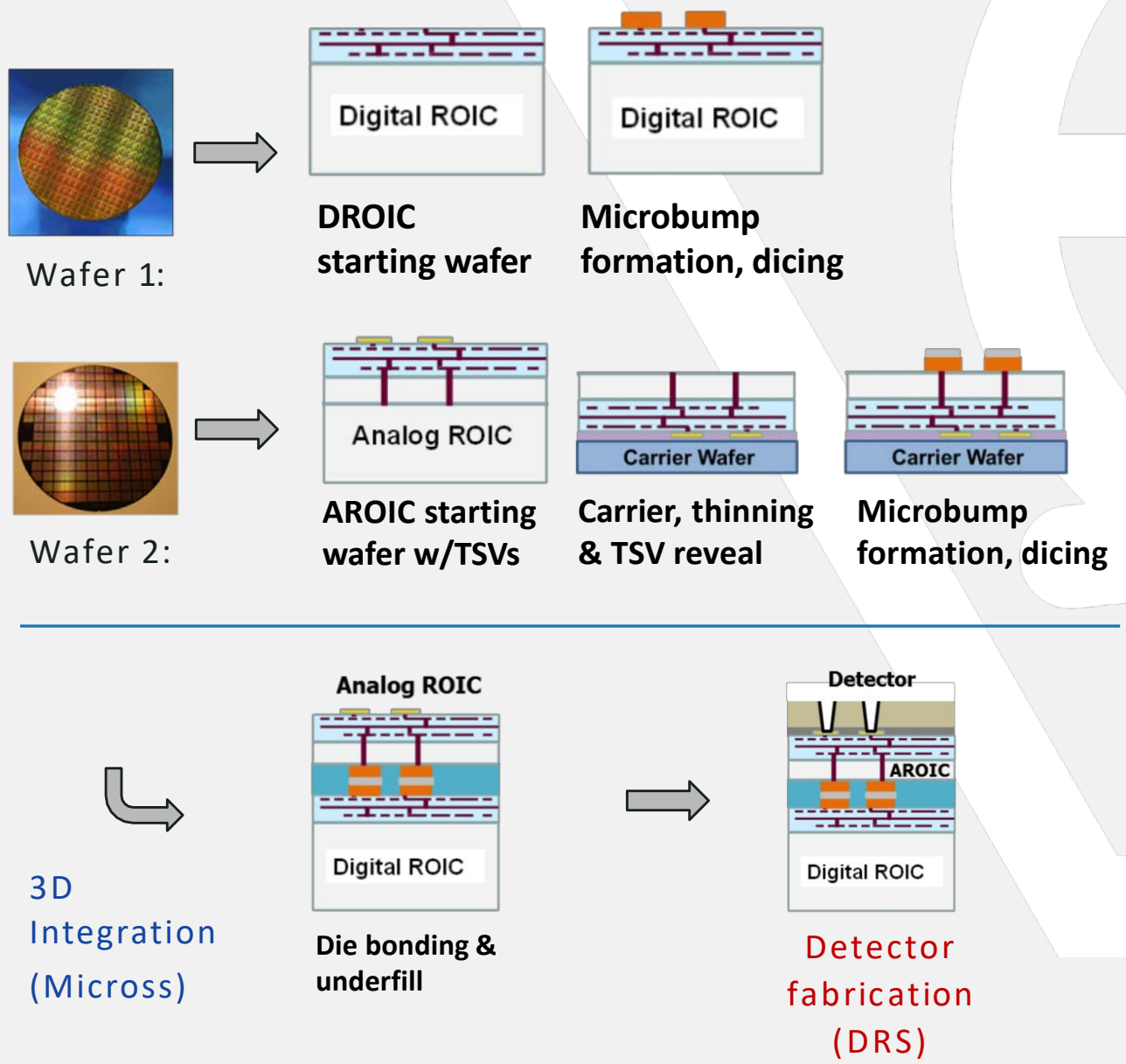


Cu/Sn-Cu Bonding Concept Diagram

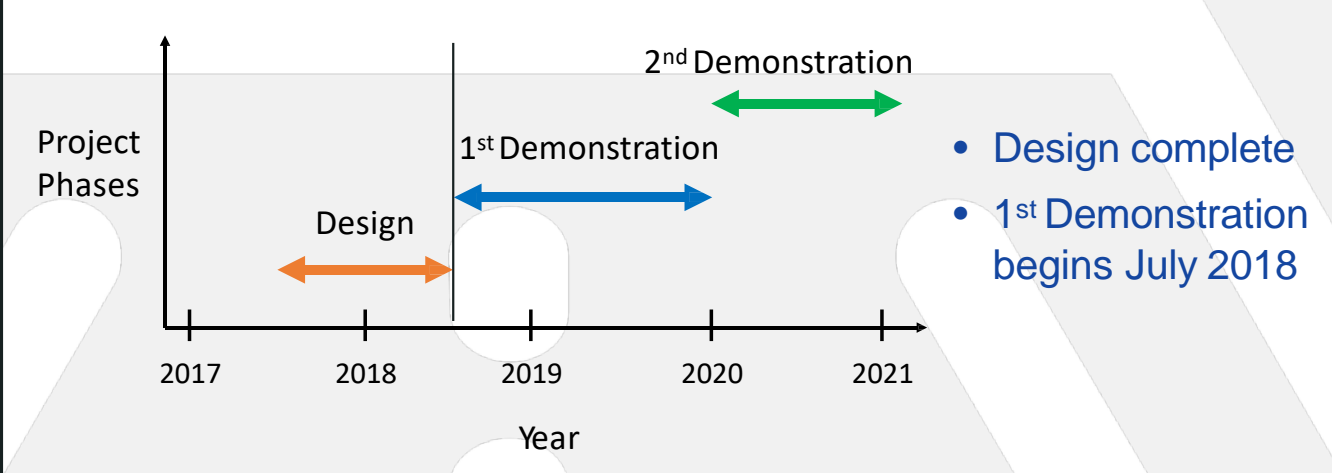


10 µm pitch Cu/Sn-Cu SLID bonds (daisy chains)

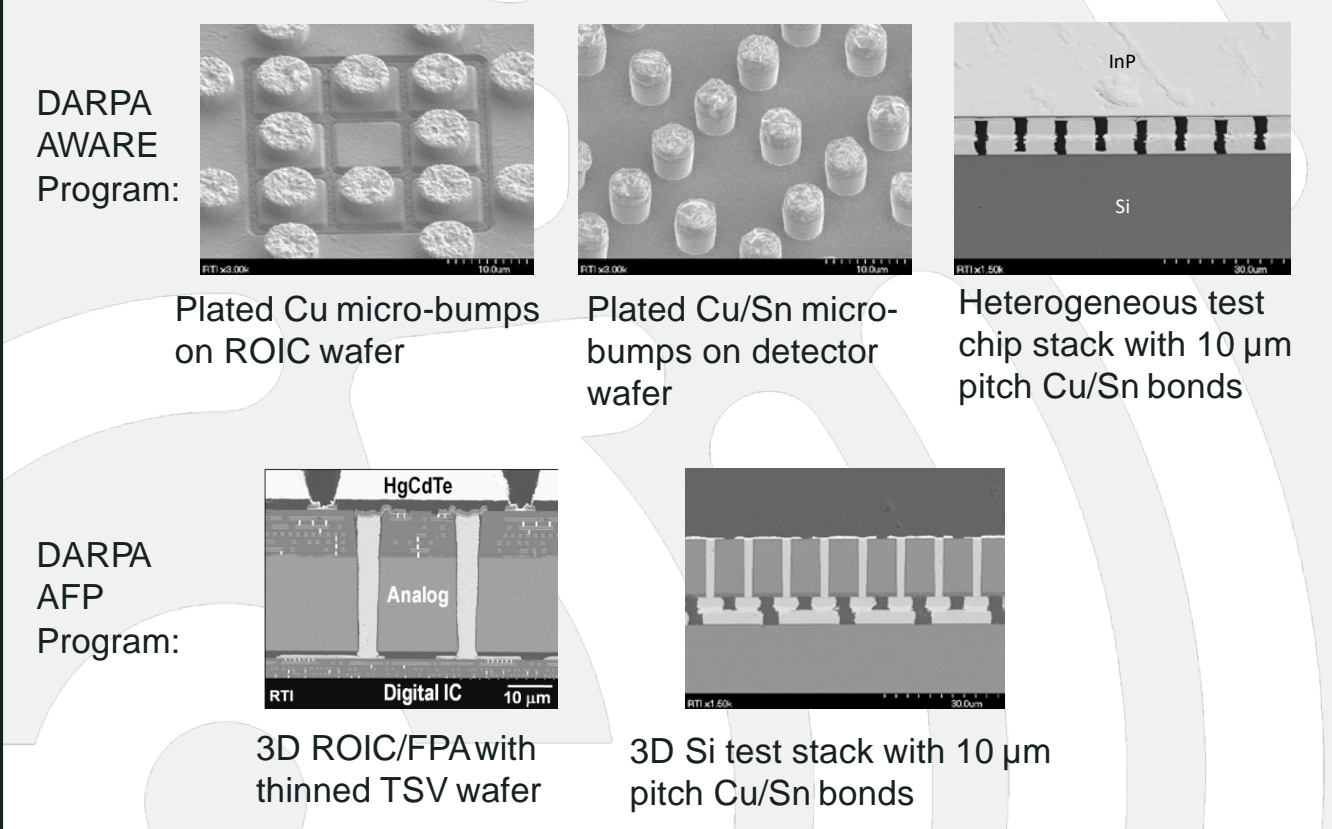
3D Integration Process flow:



Program Timeline / Status:

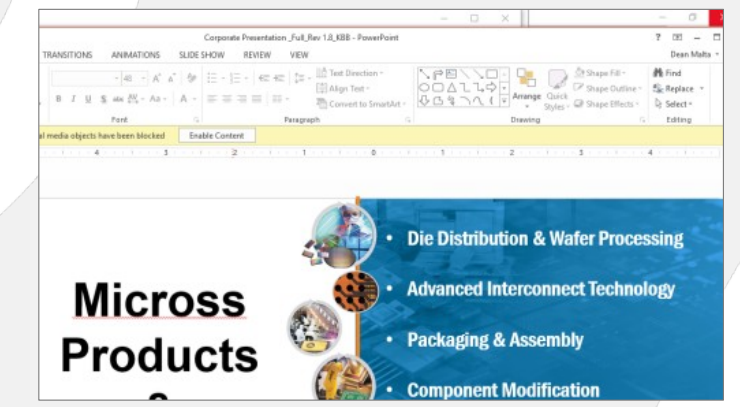


Prior Related Demonstrations:



Micros Capabilities:

Advanced Packaging & High-Rel electronic solutions for aerospace & defense, medical, and industrial markets



Micros cleanroom facility in Research Triangle Park, NC

- Micros Advanced Interconnect Technology- NC, USA**
- Wafer-level Packaging
 - Through Silicon Vias
 - 3D & Heterogeneous Integration