Development Framework for Next Generation High-Performance Processors

Domain-Focused Advanced Software-Reconfigurable Heterogeneous SoC (DASH – SoC)

Daniel Bliss & et al.

Arizona State Univ., Arm, Carnegie Mellon Univ., EpiSys Sciences, General Dynamics, Univ. of Arizona, & Univ. of Michigan

Architectures Thrust: Domain-Specific System on Chip (DSSoC)

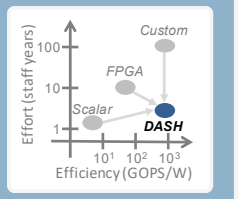
DASH Project Statement

The DASH-SoC team drives a revolution in flexible DSSoC computational systems. To support unmanned aerial, small robotic or leave-behind, and universal soldier systems, the Department of Defense (DoD) needs reduced size, weight, and power (SWaP). To support multifunction systems (communications, sensing, positioning, SIGINT, EW), the DoD requires dramatically increased processing flexibility. We break the fundamental trade that custom SoCs are required for power efficiency, but scalar processors are required for ease of implementation.

Goal

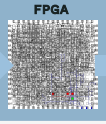
- Develop tools to design and use heterogenous processor for a range of signal processing applications
- Dramatically improve power efficiency
- Dramatically reduce engineering cost during SoC design and implementation

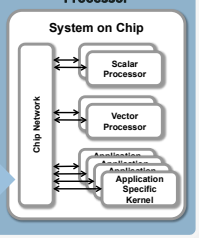
DASH Implications



Evolution of Processors

- Transition from current scalar and FPGA approaches to heterogenous processor
- Improve computational performance
- Introduce new implementation issues
- Circumvent rigid custom SoC limitations

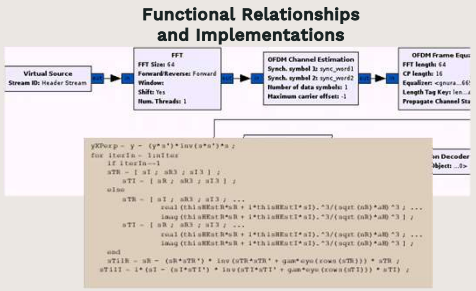


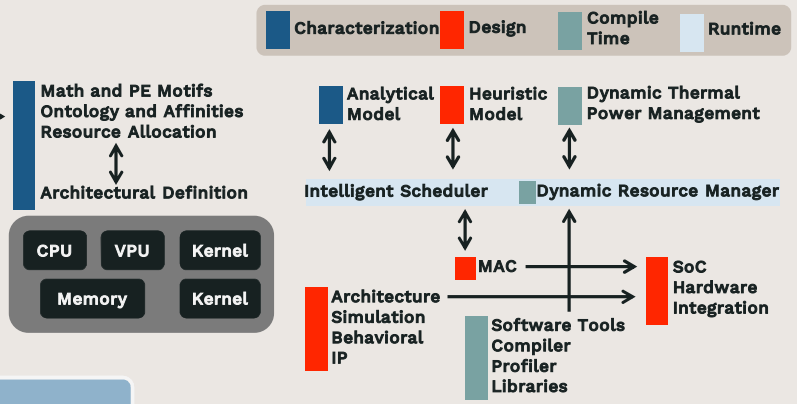


Impact

- Enable wide range of new applications that require many TOP/s such as:
  - Advanced SIGINT, modern communications → ~ 1000 GOP/s
  - Bistatic SAR, match filter → ~ 1000 GOP/s
  - Advanced video processing, 8k video image alignment → ~ 1000 GOP/s
- Support new and evolving types of DoD users (human and non-human)
- Quickly address new problems as they arise

Innovation Overview

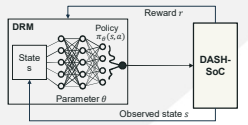




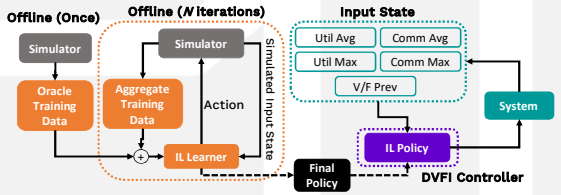
Innovation

- Develop novel ontological inference of the design-time allocation of processor elements (PEs), their parameters, and their placement given multiple simultaneously executing applications
- Develop innovative run-time resource management that learns to automatically and intelligently schedules multiple applications
- Develop a full suite of design-time, compile-time, and run-time software capabilities to enable efficient implementation with reduced expert intervention
- Develop a standard heterogeneous SoC interface and energy-efficient interconnection network to facilitate hardware integration of heterogeneous processing elements
- Design, fabricate, and validate novel DASH-SoC that dramatically reduces the algorithm implementation effort by integrating novel capabilities
- Create an explicit transition path by employing DASH development tools and SoC to implement multiple target applications

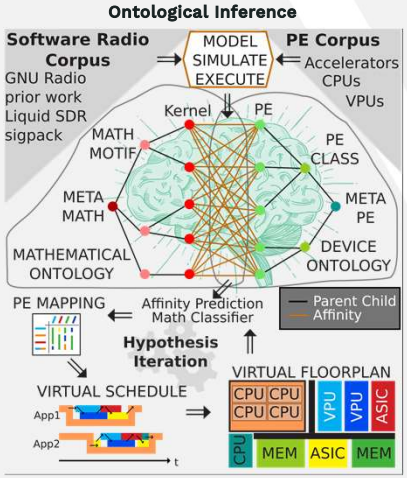
Intelligent Scheduler



Mixed Offline and Online Learning for Developing Intelligent Scheduling – The intelligent scheduler (IS) consists off a deep-reinforcement learning (DRL) scheduler and dynamic voltage-frequency controller. The IS monitors the incoming tasks and states of the processing elements (PEs). It assigns the tasks to the available PEs and controls the voltage-frequency islands to meet the performance targets under power and temperature constraints.

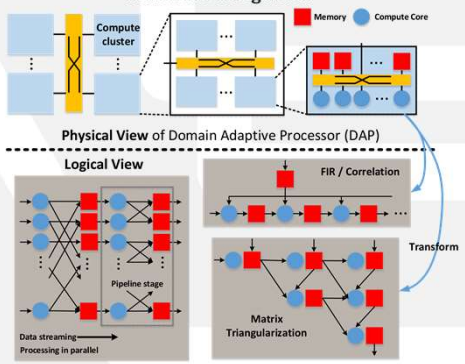


Ontological Inference



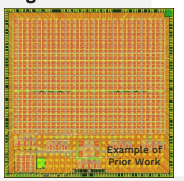
Intelligently Translate Corpus of System Specifications to Identify Processing Elements and Connections – Device and mathematical knowledge are statistically derived from a body of applications and hardware designs, resulting in taxonomies and an understanding of math's affinity for a PE. A hypothetical SoC design and schedule are proposed using a classification of the program's components and a prediction of their performance on a specific device.

Hardware Integration



Notional Representations of DASH Hardware Integration – The new Domain Adaptive Processor (DAP) are heterogeneous PEs are integrated within the DASH SoC. DAP is run-time transformable from the physical view (top) to various logical configurations (bottom) supporting dynamic compute / memory resource allocation and various streaming data movement patterns. Hierarchical crossbars in a DAP are fast reconfigurable to realize various domain-specific systolic data pipelines.

Design and Fabrication



Design and Fabricate Example DASH Chip – The team has significant expertise in designing and fabricating large SoCs, including Celerity shown in this figure with 511 RISC-V cores in 25 mm2 area.

Transition Demonstration

Over-the-Air DASH-SoC Software-Defined Radio Experiments – A development board using the DASH-SoC is developed and used to demonstrate implementation and performance advances. This also provides an initial path to transition

Prof. Daniel W. Bliss[1] – PI

Dr. Rob Aitken[2]
Prof. Ali Akoglu[6]
Mr. Stuart Biles[2]
Prof. David Blaauw[7]
Mr. Lee Eisen[2]
Mr. Tom Genduso[2]
Dr. John Goodenough[2]
Prof. John Brunhaver[1]
Prof. Chaitali Chakrabarti[3]
Prof. Ronald Dreslinski[7]
Mr. John Fielden[5]
Dr. Matt Horsnell[2]
Prof. Hun-Seok Kim[7]
Mr. Allen E. Lacey[5]
Prof. Radu Marculescu[3]
Prof. Trevor Mudge[7]
Prof. Umit Y. Ogras[1]
Dr. Nadeesha Ranasinghe[4]
Dr. Bo Ryu[4]
Mr. Donald L. Westhafer[5]

[1]Arizona State University
[2]Arm, Ltd.
[3]Carnegie Mellon University
[4]EpiSys Sciences, Inc.
[5]General Dynamics Mission Systems
[6]University of Arizona
[7]University of Michigan

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.
Distribution Statement A – Approved for Public Release, Distribution Unlimited

THE ELECTRONICS RESURGENCE INITIATIVE