Future Graph Analytics

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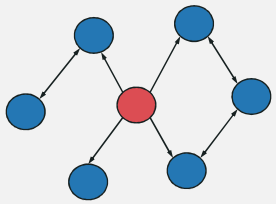
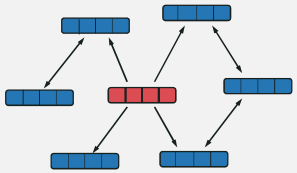
Architectures Thrust: Hierarchical Identify Verify Exploit (HIVE)

Problem Statement

- Graph workloads are sparse and irregular, meaning the computations and data accesses are unknown until runtime. Today's architectures are inefficient in this space.



Webpage ranking, community detection, clustering

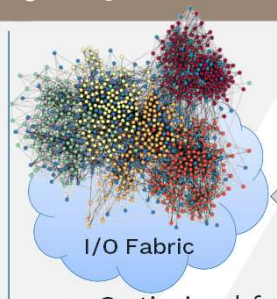


Anomaly detection, Cybersecurity, Molecular similarity

Proposed Solution

- Develop a Graph Analytics (GA) processor that is orders of magnitude more power efficient than existing systems

Intel's Approach

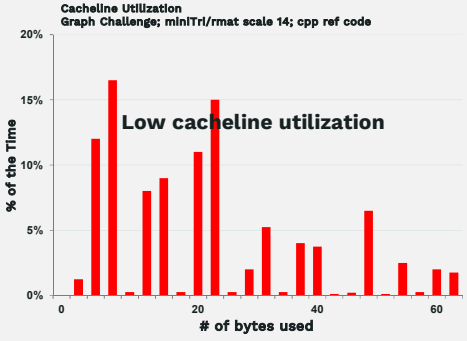


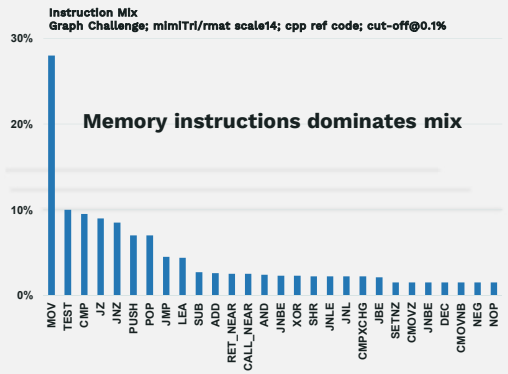
- Optimized for Energy Efficiency
  - Memory Accesses, Network Messages
- Optimized for Performance
  - Scalable Topologies
  - Memory Hierarchy Topology
- Highly Scalable Design with Balanced Memory & Compute
- Open Primitives, Software, and APIs that support different programing paradigms
- Hardware/Software co-design between Industry, Sponsored Research, and Academia

Traditional Approaches

Current Architecture Solutions Rely On

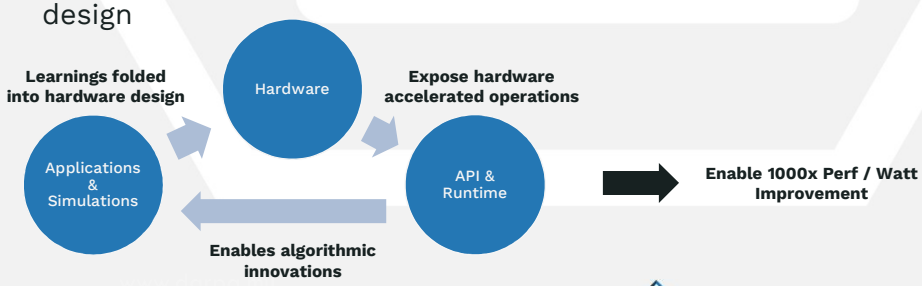
- Low capacity-to-bandwidth ratio for existing and foreseeable memory architectures
- Scalability by cache-coherent systems and coarse-grained cache-line accesses
- Software layers and network software stacks





Successful Program Enables

- Move AI from Classification to Decision Making
  - Relationships between objects and reasoning
- Real-time analytics of Big Data at the network edge by solving ~1T edge problems in seconds: O(100)TB datasets
- Facilitate breakthrough algorithm R&D
  - Removes traditional system architecture bottlenecks
  - 1,000x Perf/W Improvement
- Scalable solutions for many types of pro
- Virtuous cycle of Hardware, Runtime and Application co-design



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