OpenROAD: Foundations and Realization of Open, Accessible Design

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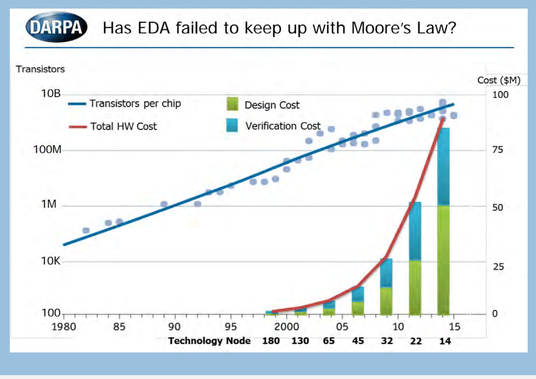
Designs Thrust: Intelligent Design of Electronic Assets (IDEA)

The Design Challenge

- Enormous barriers to HW design in advanced technologies: Cost, Expertise, Unpredictability

Background: How is it Done Today?

- HW design tools have evolved into complex "Swiss army knives"
- Chaos when tools forced to "try hard"



Innovation: New in Our Approach

24 hours, no humans – no PPA loss

- Extreme partitioning
- Parallel optimization
- Machine Learning of complex tools/flows
- Restricted layout

Design Complexity

Impact: If Successful …

- Create new "Base Technologies" that enable 24-hour, autonomous design
  - Extreme partitioning (bite-sized problems)
  - Parallel search, optimization
  - Machine learning: models of tools, designs
- Change paradigm for tools + design methods: autonomy first
- Bring down barriers → democratize HW design

Our Goal

- 24-hour, No-Human-In-Loop layout design for SOC, Package and PCB with no Power-Performance-Area (PPA) loss
- Tapeout-capable tools in source code form, with permissive licensing → seed future "Linux of EDA"

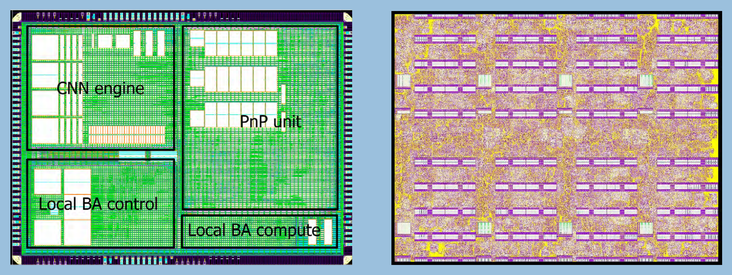
Foundations of Approach

- No humans: tools must adapt and self-tune, must never get stuck unexpectedly
- 24 hours: extreme partitioning of problems + parallel search on cloud + machine learning for predictability
- Mantra: Correctness and safety by construction
- Mantra: Embrace freedom from choice

Technical Challenges

- Data: small and expensive!
- Humans: in the loop for good reasons!
- Fundamental tradeoffs: analysis cost vs. accuracy, optimization effort vs. quality
- Activation energies: new sharing mindsets, open-source ecosystem

Impact on Design Cost



- Embedded vision chips (28/16nm) from Michigan Internal Design Advisors team
- Layout @UM: 10+ weeks, significant resource
- OpenROAD and IDEA goal: 1 day, no humans (!)

Swinging for the Fences!

- Need critical mass and critical quality
- We take on 11 of 13 IDEA TA-1 subtasks

Common Infrastructure	~~Databases / Processing~~	
	✓ Cloud Infrastructure	BROWN
	✓ Timing Analysis	UCSD
	✓ Parasitic Extraction	U of Minnesota
	✓ Readers + Writers	UD
	✓ Power and SI Analysis	U of Minnesota
Layout Generators	✓ Logic Synthesis	BROWN
	✓ Floorplanning	ILLINOIS
	✓ Placement	UD, UCSD
	✓ Clock Tree Synthesis	UCSD
	✓ Detailed Routing	UD, ILLINOIS
	✓ Layout Finishing	UD, UCSD
Design	~~SoC Design Advisors~~	

- Internal Design team from Michigan: ~70 Ph.D. / 50 M.S. graduates + 15+ new SOC designs/year
- Tools team from UCSD, Illinois, Minnesota, UT-Dallas, Brown: ~150 Ph.D. / 80 M.S. graduates + many tools, engines "on the shelf"
- Qualcomm: HW design expertise
- Arm: system, IP expertise
- And more:
  - Open-sourced commercial timing engine
  - Donated commercial source code base
  - Industry advisors, technical contributors
  - Worldwide outreach and engagement

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