Fully-Autonomous SoC Synthesis using Customizable Cell-Based Synthesizable Analog Circuits

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Designs Thrust: Intelligent Design of Electronic Assets (IDEA)

The proposed research will develop a fully-autonomous SoC synthesis tool using customizable cell-based synthesizable analog circuits for IDEA Technical Area II. **Our approach leverages a differentiating technology to synthesize "correct-by-construction" Verilog descriptions for both analog and digital circuits to enable a portable, single pass implementation flow.**

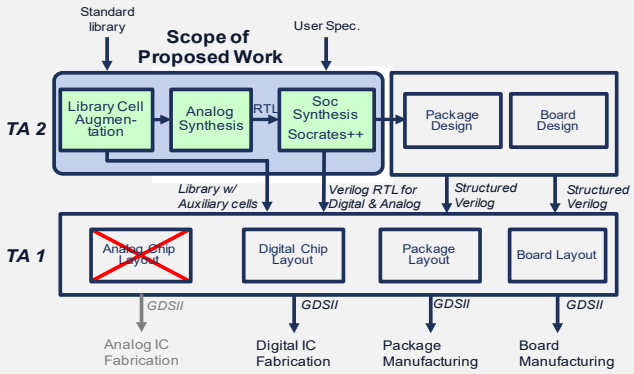


Figure 1. Scope of the proposed work, showing its fit into the BAA technical areas.

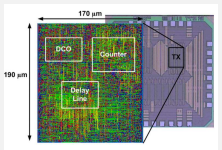
Background
- A typical SoC has many analog components, which have labor intense design processes
- Design in advanced nodes (<28nm) is getting harder
- An SoC synthesis tool realizes analog circuit automation is desired

Innovation
- A single SoC synthesis tool that produces Verilog descriptions for both analog and digital components
- This RTL is passed only to the digital chip layout tool for APR

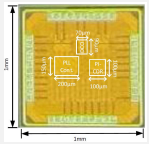
Impact
This has the advantage of creating a much simpler, unified back-end design flow and improving design portability to advanced technology nodes

Previous Work & Design Goal

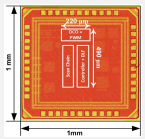
Our group has been working on synthesizable circuits, such as: ADPLL, TDC, IR UWB Transmitters, DAC, and Serial Links. The following are selected previous synthesized works, and our goal of research



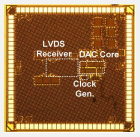
Synthesized UWB TX



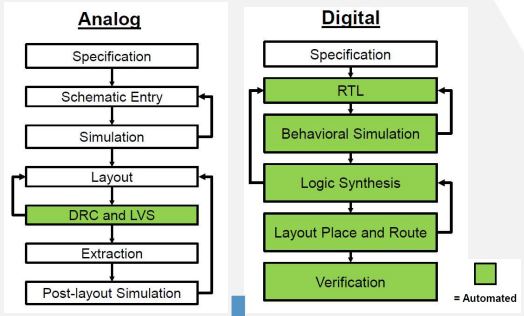
Synthesized Serial Link



Synthesized ADPLL



Synthesized DAC



Propose a fully-autonomous SoC synthesis tool to replace the time consuming analog design process developed from the previous digital design flow for advanced Finfet technology

Proposed Research

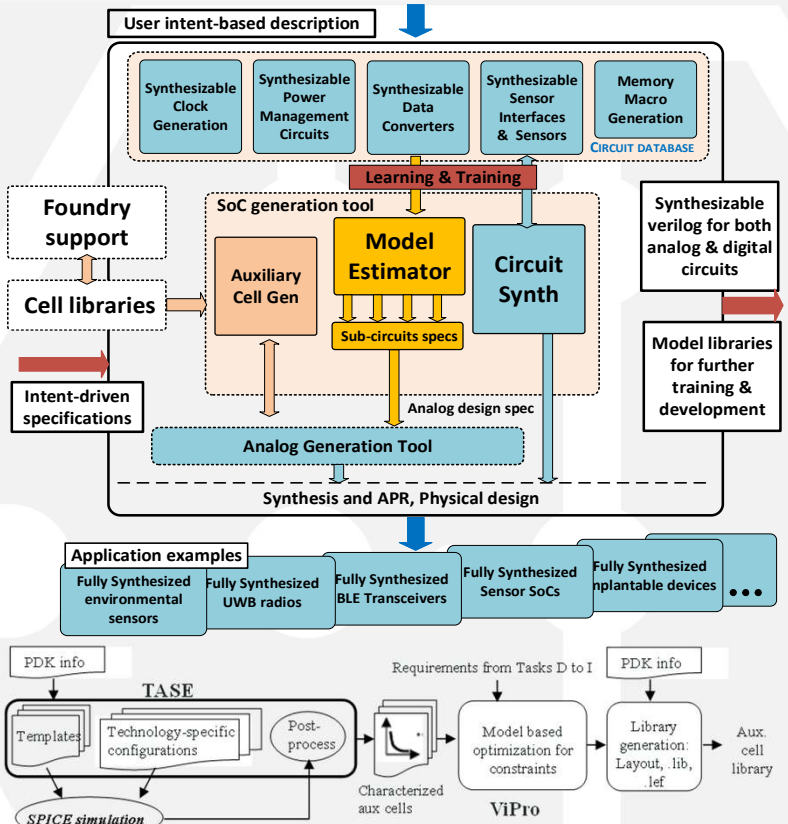


Figure 2. Block diagram of proposed research showing the interactions among tasks and the proposed auxiliary cell generation flow

Task and Milestones

IDEA TA-2 Sub-task	Proposal Tasks
TA-2, Sub-task 1: Open parts database	Extending IP-XACT, Synthesizable Circuit Blocks
TA-2, Sub-task 2: System generator	Extending Socrates Infrastructure, Correct-by-Construction Design
TA-2, Sub-task 2: Reference design generator	• Synthesizable Clock Generation • Synthesizable Power Management • Synthesizable Data Conversion • Synthesizable Sensor Interfaces • Synthesizable Thermal Sensors • Memory Macro Generation • Auxiliary Cell Generation
TA-2, Sub-task 3: Circuit optimizer	Circuit Block optimization

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