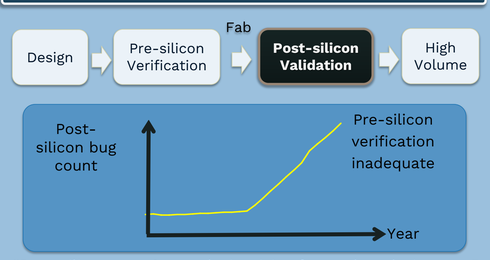
QED Bug Detection and Localization

Subhasish Mitra (Stanford)

Designs Thrust Posh Open Source Hardware (POSH)

Post-Silicon Validation Critical

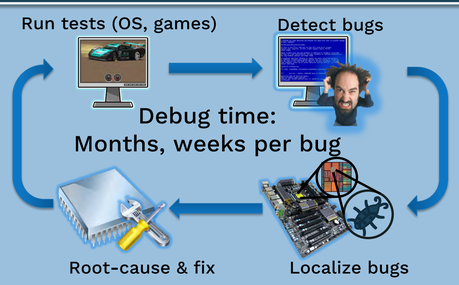


"Post-silicon cost & complexity rising faster than design cost"

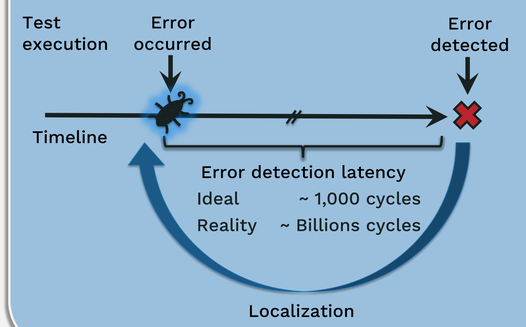
– S. Yerramilli, V.P., Intel

Source: Intel

Localization Dominates Cost



Long Error Detection Latency Challenge



Quick Error Detection

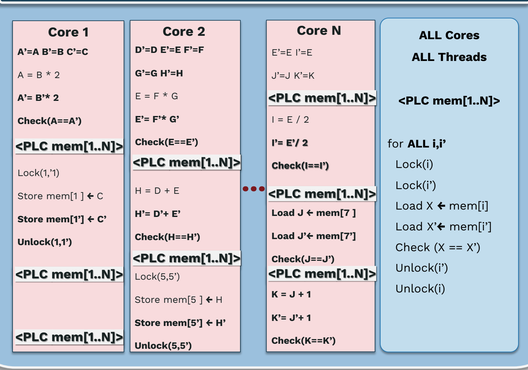
- Error detection latency: guaranteed short
- Coverage: improved
- Software & hardware approaches

Quick Error Detection Highlights

- Structured and Effective
  - 10^9X quicker detection, 4X coverage
- Automatically localize bugs
- No failure reproduction, no simulation
- Broadly applicable:

  Cores, uncore, power management, logic & electrical, accelerators

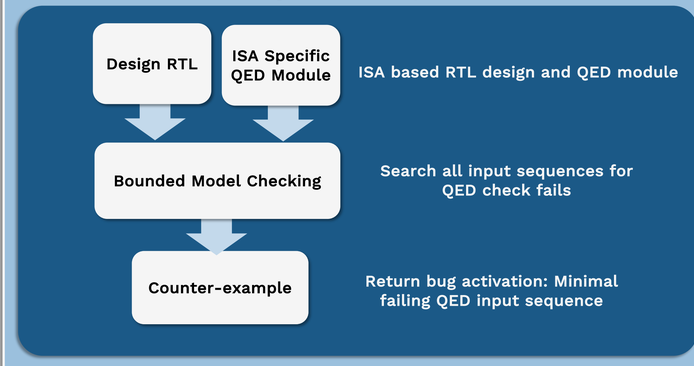
QED Transformation Example



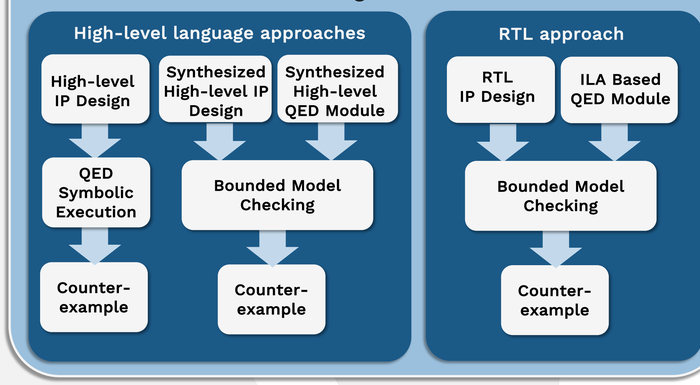
Symbolic QED and A-QED

- Fully automated logic bug localization
- Pre-silicon and post-silicon bugs
- Formal verification with no manual properties
- Implementation only dependent on ISA
- Scalable: billion-transistor SoCs
- Verify any IP block (accelerators, uncore, etc.)
- High-level language and RTL descriptions

Symbolic QED

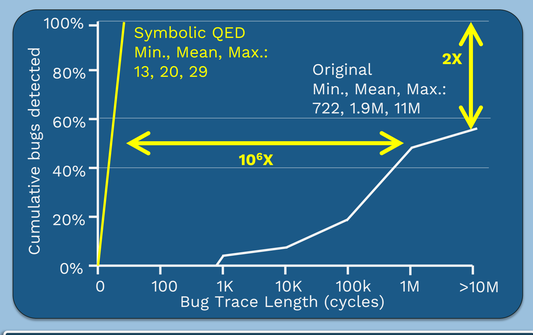


A-QED



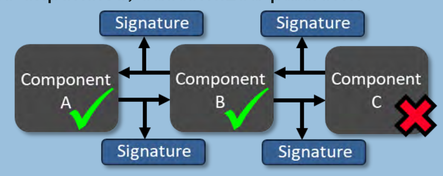
Symbolic QED Results

Traditional debug	Automatic S-QED
Weeks to months	20 mins. to 7 hours
Long bug traces	3- to 22-cycle bug traces



E-QED

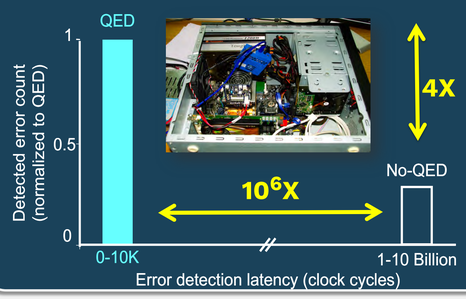
- QED enables automatic electrical bug localization
- Targets bugs at all system levels
- No expensive, customized platform



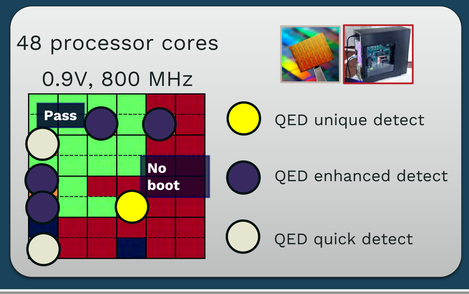
Bug localized by formal analysis of signatures

E-QED Results (min, average, max)	
Buggy design module	Uniquely identified: 100%
Flip-flop Candidates (Out of ~1 million)	(5, 18, 26) flip-flops
Area Overhead	2.5% or less
Debug Effort	Automatic
Runtime	(7, 8.7, 12) hours

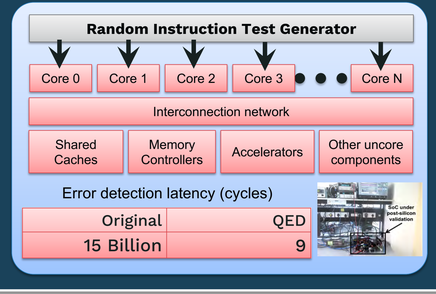
Electrical Bugs



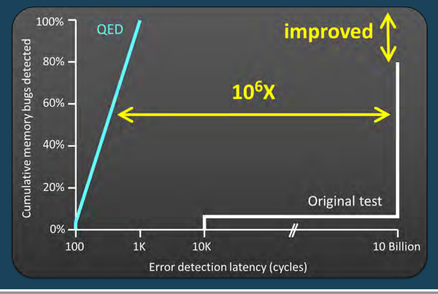
Intel® 48-Core SCC



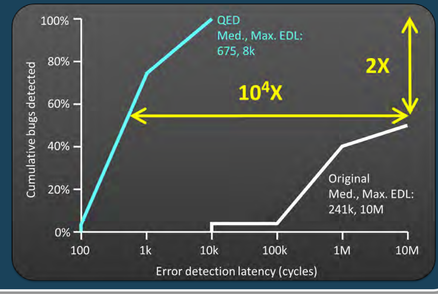
Freescale SoC Logic Bug



8-Core Industrial Test



Difficult Logic Bugs



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