RTL-to-GDS Tools and Methodologies for Sequential Integration Monolithic 3D ICs

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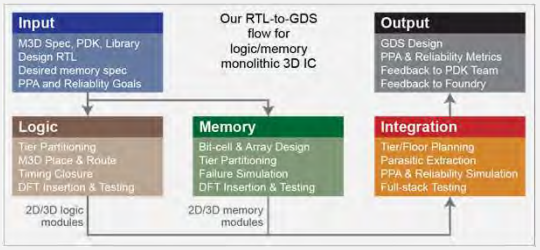
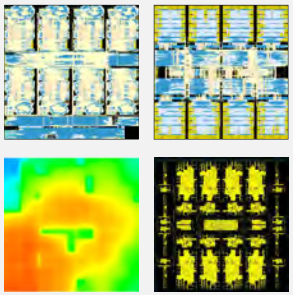
Materials & Integration Thrust: Three Dimensional Monolithic System on a Chip (3DSoC)

1. Innovative Claims



A. Comprehensive M3D RTL-to-GDS flow



B. Commercial-grade designs/simulations

tool V1 (phase 1, 18mo)
offer fundamental features
MIT/Stanford Team (DEC1)
MPW participants

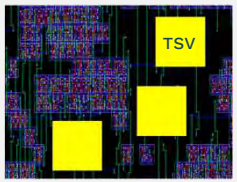
tool V2 (phase 2, 12mo)
offer advanced features
MIT/Stanford Team (DEC2 & 3)
DoD designers

tool V3 (phase 3, 12mo)
tool upgrades
DoD designers
commercial vendors

C. Tool release plans

2. Monolithic 3D IC

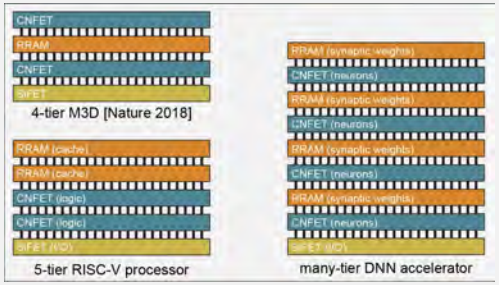
MIV (monolithic inter-tier via) offers ultra-dense 3D interconnects



TSV width = 4um

MIV width = 100nm

Support heterogeneous integration of multiple nano-technologies



3. Tool Development and Integration Plans

Our tools work with commercial 2D IC tools
- We enhance them using scripts and binaries

tool	purpose
Synopsys SiliconSmart	characterize cell delay & power
Cadence Virtuoso	draw cells
Mentor Calibre	cell LVS, DRC, and extraction
Cadence Techgen	interconnect parasitic LUT
Cadence Abstract	cell & interconnect macros
Synopsys Design Compiler	logic synthesis
Cadence Innovus	physical design
Synopsys PrimeTime	timing and power calculation
Mentor ModelSim	functional verification
ANSYS FLUENT	thermal calculation
Cadence Voltus	Power rail analysis
Mentor Calibre 3DSTACK	3D IC LVS & DRC
Synopsys TetraMAX	test vector generation

Commercial 2D IC tools we integrate

Tool	purpose
post partitioning optimizer	closes timing after tier split
M3D logic partitioner	splits logic into tiers
MIV placer	places MIVs
M3D placer	3D places gates, macros, MIVs
M3D PDN optimizer	optimizes given PDN for IR-drop
M3D clock router	builds M3D clock tree
M3D memory partitioner	splits memory into tiers
M3D memory analyzer	analyzes memory failure
M3D parasitic extractor	extracts new parasitics in M3D
M3D thermal analyzer	builds M3D thermal maps
M3D IR-drop analyzer	builds M3D IR-drop maps
M3D DFT inserter	inserts DFT modules/tiers in M3D
M3D test generator	generates test vectors for M3D

Our new tools that work with commercial tools

4. Our Tasks

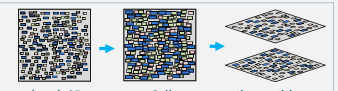
We have 18 tasks grouped into 5 themes

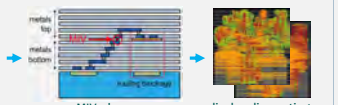
		description	ph
Logic (LIM)	T1	S2D enhancement	1
	T2	logic partitioner	1
	T3	advanced 3D placer	2
	T4	advanced PDN/CDN router	2
Memory (MUK)	T5	cell/macro design	1
	T6	memory partitioner	2
	T7	failure analyzer	1 & 2
Integration (LIM)	T8	parasitic extractor	2
	T9	thermal optimizer	1
	T10	IR-drop optimizer	1

		description	ph
DFT (CHAK)	T11	DFT inserter	1 & 2
	T12	test generator	1
	T13	MIV BIST	2
DFM (LIM)	T14	device/ckt co-design	2
	T15	int-cnt/ckt co-design	2
Release (all)	T16	V1 release	1
	T17	V2 release	2
	T18	V3 release	3
Tool upgrade	constantly		

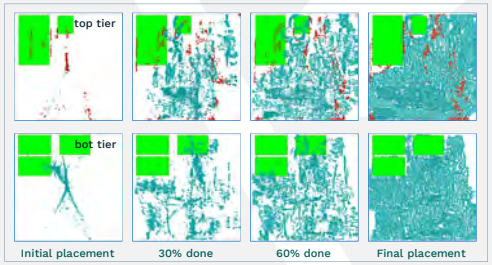
5. Logic Tasks

Two ways to obtain 3D placement



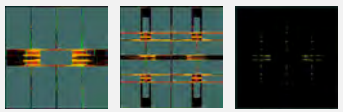


converting 2D placement to 3D



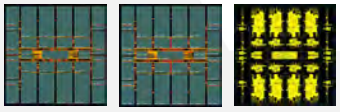
true 3D placement

Two ways to partition 2D designs



cache/core split
4,205 MIVs, 6 metals
(95.2m, 5.61W, 870MHz, 59°C, 72mV)

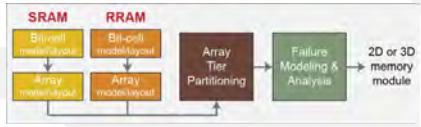
vs.



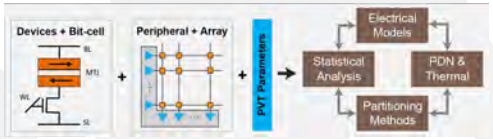
cache/core folding
838,360 MIVs, 5 metals
(76.6m, 5.03W, 870MHz, 54°C, 63mV)

6. Memory Tasks

Our plans to produce 2D and 3D memory modules

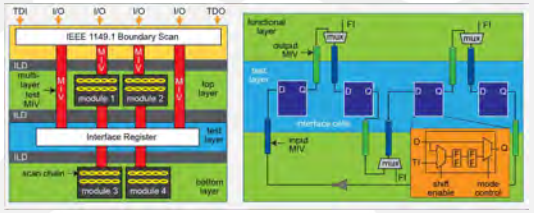


Our reliability analyzer considers statistical variations



7. Design-for-Test Tasks

We utilize a dedicated tier for M3D testing

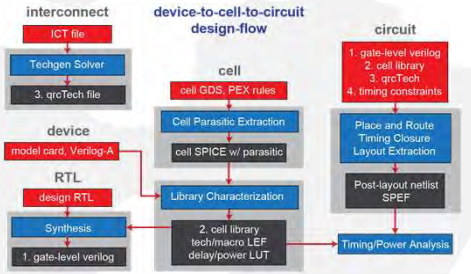


M3D test architecture

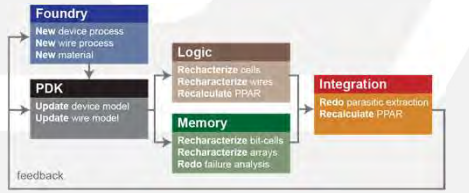
MIV BIST engine

8. Interface with Manufacturing Team

We interface via PDK and cell library



Our task for device/circuit co-design



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