



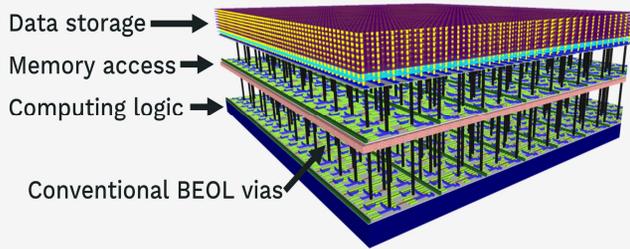
Transforming Ideas to Reality

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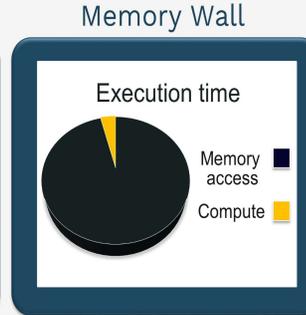
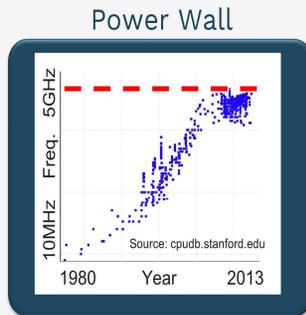
Materials & Integration Thrust : Three Dimensional Monolithic System on a Chip (3DSoC)

3DSOC: OUR APPROACH

- Monolithic 3D Integration
 - *Fine-grained integration: logic + memory*



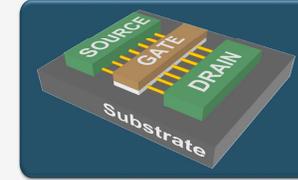
MAJOR CHALLENGES



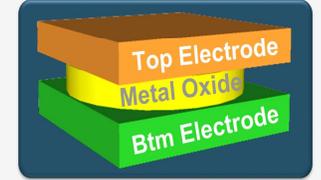
ENABLING TECHNOLOGIES

- Requires low temperature fabrication
 - *Challenging with conventional silicon CMOS*

Carbon Nanotube FETs (CNFETs)

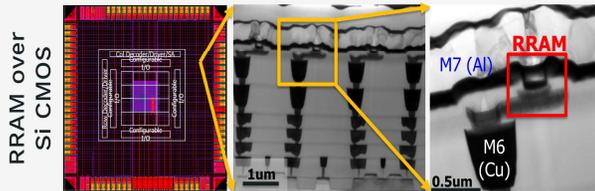


Resistive RAM (RRAM)



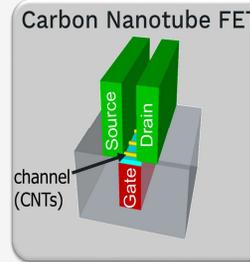
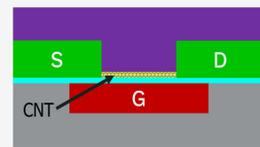
RRAM TECHNOLOGY

- Dense on-chip non-volatile memory
 - *Simple*
 - *BEOL compatible*
 - *Path to 3D RRAM*

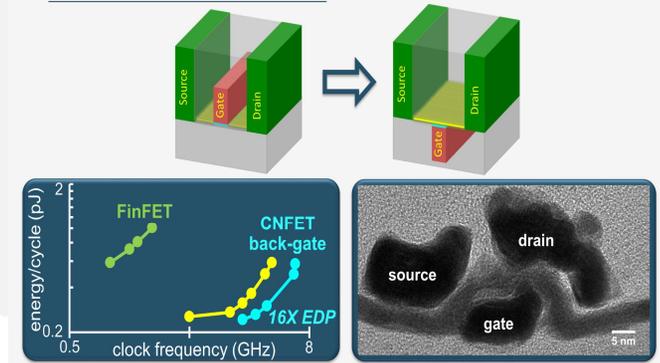


CNFET TECHNOLOGY

- 90 nm technology node
 - *Relaxes technology requirements*
 - *BEOL compatible*
 - *Fully complementary*



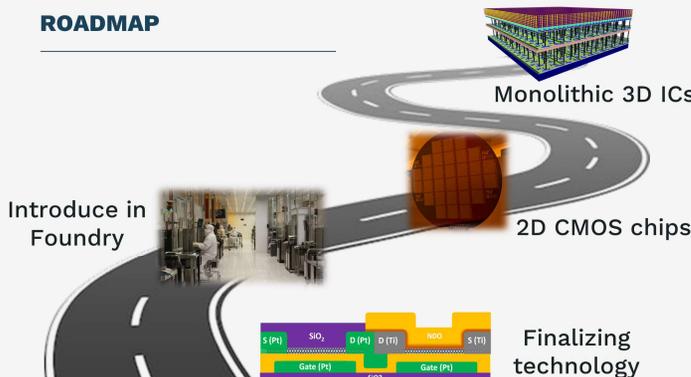
CNFET TECHNOLOGY



CNFETs: RECENT PROGRESS

materials	processing	design	manufacturing
Si-compatible; >99.99% purity	Robust doping; CNFET CMOS	Immune to metallic CNTs	Commercial facilities

ROADMAP



TEAM

 • CNFETs (optimize, transfer, PDK) • monolithic 3D fabrication • Program + system integration	 • stand-up CNFET, RRAM modules • demo monolithic 3D ICs • develop MPW offering	 • RRAM (optimize, transfer, PDK) • monolithic 3D system design • evaluation (benchmarking)	 • improving CNT material • high-volume CNT production
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