



Heterogeneous Integration Enables Next Generation Systems

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Materials & Integration: Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)

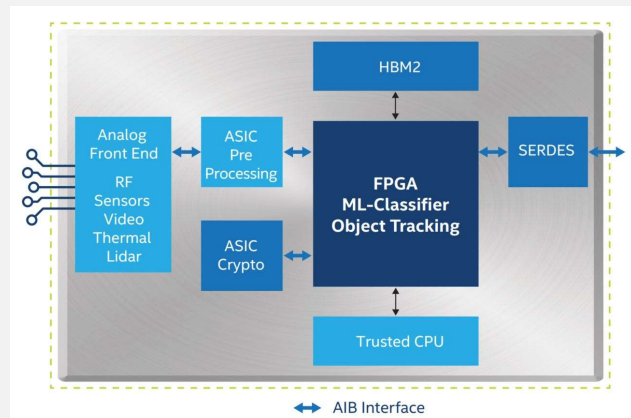
High Performance Systems with Heterogeneous System-in-Package (SIP)

Multi-chiplet integration on a single package enables complex systems with functional building blocks

- Advanced Interface Bus (AIB) - **high bandwidth, low power** die-to-die interface that provides a common interconnect independent of chiplet function or packaging technology
- System level Integration** of functions otherwise not possible with monolithic implementation
- Optimize** functions with the **right process** technology (example – SiGe for analog, 10nm for digital logic)
- Design **reuse** of common functions across platforms unlike monolithic implementations that require redesign every generation

Example Heterogeneous Integration: Machine Learning on RF Sensor Array Data

The example below shows the potential of heterogeneous integration of multiple functions using chiplets interconnected with the AIB interface.



Now possible: Advanced Multi-technology Systems in Package

Image Sources: Intel

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New Technology for Heterogeneous Integration

New **high density packaging** provides many more wires between dies than standard packaging technology

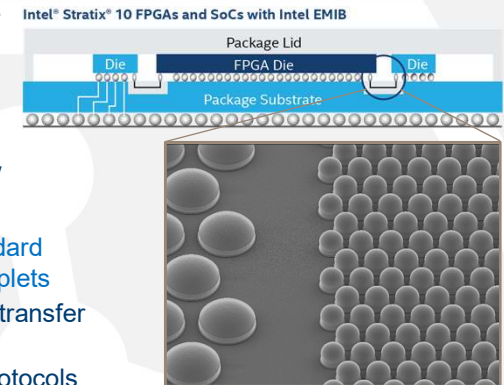
- Microbumps provide 5-10x IOs/mm² vs. standard flip-chip bumps
- This density is the base of the AIB low power, high bandwidth interface

AIB, Advanced Interface Bus, is a standard interface for data transfers between chiplets

- AIB is a clock forwarded parallel data transfer like DDR DRAM
- AIB is PHY level, OSI Layer 1, with protocols like AXI-4 or PCI Express on top of AIB
- AIB has **power and performance advantages** over conventional SERDES (Serializer/ Deserializer) interfaces

Metric		AIB	SERDES (typical)
Energy	Smaller is better	1pJ/bit ✓	16pJ/bit
Bandwidth/mm	Larger is better	615Gbps ✓	96Gbps
Latency	Smaller is better	3ns ✓	37ns

The performance figures shown are optimized on Intel technology. Performance varies based on system configuration.



	OSI Model Layer
7	Application
6	Presentation
5	Session
4	Transport
3	Network
2	Data Link
1	Physical

AIB

Enabling Next Generation Systems

Heterogeneous systems are part of Moore's Law, extending integration beyond monolithic devices

Mix best of breed technologies **AND** achieve near-monolithic bandwidth and power

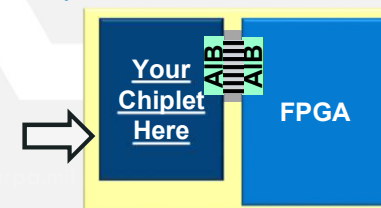
Use **AIB chiplets** to build your **next generation system**



Cramming More Components onto Integrated Circuits

GORDON E. MOORE, LIFE FELLOW, IEEE

...It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected. – 1965



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