Synopsys Semiconductor IP in Chiplet Format with AIB Interface for CHIPS Integration

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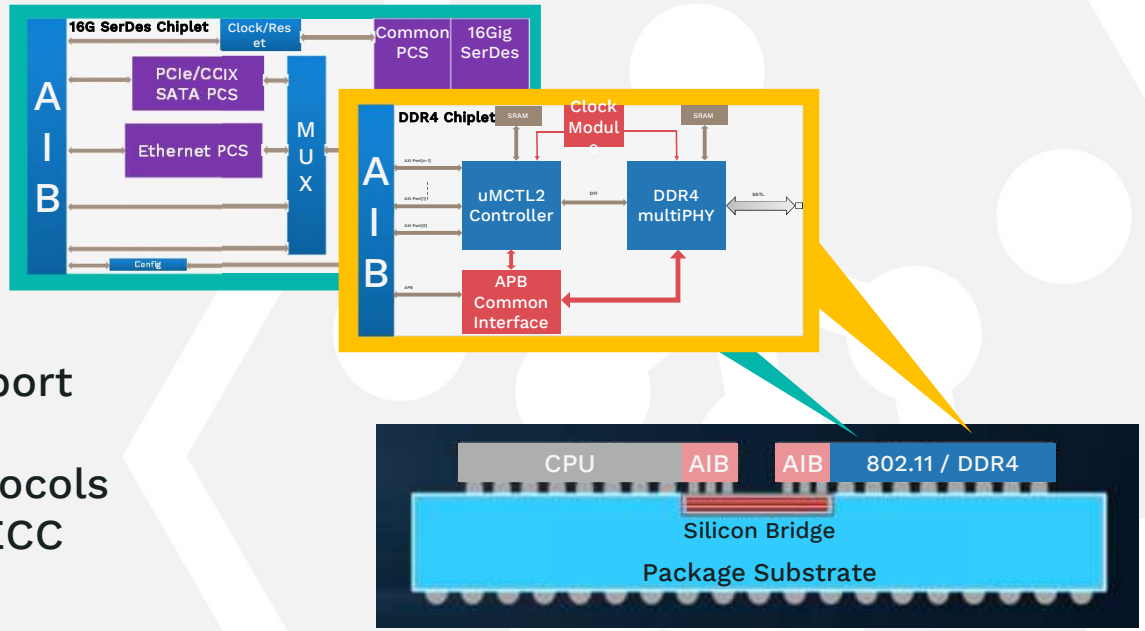
Materials & Integration: Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)

Leading-Edge Commercial IP Available for DoD Applications via CHIPS Ecosystem

State-of-the-art 16Gbps SerDes and DDR4 IP blocks with AIB interface for CHIPS integration

- Advanced Interface Bus and Chiplet Protocol Interface Support



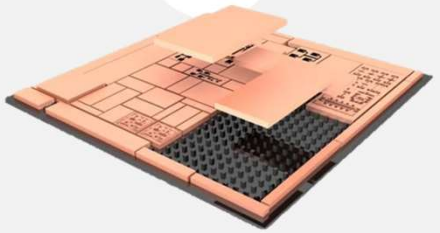
- 16Gbps for PCIe/CCIX Protocol Support
- 10Gbps Ethernet Support
- Common PCS bypass for other protocols
- DDR4 72b Channel: 64b Data + 8b ECC
- DDR4 2400 Support
- Supports -40C to 125C

Today's ASIC Flow

1) Purchase IP
2) Configure IP
3) Connect & Test to System
4) Harden/Close Timing
5) Manufacture
6) Assemble

New ASIC Flow with CHIPS

1) Purchase Chiplets
2) Assemble & Test



- **Ease ASIC Configuration – Swap interfaces in 4-5 weeks**
- **Lower Cost – Save over 250 weeks of effort**

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