2.5D System Design Using Modular Chiplets Based on Standard Interface

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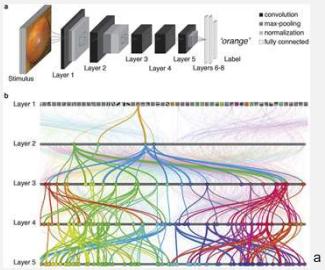
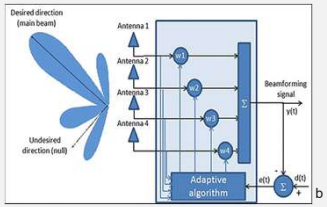
Materials & Integration: Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)

Machine Learning Systems
- Large-scale compute
- Large memory capacity
- High access bandwidth

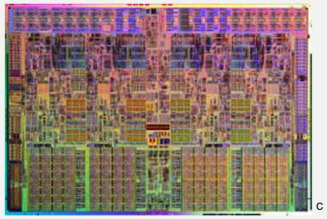


Smart Antenna Systems
- Mixed-signal
- Heterogenous integration
- High-bandwidth streaming



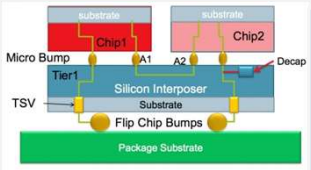
Current Approaches

Monolithic Integration
- Soft IP reuse
- High design effort, high risk
- Cost prohibitive



Board-Level Integration
- Hard IP reuse
- Heterogenous integration
- Low performance

New Approach: 2.5D Integration



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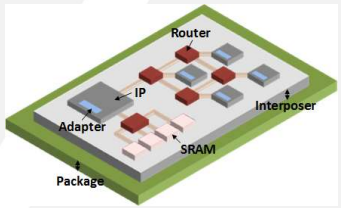
Benefits
- Hard IP reuse
- Heterogeneous integration
- High performance
- Lower effort
- Lower risk
- Lower cost

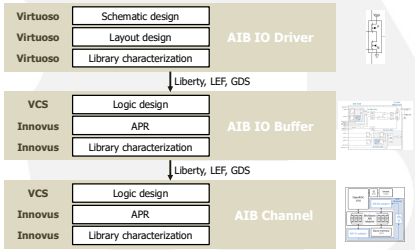
Challenges
- Need standard interface
- Need efficient high-speed IO
- Need availability of IPs
- Need use cases

Efficient Interface and Chiplets for Building High-Performance ML and Comm Systems

Modular 2.5D System Based on Intel AIB Interface

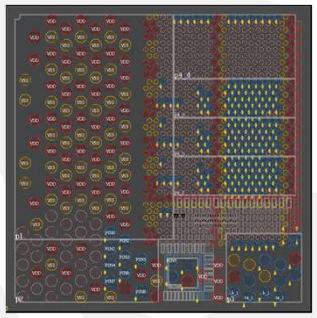


Automated Design of AIB IO

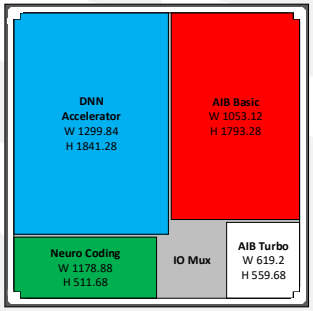


First Prototype Design

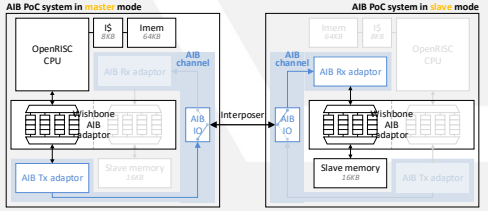
16nm CMOS AIB Test Chip with Micro and Core Bumps



RISC Processor, DNN, Neuro Coding, Ser-Des Chiplets



Prototype System



Potential Impacts
- IP reuse: >80%
- Heterogeneous integration: >3 technologies
- NRE reduction: >70%
- Time reduction: >70%
- Performance: >100%

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