

# Scalable, Energy-Efficient, And High-Throughput All-Memristor Neuromorphic Processor

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## Materials & Integration: Framework for Novel Compute (FRANC)



#### Summary:

To break the "memory bottleneck" of von Neumann architectures by developing an all-memristor NMC chip

#### **Technology Approach:**

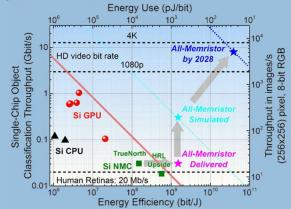
HRL's approach combines novel biomimetic active memristor spiking neurons with passive memristor synapses to build a spiking neural network (SNN) processor that can potentially reach human brain energy efficiency (EE) (0.1pJ/spike), density (10<sup>6</sup>/cm<sup>2</sup> neurons, 10<sup>10</sup>/cm<sup>2</sup> synapses), and complexity.

#### SOA & Challenges:

Current SOA processors are based on conventional CMOS technology – devices which do not naturally implement neurosynaptic functions

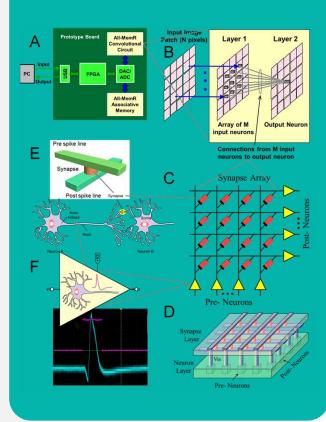
#### For image classification

- CMOS NMC (TrueNorth): SOA EE of 6.7 nJ/bit, low throughput of 30.7Mbit/s
- GPUs: SOA throughput ~1Gbit/s, but consume ~kW



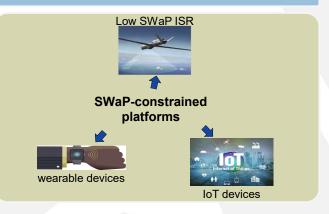
#### **Deliverable:**

HRL's FRANC program will deliver an image classification board (A) based on all-memristor NMC processors that perform convolution and associative learning (B) using crossbar networks (C) that integrate (D) scalable, energy-efficient, and biomimetic passive memristor synapses (E) and active memristor neurons (F).



NMC: neuromorphic circuit topology EE: energy efficiency SOA: state of the art SWaP: size, weight, and power SNN: spiking neural network

#### **Applications:**



#### <u>Metrics:</u> 10x enhancement in EE over the SOA Si NMC chip with comparable classification throughput

Metrics	SOA*	Phase 1	Phase 2	Phase 3		
EE	6.7nJ/bit	0.64nJ/bit	0.64nJ/bit	0.64nJ/bit		
	TrueNorth	Simulated	Designed	Tested		
Throughput	roughput 30.7Mb/s		33.4Mb/s	33.4Mb/s		
	TrueNorth		Designed	Tested		

\* Data from S. K. Esser et al., Proc. Nat. Acad. Sci. 113, 11441 (2016). DOI: 10.1073/pnas.1604850113

THE ELECTRONICS

**RESURGENCE INITIATIVE** 

### Transition Plan:

Mem	risto	or Sl	NN 1	<b>r</b> an	sitic	n Re	oadr	nap			
	2018	'19	<b>'20</b>	'21	'22	'23	'24	'25	'26	'27	'28 <b>&gt;</b>
FRANC Memristor SNN Dev	P1	P2		P3							
Early Adopt. Prog. Low SWAP ISR Wearable Devices		loeing/H Gov't/HF		Prog. L Prog. De	BA/ Dev. ALC BA/	W SWA	Syste	m dem m dem			
200mm Foundry Transition			F	oundry E	Mai Engage. /	-	v. Feas ry Trans		qual. F <i>d. Dev</i> .	Prod. re	eleased
300mm Foundry Transition						Found	lry Engag		t gate T Indry Tra		ual. gate

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