Scalable, Energy-Efficient, And High-Throughput All-Memristor Neuromorphic Processor

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Materials & Integration: Framework for Novel Compute (FRANC)

Summary:

To break the "memory bottleneck" of von Neumann architectures by developing an all-memristor NMC chip

Technology Approach:

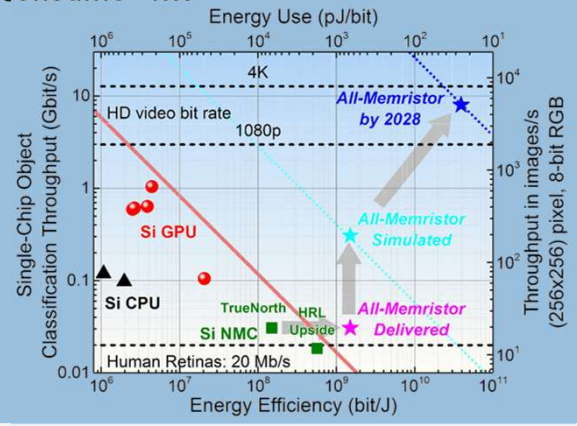
HRL's approach combines novel biomimetic active memristor spiking neurons with passive memristor synapses to build a spiking neural network (SNN) processor that can potentially reach human brain energy efficiency (EE) (0.1pJ/spike), density (10^6/cm^2 neurons, 10^{10}/cm^2 synapses), and complexity.

SOA & Challenges:

Current SOA processors are based on conventional CMOS technology – devices which do not naturally implement neurosynaptic functions

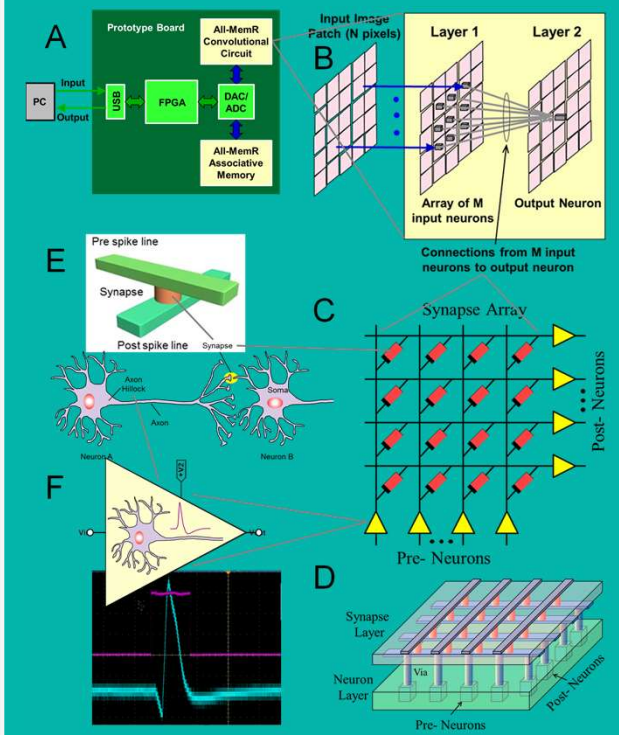
For image classification

- CMOS NMC (TrueNorth): SOA EE of 6.7 nJ/bit, low throughput of 30.7Mbit/s
- GPUs: SOA throughput ~1Gbit/s, but consume ~kW



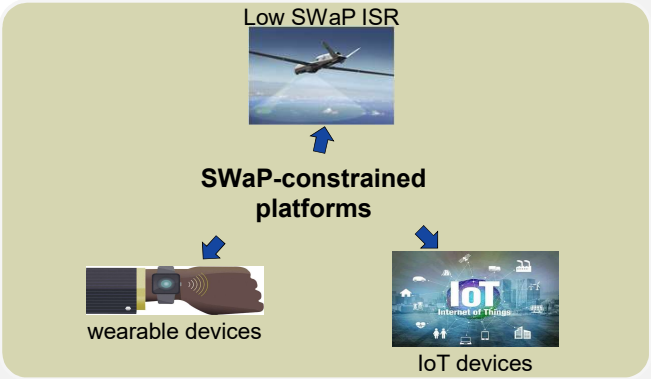
Deliverable:

HRL's FRANC program will deliver an image classification board (A) based on all-memristor NMC processors that perform convolution and associative learning (B) using crossbar networks (C) that integrate (D) scalable, energy-efficient, and biomimetic passive memristor synapses (E) and active memristor neurons (F).



NMC: neuromorphic circuit topology
EE: energy efficiency
SOA: state of the art
SWaP: size, weight, and power
SNN: spiking neural network

Applications:

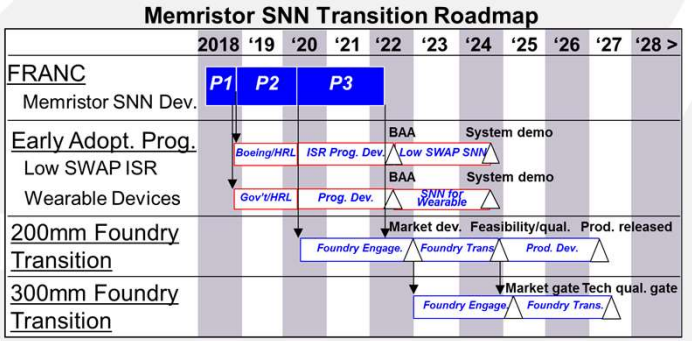


Metrics: 10x enhancement in EE over the SOA Si NMC chip with comparable classification throughput

Metrics	SOA*	Phase 1	Phase 2	Phase 3
EE	6.7nJ/bit TrueNorth	0.64nJ/bit Simulated	0.64nJ/bit Designed	0.64nJ/bit Tested
Throughput	30.7Mb/s TrueNorth	33.4Mb/s Simulated	33.4Mb/s Designed	33.4Mb/s Tested

* Data from S. K. Esser et al., Proc. Nat. Acad. Sci. 113, 11441 (2016). DOI: 10.1073/pnas.1604850113

Transition Plan:



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