OSD and Air Force Microelectronics Design and Prototype Challenge

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Senior Electronics Engineer, United States Air Force

2020 DARPA ERI Summit
Creating a Resilient and Robust Microelectronics Pipeline

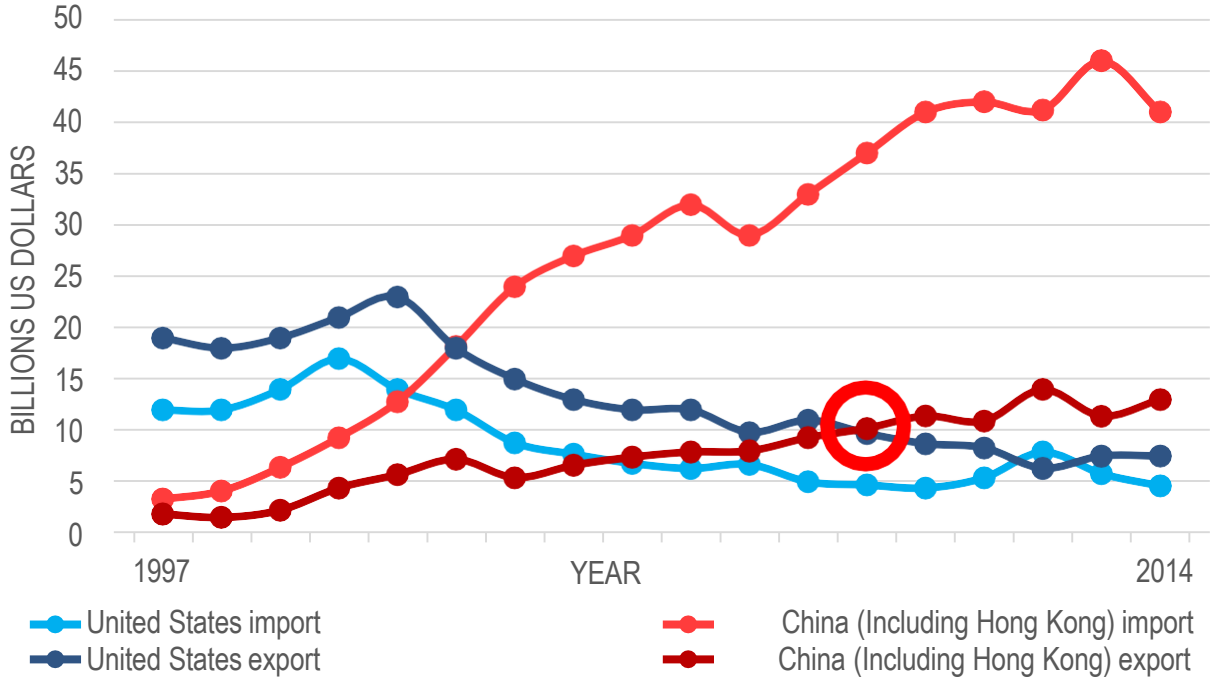
19 August 2020

https://www.CTO.mil *@DoDCTO*

Current State of Affairs

Horizontal Integration of Semiconductor Fabrication

- ***Increased cost for state-of-the-art foundry***
- ***Increased Reliance on Third-party Manufacturing***
- ***Reduction in U.S. semiconductor manufacturing***
- ***Increased Risk***

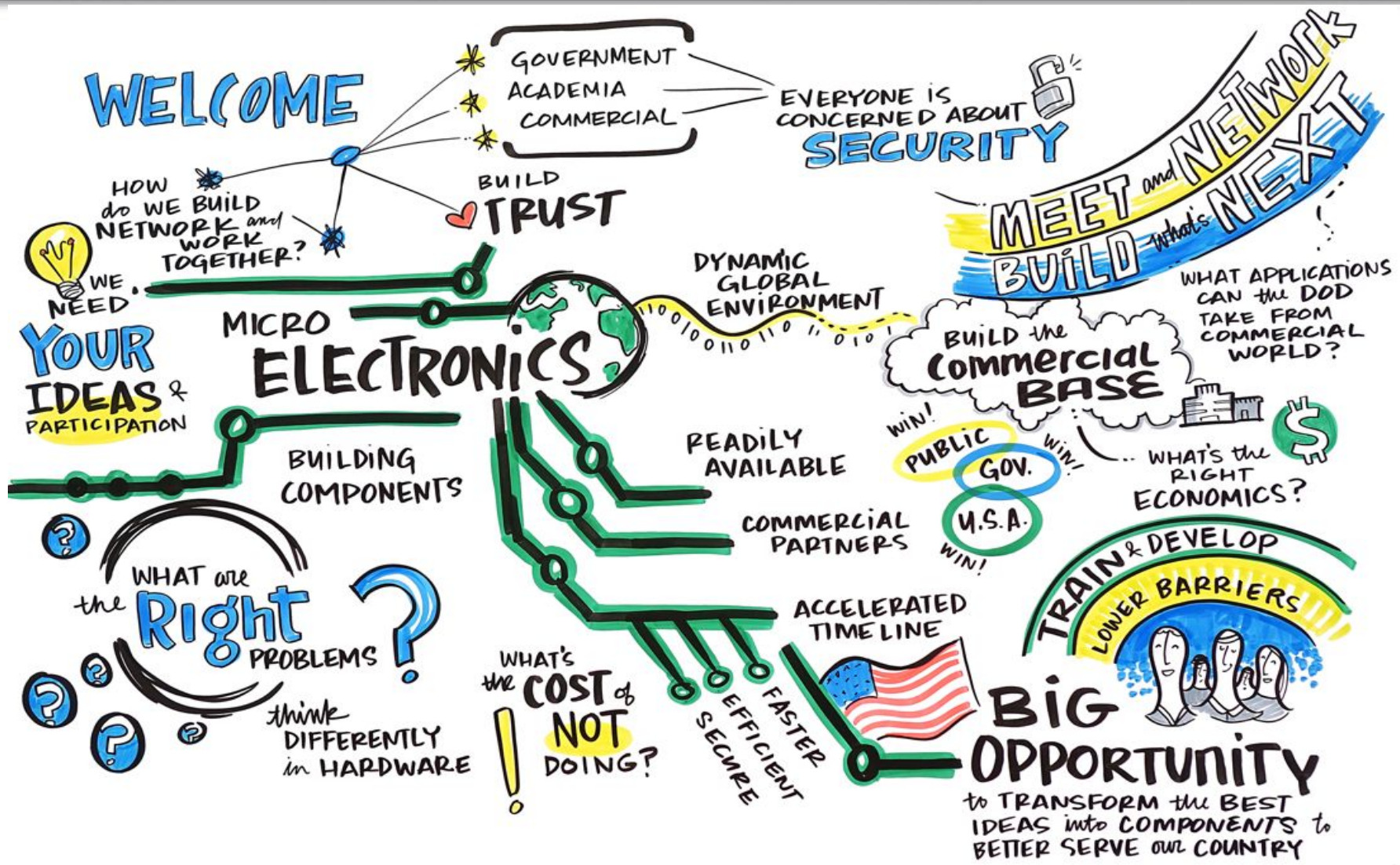


Desires

- ***To maintain access to SoA IC facilities and technologies***
- ***Increase domestic workforce***
- ***To reduce risk***
- ***To prevent IP theft, malicious modification***

Source: Center for International Data from Robert Feenstra
Source: BACI International Trade Database

Innovation Pipeline



Innovation Challenges

Stimulating and Supporting Innovation:
Lowering barriers to advanced IC technologies
Encouraging and adopting rigorous design practices
Providing IP design capture, integrity, and assurance environments and tools

In Progress…

Source: https://afwerxchallenge.com/microdesign

ICs for operation or improvement of a self-defined autonomous product while maintaining the provenance, traceability and security needs.

82 Proposals
44 Showcase Participants
Phase 2: 10 Performers
Phase 3: 4 Performers/3 Teams

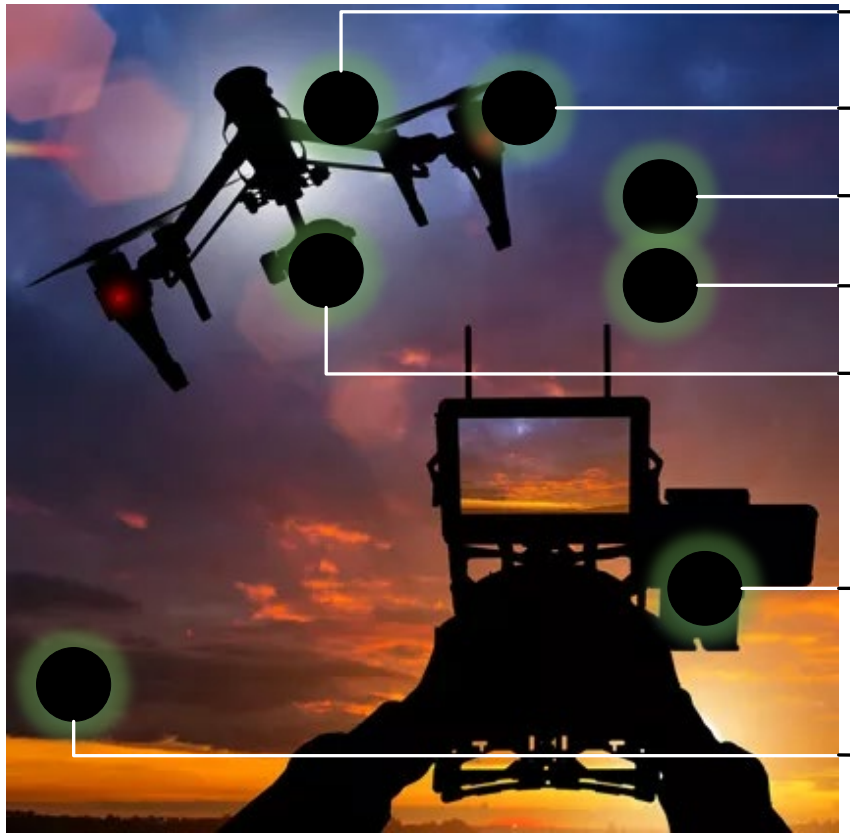
Commercial application, Dual-use, Non-ITAR

Phase 1: ~ 2.5 months
Submit Proposals
Phase 2: ~ 4 months
Design & Simulation
Phase 3: ~ 6 months
Physical Design
Phase 4: ~ 7 months (incl. fabrication)
Physical Prototype
Phase 5: ~ 5 months
Prototype Testing and Demonstration
Phase 6: TBD
Full Production

Addressing Domestic Autonomous Needs

Applicable Performer Technologies

- Interior Department grounds its drones over Chinese **spying fears** and **cyber security concerns**.



- Enhanced Sensor Interfaces
- Navigation Systems
- Autonomy
- AI/ML Capabilities
- Computer Vision
- Improved Mission Duration

Microelectronics Design/Prototyping Range
-Federated Cloud Development Platform
-SoA Commercial Design Tools and IPs
-Traceability, Provenance, Assurance, from Concept through End-of-Life

Source: https://www.nytimes.com/2020/01/29/technology/interior-chinese-drones.html

Source: https://techcrunch.com/2020/01/29/interior-ground-drones-cybersecurity/

Advanced Microelectronics Design and Prototype Challenge (1/2)

Embodiment of Innovation Challenge

Phase 2 Performers

DEFENSEWERX

E y L

|galois|

GrAI Matter Labs

INDIANA INTEGRATED CIRCUITS, LLC.

borsetta

InertialWave

uTD

LUCID CIRCUITS

Ridgetop Group Inc.

IoT/AI
(Intelesense Technologies)

Current Vendor Partners providing EDA, IP, and Support

ANSYS

arm

cādence

GLOBALFOUNDRIES

synopsys

Tortuga Logic

onespin

ME Ecosystem Provided via Existing Infrastructure

Nimbis Services

DoD-accessible challenge focusing on innovation through offerings of SoA technologies and reducing their costs to non-traditional performers where the USAF is the licensee.

Advanced Microelectronics Design and Prototype Challenge (2/2)

Embodiment of Innovation Challenge

Phase 3 Teams

★ARCNet

|galois|

InertialWave / UTD

IoT/AI
(Intelesense Technologies)

Current Vendor Partners providing EDA, IP, and Support

ANSYS arm cādence

GLOBALFOUNDRIES

synopsys Tortuga Logic onespin

ME Ecosystem Provided via Existing Infrastructure

Nimbis Services

DoD-accessible challenge focusing on innovation through offerings of SoA technologies and reducing their costs to non-traditional performers where the USAF is the licensee.

ME Challenge Secure Design Environment

Paradigm Shift in Microelectronics

- Limited Users within Team Projects (no repo/data sharing)
- Elevated Users within AFRL Team Project (yes repo/data sharing)
- Images built with no internet access.

Cadence Image
Synopsys Image
Hybrid Images
Arm Image
⋮

Vendor Partners: ANSYS, Arm, Cadence, Nimbis Services, GLOBALFOUNDRIES, OneSpin, Synopsys, Tortuga Logic

Nimbis IT Support

Access granted per signed vendor agreements & AFRL concurrence

Ingress Data
Restricted
Ports Access

Project@Team1
Ind1@Team1
repo1_T1
Ind3@Team1
repo3_T1
Ind2@Team1
repo2_T1
…
Repo Sharing w/in Project

No Repo or Data Sharing

Project@Team2 …
Ind1@Team2
repo1_T2
Ind3@Team2
repo3_T2
Ind2@Team2
repo2_T2
…
Repo Sharing w/in Project

Ingress Data
Restricted
Ports Access

Project@AFRL
Ind1@AFRL
Synopsys IP Repo/Team
Arm IP Repo for All
⋮

Cadence License Server/ Team
Synopsys License Server/ Team
Synopsys IP Server/ Team
…
Access Managed via License Managers

Providing Ready-to-use Design Environments
Protecting Vendor and Performer IPs
Enabling Multi-party Collaborations
Providing Provenance and Traceability

*Example for Discussions

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Performer's Testimonial Pay-offs, Benefits, and Impacts

- Access to and design in advanced node IC technology at a reduced cost (~Typically 100s of thousands of dollars for small chips)
- Increased computing, AI capabilities
- Introductions to the microelectronics' vendors; working business relationship and potential product
- Access to ~$10Ms of IPs and EDA tools per performer
- Access to advanced computing infrastructure
- Access to vendor support and training
- Design prototypes with reduced upfront costs
- Prototypes can be used to raise funding for production run and new starts
- Simply could not develop 12 nm secure chips without support from ME challenge.
- Huge impact on human resource development: University teams gain access to unprecedented level of tools and IPs to help them grow professionally and offer US marketable skills

Innovation Accelerators: Other Challenges

In-Progress

AFRL

GaN RF Design Challenge

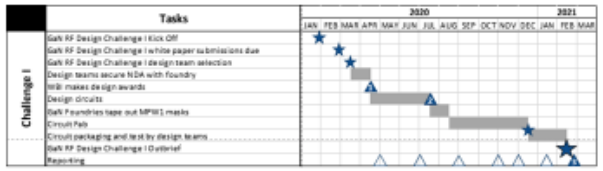
Challenge Objectives
- Remove barriers to entry to leverage GaN technology
- Engage with non-traditional GaN PA designers
- Foster domestic design and fabrication capability
- Enable rigorous RF design practices
- Provide cloud-based design capture and assurance

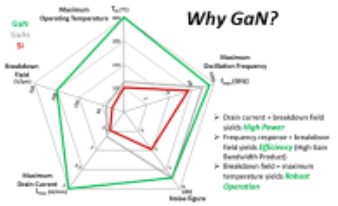
QORVO BAE Systems

Nimbis Services

AFRL/RYD & Navy NSWC Crane in conjunction with Wright Brothers Institute (WBI) & Nimbis are executing challenge
- Selected design teams receive access to one of two advanced GaN foundries – ***Qorvo 150nm for 5G*** or ***BAE 180nm for EW***
- Cloud EDA tools (ADS and AWR) and PDKs provided through Distributed Transition Environment (DTE) via Nimbis
- MPW runs for prototype circuits for design team evaluation
- Packaged and tested circuits to be delivered to government for verification

1ST of three planned cycles (roughly annual cadence)





10 Design Teams out of 24 submissions received awards

5G Design Teams
CU, Gtech, Teledyne Technologies, Obsidian Microwave, SenseICs, MaXentric

EW Design Teams
MSU, NAVSEA, ReconRF, MaXentric AFRL, Electromagnetics Technologies, Inc.

*Government Design Teams self-funded

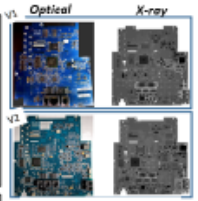
- III-V Technologies
- Domestic Foundries: Qorvo and BAE Systems
- Performers include non-traditional small businesses and universities.
- Performers are designing power amplifiers for 5G or EW
- Using ANSYS, cādence, and Keysight EDA tools

Completed

Supply Chain Challenge

Summary

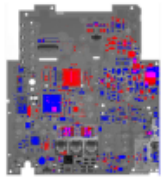
AFRL and AFWERX have partnered to launch the Supply Chain Provenance Challenge geared around demonstrating solutions that help solve the current microelectronic supply chain problem. The challenge is attempting to identify solutions that are non-destructive in nature and prove provenance and suitability for military use of microelectronic parts in commercial off the shelf hardware to be used on base installations or in operation.



Participants

BATTELLE
KPMG
KBSI

Brunel
Supply Dynamics
Object Security
Riverside Research

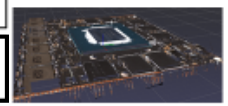


Sponsors

cisco nVIDIA

Demonstration

International Test Conference, Nov. 12-14, 2019
Marriot Washington Wardman Park



Winner: Team 2

Brunel
Supply Dynamics

Summary and Highlights

- Addressing domain of autonomous systems, which augment lack of domestic sources
- OSD ME Challenge is currently in Phase 3.
- Mid-point review on August 27
- All performers have access to platform.
- Performers pushing through physical design.

- Funding enhancement provided by another service agency.
- First demonstration of non-egress secure design for challenges.
- ME challenge helped set up methodology for other innovation accelerators.
  - Commercial support, training, maintenance, and vendor involvement in the DoD ecosystem.
- Created best practices document to navigate the DoD's process for access to GF's IPs, PDKs, and fabrication via DMEA and KCNSC.
- Increased DoD's knowledge-base and understanding for infrastructure and deployment of advanced ME IPs and EDA tools (Workforce development and experience)
- Paradigm shift: DoD representative model for how a Service can be the licensee for ME IPs and EDA tools
  - ME challenge model (IP, EDA, pricing, and purchasing) being extended into other DoD-wide approaches to ME.

Acknowledgments

- USAF, OSD, and Government Team
  - AFRL: Todd James, Kevin Miller, Ray Garcia, Stacie Smith-Turner, Susan Borger Ranly, P. Len Orlando III, April Ratliff, Brooke Jett, and Team
  - DMEA/TAPO: Michael Kessler, Jean Pierre Crovetto, Jon Lloyd, and Team
  - DefenseWerx: Greg Britton, Mohamed Kassem, and Team
  - ARCNet: Andrea Seitz, Marcia Gross, Mark Pohl, Ken Wall, Corey Schumacher, Stella Speranza, and Team
  - AFRL/RW, AFRL/RI, 96 TW/JAQ, AFLOA/JAQ, AFMCLO/JAZ, AFRL/SDPE, 711 HPW, AFWERX
- Vendor Partners
  - Arm: Jose-Maria Moniz, Russell Powell, Jennifer Chen, and Team
  - Ansys: Scott Granger, Gary Hunt, and Team
  - Cadence: Jeff Hutton, Rich Gast, Jai Iyer, Morteza Shafiei-Sarvestani, and Team
  - GlobalFoundries: Sebastian Ventrone, Lance Pickup, David Brown, James Mecke, Terry Lovelette, and Team
  - Nimbis Services: Schoeller Porter, Shaun Brady, Jim Jobe, and Team
  - OneSpin: John Rockfort, David Landoll, and Team
  - Synopsys: John Kapinos, Shawn Fetterolf, Sean Curry, and Team
  - Tortuga Logic: Jason Oberg, Jagadish Nayak, Juan Chapa, and Team
- Performers
  - Borsetta, Inc., Eyl, Inc., Galois, Inc., GrAI Matter Labs SAS, IIC, LLC, Inertial Wave, Inc., Intelesense Technologies (IOTAI), Lucid Circuit, Inc., Ridgetop Group, Inc., UT at Dallas

ME Challenge:
Phase 3 Performer Technologies

GLASS-CV – Galois Low-energy Asynchronous Secure SoC for Computer Vision

Jason Graalum, jasongraalum@galois.com

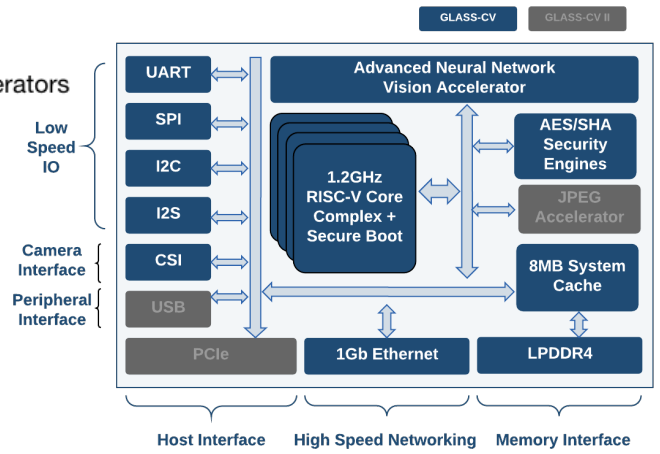
Low-Power, Secure System-on-Chip (SoC)
Specifically targeted for autonomous systems

Advanced Accelerators
Efficient AI, image processing, and DSP accelerators

Formally Verified Gbps Cryptography
Architected for anti-tamper data protection

Secure-Boot
RISC-V general purpose processor

High-Speed I/O
PCIe, Ethernet, DDR4, USB, CSI



Problem Statement

Computer Vision and Artificial Intelligence applications can enable many autonomous, IoT and edge applications. Currently available commercial processors for such are too power hungry and do not fit within the power profile that such applications frequently require. Additionally existing solutions do not address security at all.

Objective

Create a secure processor SoC, capable of executing CV and AI workloads in real-time, while operating within a 1W TDP power envelope. Achieve unprecedented energy efficiency while executing complex machine learning algorithms.

Technical Approach

- **We integrate formally verified hardware cryptographic accelerator cores for data security and a secure-boot complex for tamper detection**
- **We implement a variety of methods to test provenance techniques including logic obfuscation and power modeling**
- **We use asynchronous circuit technology to enable aggressive voltage scaling achieving dramatic power efficiency**

Target Application and Demonstration

- **Small drones, intelligent sensor networks, mobile/wearable vision systems.**
- **We will present a physical demonstration of thermal failure in current solutions comparable to GLASS-CV.**

Customers/Partners/Stakeholders

- Customers/stakeholders
  - GE, Oil&Gas
  - IC
- Service Interests
  - SOCOM
  - USAF (SMC)

Inertial Navigation System on a Chip Development

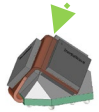
Peter Bond, peter@inertialwave.com

Honeywell RLG based INS:
100 in^3,10W, $100K (today)

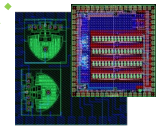
Nav Grade Performance:

Low Volume

High Volume



MEMS based INS:
2in^3,1W, $300 (2021)



SOA MEMS
Inertial Sensors,
IW Algorithms IP
Sensor Controllers

UT Dallas/ Univ. Minnesota Trusted IC, Ultra low noise timing

Bliley Tech.
Atomic
Clock Stable
Algorithms

Problem Statement

State of the art high-end Inertial IMU/INS solutions power consumption and volume are too large for A-UAV systems. Much of that power and size comes from the inefficient inertial sensor and INS processing. There are currently no SoC-based INS commercial or military market solutions that provide high end performance (tactical grade and higher) that can address the power and volume needs of A-UAVs. Added capabilities for TRUSTED IC.

Objective

The SoC implements a robust inertial navigation system (INS) operating with navigation grade inertial sensors, integrated atomic clock accurate timing, vision aiding & localization, and GPS anti-spoofing. It incorporates extensive security for resilience to tampering, HW attacks, and counterfeiting. The 14nm technology drastically reduces SWaP & enables self-calibrating navigation for ubiquitous trusted inertial-based sub-millimeter position awareness and low noise long term stable timing in Air Force autonomous systems.

Technical Approach

- The SoC incorporates InertialWave's innovative inertial sensor controller technology which integrates a direct digital baseband architecture, inertial sensor control, compensation and electronic self-calibration algorithms, and sensor fusion algorithms implemented in a 6-degree of freedom (DOF) multi-channel configuration to provide an ultra-compact solution. Added capability for short term noise, long term stable clock generation for timing support.

Target Application and Demonstration

- Our target application is to provide resilient mission operation with precise positioning, navigation, and timing capabilities integrated into autonomous unmanned air vehicles (A-UAVs) operating against a peer or near-peer adversary in inherently contested cyber and electromagnetic environments.

Customers/Partners/Stakeholders

SoC Team (Phase 3)

UT Dallas U of Minnesota

Demo Partners (Phase 4/5)

U of Washington, A-UAVS

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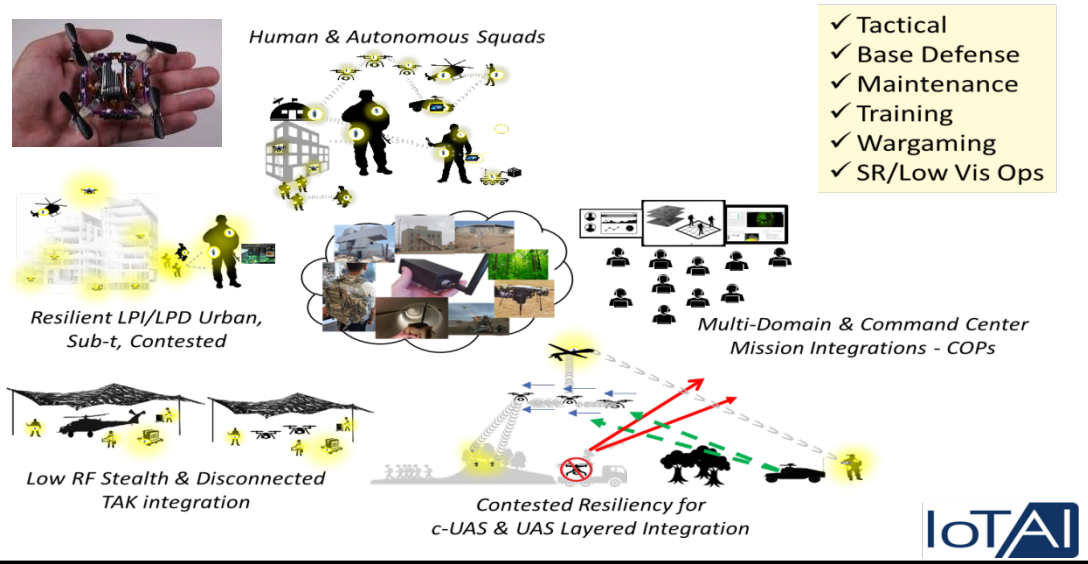
IoT/AI Autonomous Nanodrone for In-building and Subterranean Operations

(Intelesense Technologies)

Dr Kevin Montgomery, kevin@iot.ai



Problem Statement

- Current UAV RF comms can be easily jammed/cracked/spoofed
- Cant penetrate far into buildings/subterranean environments
- Current recon drones too big for subterranean environments

Objective

Next-generation trusted radio with superior penetration/ security with advanced mesh network on pocket nanodrone, Low power/weight/size

Technical Approach

- Shrink existing field-proven next-generation radio/comms platform down to low-power, low-size single-chip implementation for use in nanodrones, sensors, personnel,…

Target Application and Demonstration

- Deep in-building/subterranean reconnaissance using pocket-sized nanodrone that cannot be jammed/cracked/spoofed
- Additional benefits: Generalized ultrasecure comms platform for ATAK, sensors, general UAV use, etc with high scalability and resilience

Customers/Partners/Stakeholders

USAF:
- ABMS/Agile Combat, Base Security, Flightline of the Future)

Army:
- School of Infantry, Futures Command)

DHS/DOI:
- Drone communications

Non-govt:
- Emerson Process Controls, Amazon, Textron, ENSCO