2020 DARPA ERI Workshop

Security and Access - Access to State of the Art Microelectronics with Quantifiable Assurance

Wednesday, August 19, 2020, 2:15 - 5:45 PM

Dr. Morgan Thoma, Office of the Under Secretary of Defense for Research and Engineering (OUSD(R&E))
Dr. Brian Dupaix, Air Force Research Lab (AFRL)

The Department of Defense (DoD) is committed to the secure development and demonstration of new microelectronics technology solutions. This workshop will review two major DoD thrusts: 1) Access to State of the Art Commercial Technology and 2) Data-Driven Quantifiable Assurance. These initiatives are leveraging strategic partnerships with commercial domestic providers to perfect a data-driven, "zero-trust" risk-based approach for supply chain protection and assured access to advanced microelectronics technology and electronic components. The workshop will examine new assurance paradigms and standards for supply chain protection and methods for strengthening security while improving access to and protection of sensitive intellectual property (IP). Quantifiable assured design concepts will be discussed along with risk-based protection techniques that meet or exceed National Security Agency standards for IP protection. The goal of these thrust areas is to keep pace with the advancements in microelectronics technology and the globalization of the industrial sector.

Agenda – Access to State of the Art Commercial Technology

• Introduction	Morgan Thoma
• Secure Design – Trusted Silicon Stratus (TSS)	Len Orlando
• Front Door Foundry Access	Morgan Thoma
• User Experience	Saverio Fazzari
• Access to GlobalFoundries/TAPO	Aman Gahoonia
• Access to SOTA • Technology Exploration and Engagement	John Damoulakis
• Q&A - Discussion	Panel

Trusted and Assured Microelectronics Program

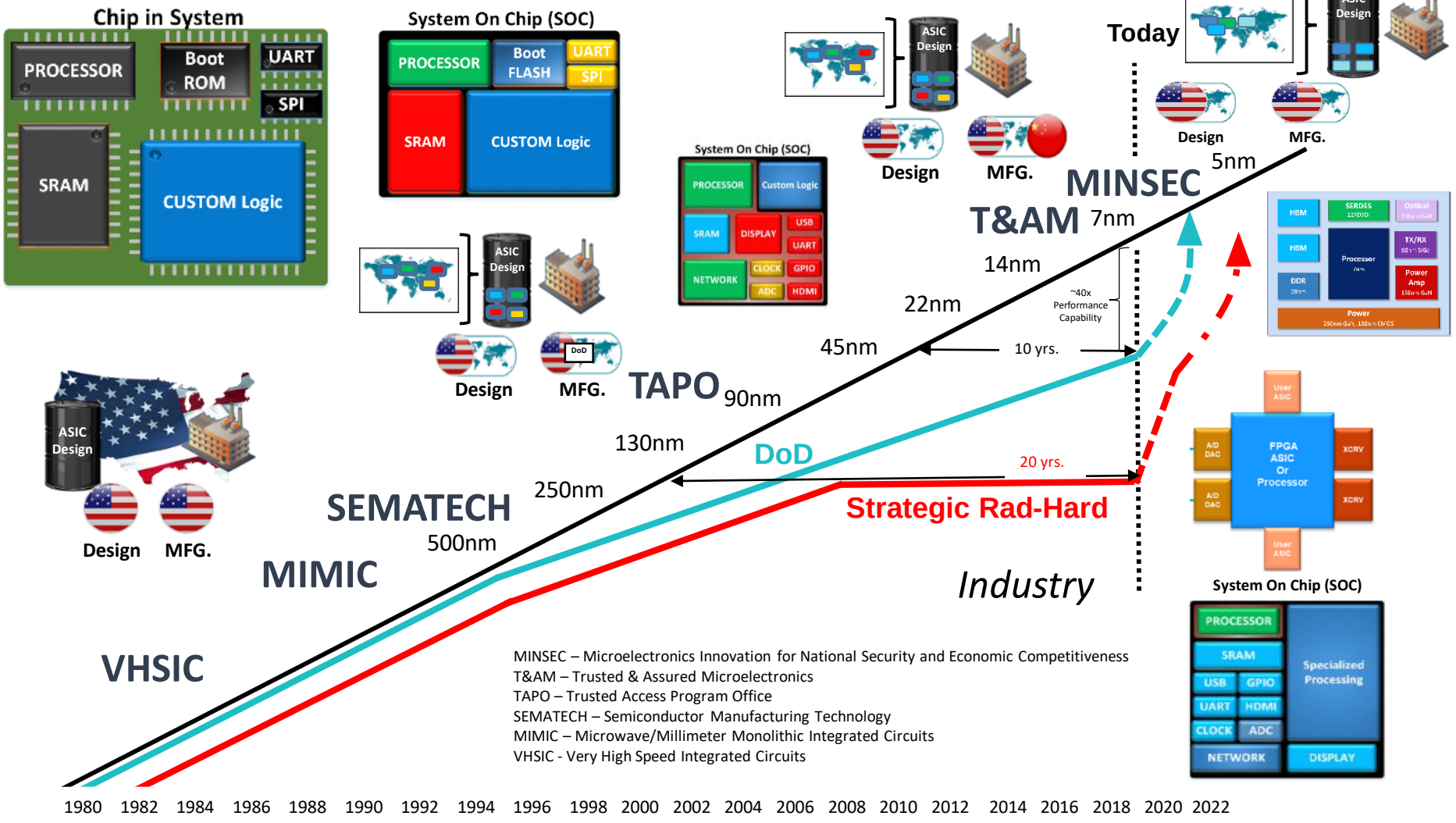
Access to State of the Art Commercial Technology

Morgan Thoma, Ph.D., Project Lead

August 2020

https://www.CTO.mil @DoDCTO

Assured Microelectronics Evolution



MINSEC – Microelectronics Innovation for National Security and Economic Competitiveness
T&AM – Trusted & Assured Microelectronics
TAPO – Trusted Access Program Office
SEMATECH – Semiconductor Manufacturing Technology
MIMIC – Microwave/Millimeter Monolithic Integrated Circuits
VHSIC - Very High Speed Integrated Circuits

T&AM/MINSEC Program is developing the secure ecosystem to assure SOTA performance for Modernization

Trusted and Assured Microelectronics Strategic Approach

Microelectronics - DoD's Top Modernization Priority

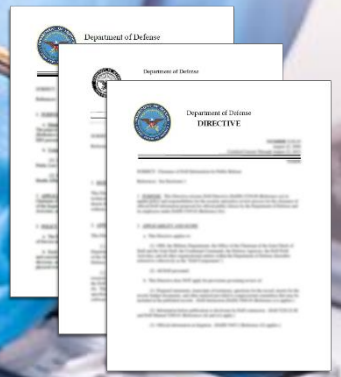
We cannot expect success fighting tomorrow's conflicts with yesterday's weapons or equipment.

-National Defense Strategy

	Access to State of the Art Commercial Technology	Data Driven Quantifiable Assurance	Address DoD Unique Needs	Create a Resilient and Robust Pipeline
				
Gaps:	DoD lags commercial CMOS ecosystem/ infrastructure	Threats to design and manufacturing in global supply chain	Increased sources for national strategic defense	Domestic and Allied Ecosystem to rapidly and securely mature emerging advanced technology
Approach:	Establish best practices for secure design, assembly, packaging, and test capabilities to support DIB and co-development of dual use electronics	Secure full lifecycle confidentiality, Integrity, verification & validation, and supply chain for assured warfighters electronics	Develop sustainable sources of mission essential niche rad-hard electronics capabilities, and specialized radio frequency and electro-optic components	Invigorate secure pipeline for disruptive R&D transition, supply chain aware technology development, education and workforce.

Access to State of the Art Commercial Technology

Get on the commercial curve and secure data products!



Secure Design

- Secure Design Cloud Infrastructure and persistent expertise
- Secure Design EDA, V&V, and HW Emulation tools leveraging commercial best practice
- Secure Design Intellectual Property for multi-vendor access

Front Door Foundry Access

- Support a multi-foundry access model for commercial SOTA technology access
- MPW access for DoD sponsored development
- Exploration and Engagement on new technologies to develop commercial access

Advance Packaging and Test

- Digital and RF heterogeneous integration design and advanced packaging and test proto-type capability.
- Develop Root of Security
- Specialty capability and transition

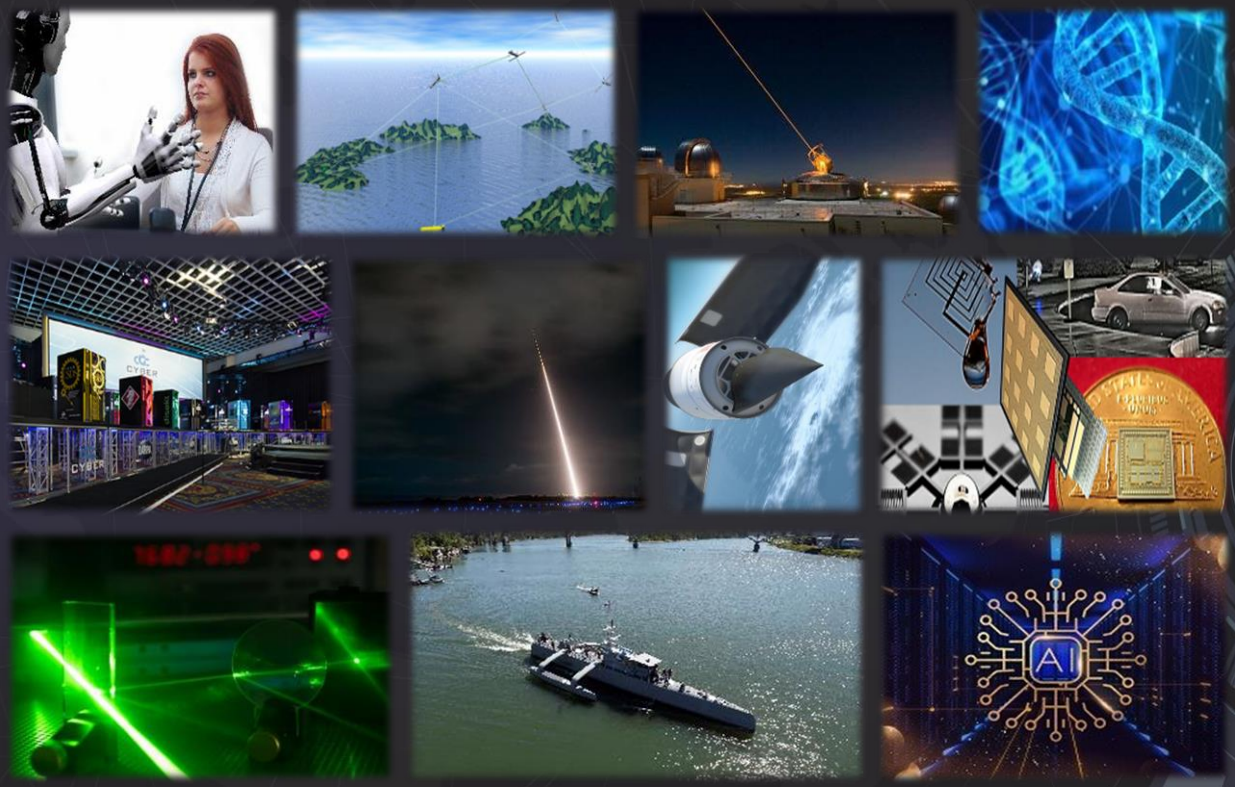
Policy & Standards

- Supportive framework for SOTA Access
- Trust, Export Control policy, and Commercial Supply Chain Standards
- Engagement in Standards bodies

Program* Development & Capabilities → **PPP*/ CPI** → **Design** → **Verify** → **Mask** → **Fabrication** → **Pack. & test** → **Verify & validate** → **Config./ prog. SW** → **Integrate & test** → **Operation & maint.**

DoD Research and Engineering Enterprise

Creating the Technologies of the Future Fight



DoD Research and Engineering Enterprise
https://www.CTO.mil/

Twitter
@DoDCTO

Agenda – Access to State of the Art Commercial Technology

• Introduction	Morgan Thoma
• Secure Design – Trusted Silicon Stratus (TSS)	Len Orlando
• Front Door Foundry Access	Morgan Thoma
• User Experience	Saverio Fazzari
• Access to GlobalFoundries/TAPO	Aman Gahoonia
• Access to SOTA • Technology Exploration and Engagement	John Damoulakis
• Q&A - Discussion	Panel

Access to State of the Art Microelectronics Secure Design

P. Len Orlando III

Air Force Research Laboratory – Sensors Directorate (AFRL/RYDT)

Secure Design

Benefits to Warfighter/ Deliverables

- Secure Design Environment serves as the information conduit for quantifiable assurance and risk based assessments of microelectronics
- DoD ME enterprise common configuration management
- Persistent data access, archival, and sharing
- Provenance and traceability built-in to determine who did what, when it was done, and what was modified.
- Scalable compute infrastructure leveraging commercial economies of scale

Description

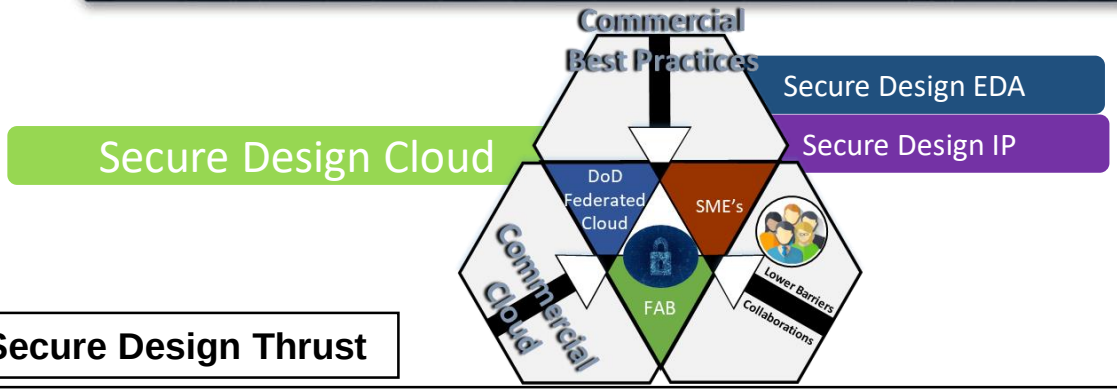
- Multi-Service multi-tenant ATO-approved secure cloud environment enabling Government, DiB, FFRDC, University, and Small Business collaboration of SOTA Microelectronics.
- Modular and automated configuration management
- Built upon commercial cloud technologies
- Granular access controls of IP, Process Design Kits, electronic design automation tools, ME Hardware

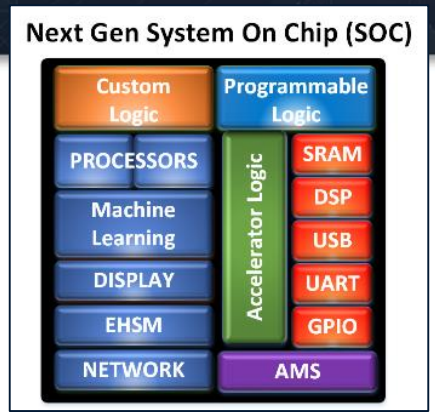
A Secure Design Cloud
- Development, management, and maintenance of cloud infrastructure

B Secure Design EDA
- Enterprise Licensing of COTS design software and hardware

C Secure Design IP
- Enterprise Licensing of IP

Secure Design





Secure Design Thrust

(1) Provides access to SOTA foundry offerings, design environments, and intellectual property necessary for SOTA Application-specific integrated circuits
(2) Enables lifecycle quantifiable assurance assessments to be performed
(3) Multiple Vendor access

Accomplishments:
- ATO'd secure design environment
- ***12 Security Technical Implementation Guide compliant appliances, Windows and Linux deployments,***
- ***Automated processes that enable time to deploy (weeks) having standardized configurations via automation***
- ***4 tapeouts performed – 11 on-going***
- ***Terraformation across 2 commercial clouds has been demonstrated***
- ***2 Challenges Microelectronics and RF GaN***
- ***Big 3 in EDA supporting Digital, AMS, and RF, specialized tools for multiphysics analysis, emulation, and security.***
- ***Multiple analytical engines from Assurance Community***

Agenda – Access to State of the Art Commercial Technology

• Introduction	Morgan Thoma
• Secure Design – Trusted Silicon Stratus (TSS)	Len Orlando
• Front Door Foundry Access	Morgan Thoma
• User Experience	Saverio Fazzari
• Access to GlobalFoundries/TAPO	Aman Gahoonia
• Access to SOTA • Technology Exploration and Engagement	John Damoulakis
• Q&A - Discussion	Panel

Trusted and Assured Microelectronics Program

Access to State of the Art Commercial Technology

Front Door Access

ERI Summit SOTA Workshop slides

August 2020

https://www.CTO.mil @DoDCTO

Front Door Foundry Access to SOTA Technology

Key Partnerships

POC: Morgan J. Thoma, OUSD(R&E)

Key DoD/USG Partners: AFRL, DARPA, DMEA

Key Contract Partners: GlobalFoundries, Intel, MOSIS

Description

- Enable access to SOTA US commercial foundries ≤ 32nm for DoD-specific designs
- Invest in and pursue access to multiple vendors through lifecycle quantifiable assurance protections of sensitive design information

How is this addressing the Roadmap Milestones

- Currently the DoD has limited access to SOTA ≤ 32nm technologies
- Provide access to multiple vendors of SOTA processes not currently accessible to the USG
- Provide MPW runs in support of Quantifiable Assurance goals and to aid in developing DoD specific PDK's and IP as well as enabling US vendors to improve their ability to operate more effectively as a foundry.

Benefits to Warfighter/ Deliverables

- Provide more timely access to SOTA technologies using quantifiable assurance methods no later than 2 years after contract award
- Enable SOTA products to be fielded in a more timely manner with less risk of the technologies becoming obsolete and unavailable

Front Door Foundry Access Objectives

- Technology Access – Exploration and Engagement
  - What technologies that meet USG needs are potentially available for access
- MPW Access
  - PDK delivery, availability and usability - TSS
  - Exploratory fab runs
  - MPW runs
  - Dedicated fab runs
  - IP and architecture development
- Commercial Access
  - Long Term Access Model

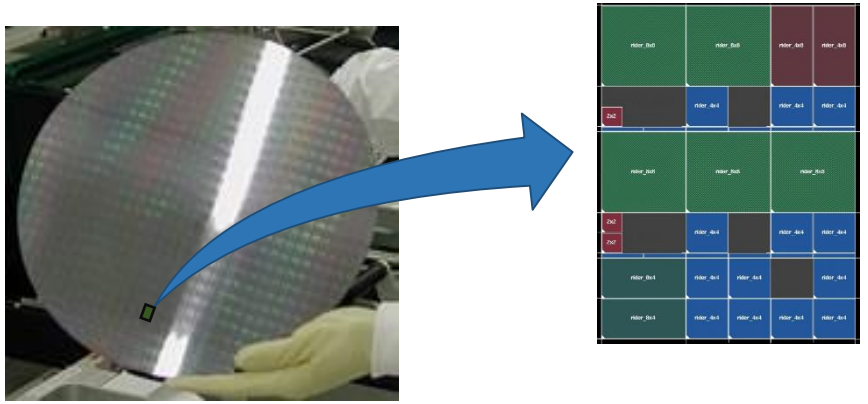
Access to State of the Art Microelectronics

- MPW Coordination
  - Formed a small team meeting ~biweekly
    - Saverio Fazzari and Richard-Duane Chambers – DARPA
    - Brian Dupaix – AFRL
    - Aman Gahoonia – DMEA
    - Morgan Thoma – OSD
    - Others as required
  - Goals
    - Communicate runs
    - Manage riders
    - Mediate space allocation if over-subscribed
    - Manage budget and requested splits
    - Manage schedule
  - Requirements
    - Riders must submit a description of intended design and must describe how it supports the T&AM Program

Front Door Foundry Access
T&AM MPW Access

DMEA - Trusted Access Program Office (TAPO) MPW Program

- Providing guaranteed access to leading-edge Trusted Microelectronics technologies for DoD and the Intelligence Community to support current and future critical system needs.
- Reduces development cost for DoD and the Intelligence Community.



Global Foundries

- ***Access to Global Foundries GF14LPP technology.***
- ***4 MPW runs in FY20.***
- ***~12 riders per run from academia, industry and gov't laboratories.***
- ***Continue runs beyond FY20 based on need.***

Access to Intel 22FFL MOSIS Engagement

Front Door Foundry Access: *Access to SOTA*

This effort ensures access of MINSEC and T&AM users to Intel Corporation's 22FFL IC fabrication process for digital, analog, and RF mixed signal ICs – a State-of-the-Art Process.

22FFL Design Ecosystem Attributes

- High transistor dive currents similar to Intel 14nm.
- >100X leakage power reduction with new ultra-low-power transistors.
- Die area scaling better than other industry's 28/22 nm processes.
- Wide range of advanced logic, analog, and RF devices.
- Use of single patterning for affordable ease-of-design.
- Mature die yield with use of proven 22/14 nm features.
- Design ecosystem (tools, IP, etc.) supported by main-stream companies (ANSYS, Cadence, Synopsys, Mentor, etc.).

FY19-20 Accomplishment:

MOSIS and Intel established an alliance to provide access to Intel's Custom Foundry for 22FFL technology with fabrication run/s planned in FY-2021 time-frame.

Development Highlights:

- Alliance between MOSIS and Intel Corporation in the U.S. represents a significant milestone in progress towards establishing a U.S. source for DoD's advanced microelectronics needs.
- 22FFL technology has broad capabilities for fabrication of digital, analog, and RF mixed signal ICs for a range of applications including 5G, sensors, advanced radar and EW systems, next-generation IoT, and AI/Machine-learning.

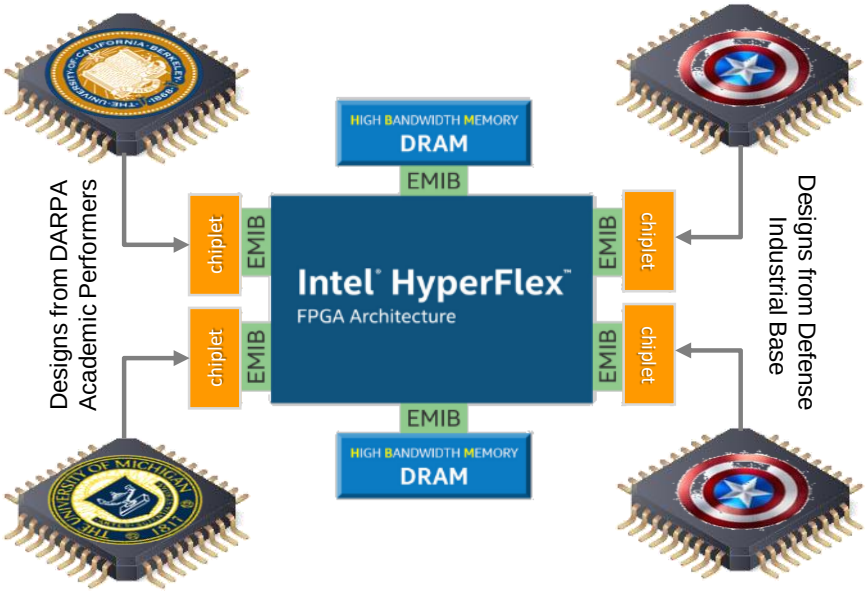
FY-2020 Objectives:

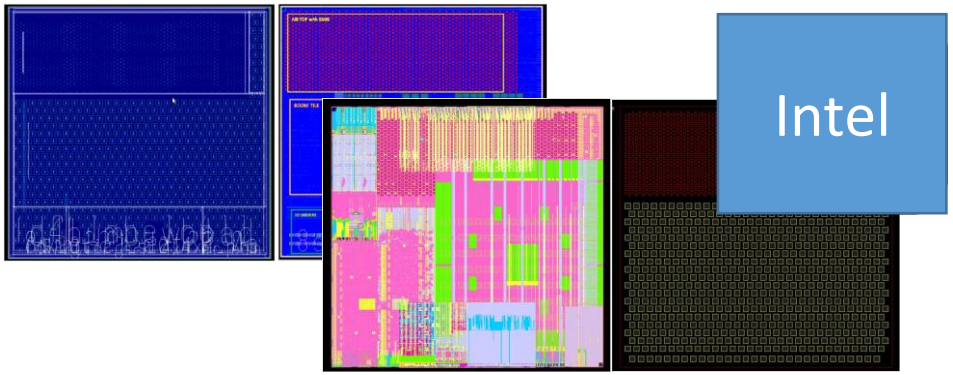
- **Support AFRL/OSD in selecting participants for fabrication run.**
- **Identify opportunities to enhance the MOSIS-Intel infrastructure.**

T&AM Access to SOTA Success

Establishing Access to domestic SOTA Technology

Created new front door access for domestic State-of-the-Art Foundry





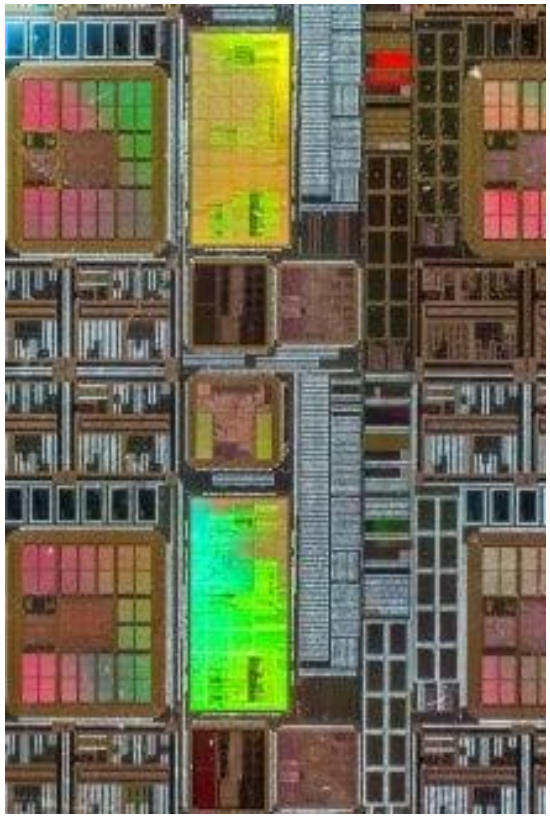
~25 T&AM sponsored designs planned in 1st MPW run

Accomplishments:

- ***Academic designs completed and taped out in 22FFL (HI3)***
- ***DIB partners designing chiplets (HI3)***
- ***Sponsored 1st ever Intel Custom Foundry Multi-Project-Wafer (MPW) Run RFI***

Foundry Access

DARPA & T&AM advanced node fabrication access partnership facilitated multi-project wafers with both research and Defense Industrial Base designs.



Accomplishment:

- ***Provided Global Foundries 14LPP access to: Boeing, Northrup Grumman, Raytheon, MIT-LL, + 7 universities***
- ***Provided Intel 22FFL access to: U. Michigan, U. Berkeley, Northrup Grumman, Draper Labs; (DARPA HI3)***
- ***In process to provide access to Intel 22FFL via MOSIS***
- ***Broadening SOTA development ecosystem***

Agenda – Access to State of the Art Commercial Technology

• Introduction	Morgan Thoma
• Secure Design – Trusted Silicon Stratus (TSS)	Len Orlando
• Front Door Foundry Access	Morgan Thoma
• User Experience	Saverio Fazzari
• Access to GlobalFoundries/TAPO	Aman Gahoonia
• Access to SOTA • Technology Exploration and Engagement	John Damoulakis
• Q&A - Discussion	Panel

The User Experience

Saverio Fazzari

DARPA – Microsystems Technology Office

User Experiences

- DARPA had done research at sub 28 nm for last 5 years
- DARPA has used multiple technologies
  - Global Foundries 14nm/12m
  - TSMC 16nm
  - Intel 22FFL
- Successful tapeouts of 10s of designs from small test chips to one of the large DoD designs ever done
- Multiple new efforts underway

Lessons Learned

- Size of the design matters
- Plan extra time for use of the technology
- Need to learn new ways of doing things
- Communicate with the support team
- What worked in the past will not work now

Proposal Summary
T&AM MPW Program

Rider information

- Name
- Location
- Type of Business
- POC's (PM, Technical, etc.)
- x

How does proposal meet T&AM objectives

x

Proposal Summary

- Proposal overview
- Objective and/or benefits of proposal
- x

Other information

x

Updated Implementation Model

- Timely tracking of riders' schedule status is critical to a successful execution of the run
- Thorough documentation for each run enables accurate records for future reference and MPW process improvement
- Standardization of run information
  - List of Riders and Proposals
  - Reticle layout
  - Parametric data from wafer fab process
- Assess riders design experience early in process
- Formalize documentation and tracking practices
- Maintain lessons learned from each run

Notional MPW Schedule

Legal/Acct/Tech Enablement documents sent
ITAR Plan Established
Initial Design Size mm
14/12 nm Experience?
Design Start Date
Design Progress %
ECCN Submitted
Design Enablement confirmed
Die Size submission
Initial Design Review
ECCN confirmation
Final Design Review
Can submit 2-4 weeks early
Preliminary Design Submission
Final Waiver submission
Last day to change die size
Shuttle Payment due or bump
Last day to cancel reservation
Last day to submit a waiver
Run Close
TAPE IN

Agenda – Access to State of the Art Commercial Technology

• Introduction	Morgan Thoma
• Secure Design – Trusted Silicon Stratus (TSS)	Len Orlando
• Front Door Foundry Access	Morgan Thoma
• User Experience	Saverio Fazzari
• Access to GlobalFoundries/TAPO	Aman Gahoonia
• Access to SOTA • Technology Exploration and Engagement	John Damoulakis
• Q&A - Discussion	Panel

Access to State of the Art Microelectronics Multi-Project Wafer (MPW) program

Aman Gahoonia

Defense Microelectronics Activity

https://www.CTO.mil @DoDCTO

DARPA ERI and T&AM

- Front Door Foundry Access to State of the Art Microelectronics Fabrication Facilities
  - Silicon space available for leading edge nodes at GLOBALFOUNDRIES
  - MPW Coordination
    - Formed a small team, meeting ~biweekly
      - Saverio Fazzari– DARPA
        - Supported w/biweekly GF/DARPA/DMEA milestone interlocks
      - Brian Dupaix – AFRL
      - Aman Gahoonia – DMEA
      - Morgan Thoma – OSD
      - Others as required
    - Goals
      - Communicate runs; Manage riders
      - Mediate space allocation if over-subscribed
      - Manage schedule
    - Requirements
      - Riders must submit a description of their intended design and must describe how it supports the T&AM Program or ERI

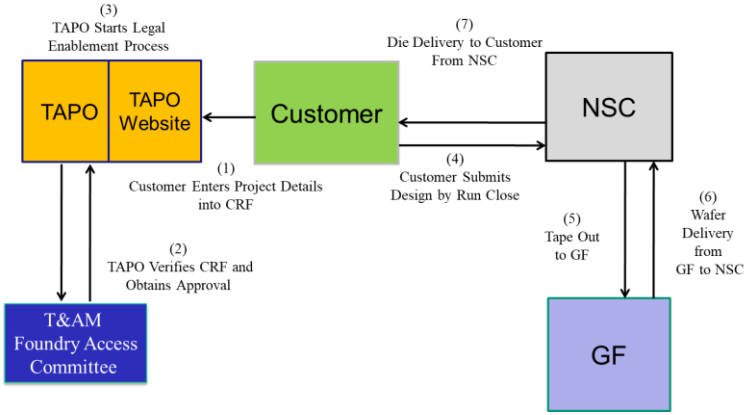
Milestones	T&AM/MINSEC/ERI				
	14LPP 19R2 (GF CS31)	14LPP 20S1 (GF CS39)	14LPP 20TT1	14LPP 20R2	12LP 21R1
Legal/Acct/Tech Enablement	12/08/19	01/17/20	03/18/20	08/03/20	12/18/20
ECCN Submitted	12/22/19	01/31/20	04/01/20	08/17/20	01/01/21
Preliminary Design Submission	02/06/20	03/17/20	04/17/20	10/02/20	02/16/21
Last day to change die size	02/06/20	03/17/20	05/17/20	10/02/20	02/16/21
Last day to cancel reservation	01/21/20	03/01/20	05/31/20	09/16/20	12/01/20
Last day to submit a waiver	03/11/20	04/09/20	06/09/20	10/25/20	03/11/21
Run Close	02/20/20	03/31/20	06/16/20	10/16/20	03/02/21
Interconnect Type (free)	C4	C4	C4	C4	C4
Metal Stack offering	Opt 9	Opt 9	Opt 9	Opt 9	Opt 9

Run Close: DRC clean designs due to KCP, with approved ECCN paperwork and waivers already submited.

Trusted Access Program Office Access

- TAPO Benefits
  - Facilitation of central and rapid contracting for access to processes and parts across the USG
  - Contracts for guaranteed access regardless of project size for the USG
  - Procurement of specialized IP for DoD applications (hardened IP, temperature specs, etc.)
  - Efficient foundry interface and packaging sources available

- TAPO Access at GLOABALFOUNRIES
  - Access to leading edge technologies
    - 45RF-SOI (45nm)
    - 9HP (90nm SiGe)
    - 22FDX (22nm)
    - 12LP (12nm, 14nm)
      - -55C Extended Temp Range
    - 12LP+ (12nm)
      - -55C Extended Temp Range



- TAPO Support/ Designer Mentoring
  - Tech Support / Process Design Kit installation assistance
    - Over 15 years (100's of designs) of ASIC tape in experience with GLOBALFOUNDRIES
    - Run announcement FAQ's
    - PDK Enablement

- Quantifiably Assured Manufacturing
  - Pilot Program at GLOBALFOUNDRIES Fab 8 in Malta, New York

Agenda – Access to State of the Art Commercial Technology

• Introduction	Morgan Thoma
• Secure Design – Trusted Silicon Stratus (TSS)	Len Orlando
• Front Door Foundry Access	Morgan Thoma
• User Experience	Saverio Fazzari
• Access to GlobalFoundries/TAPO	Aman Gahoonia
• Access to SOTA • Technology Exploration and Engagement	John Damoulakis
• Q&A - Discussion	Panel

Security and Access:
" Access to State-of-the-Art Microelectronics with Quantifiable Assurance "
==========

Dr. John N. Damoulakis
University of Southern California – Information Sciences Institute
Sr. Institute Director – Advanced Electronics
703-812-3718; jdamoulakis@isi.edu

Microelectronics Industry Landscape

- Advanced microelectronics fabrication (≤22nm) is dominated by the Asian-Pacific region:
  - TSMC and Samsung are the only worldwide advanced foundries having a full spectrum of technology nodes (90nm – 5nm), and plan to get to 3nm (and beyond) in near future for both digital and analog/digital ICs.
  - Both have a complete IC design, fabrication, and packaging ecosystem.
- U.S. based Intel has excellent advanced technology (<22nm), and is on-track to offer <10nm. Also, recent efforts are underway to open the foundry to industry at large.
- Global Foundries (Malta, NY) offers 12nm CMOS, but no plans to go further.
- U.S. military systems needs:
  - Access of advanced technology nodes is a "must" for U.S. high-value DoD systems.
- Challenges facing DIB (Defense Industrial Base):
  - Uneasiness on using trust-unverifiable, mission-critical, foreign-made electronic ICs.
  - Foundries reluctance to adopt in wafer flows all DoD's directives on "trusted ICs".
  - Non certifiable assurance that ICs manufactured off-shore are trusted.

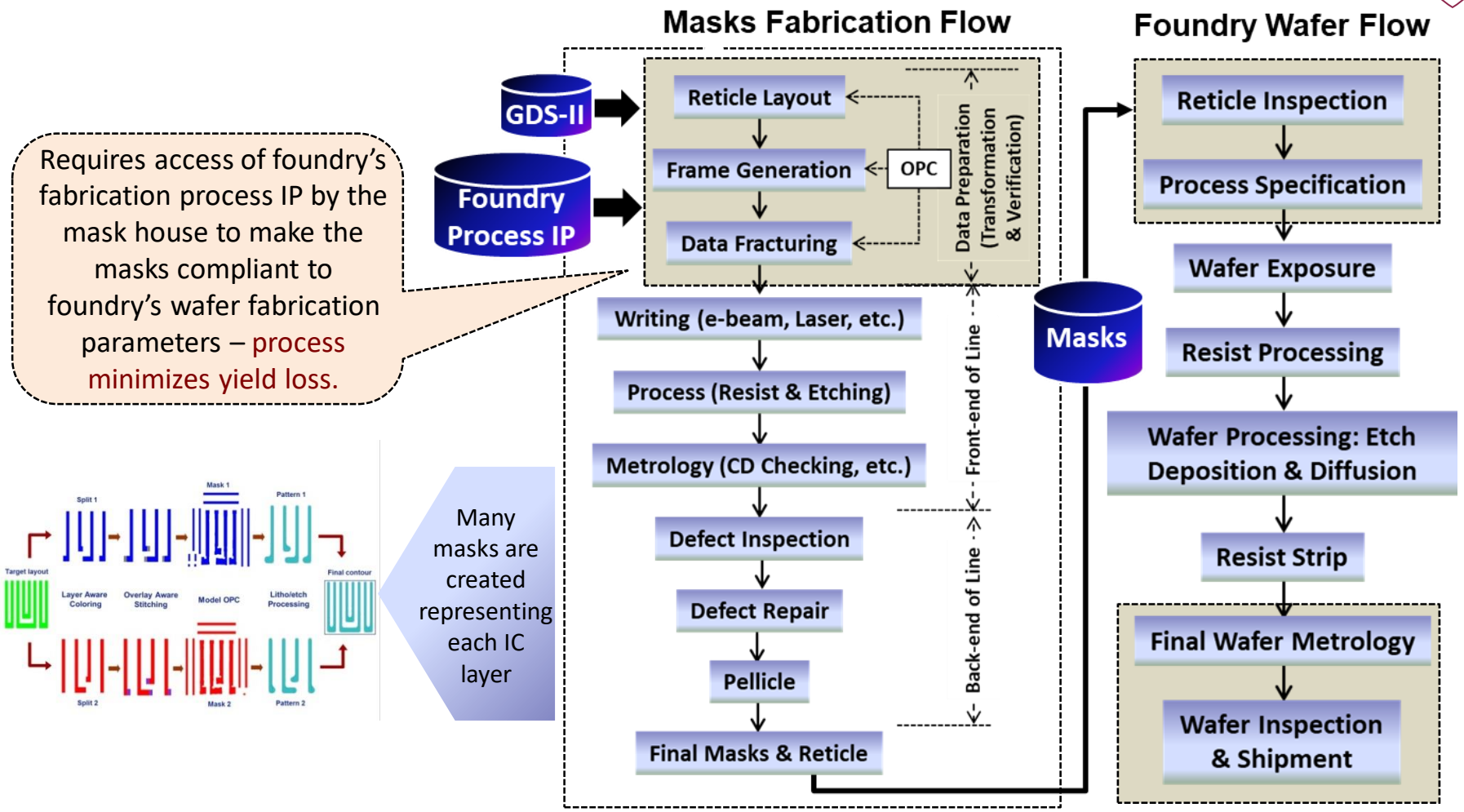
All advanced foundries have well-established, and practiced, verifiable processes to safeguard customers IP. These processes can be tailored to satisfy DoD needs to produce assured ICs with high confidence.

Access and Quantifiable Assurance

- **Access to advanced foundries:**
  - Large companies have always their ways to arrange access to advanced technology.
  - SMEs (Small & Medium Enterprises), Start-ups, and Academia: a) access to advanced technology many times is problematic; b) TSMC and GF have regular MPW shuttles that can be used; and c) MOSIS is a viable alternative with TSMC and GF - also, plans are under-way to offer MPW shuttle services with Intel and Samsung.
- **Quantifiable assurance:**
  - Since 2006 – 2007, DoD has explored many design options to produce trusted ICs.
  - There have been noticeable successes, many of these efforts have generally resulted in the increase of both complexity and cost.
  - With the exception of full foundry-centric trusted flow (e.g., TAPO), all other design approaches do not provide 100% probability of trust.
  - ➢ Foundry-centric trusted flows in advanced foundries (<10nm) are not viable options.

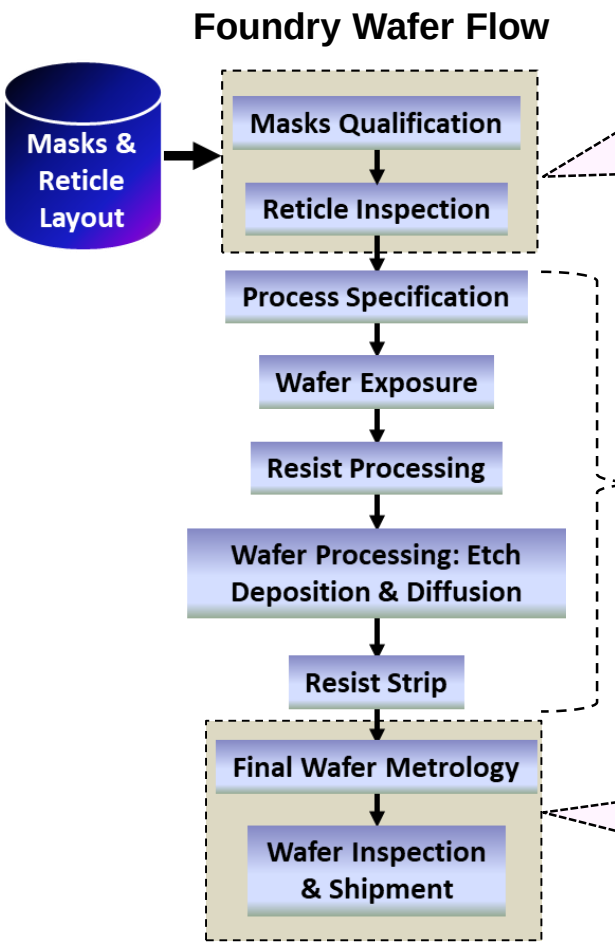
Access to advanced foundries will require new models: a) establish a trust with the foundry; b) no alterations to wafer-flow; and c) use of foundry's processes about authenticity of design IC checks, i.e., it is exactly what customers provide.

A Model for Quantifiable Assurance



A complex process with many steps requiring the very close relationship between the foundry and mask producing entity (foundry reveals its process IP).

Foundry Wafer Flow Vulnerabilities



Key dilemma: can the IC's mask data be compromised?

- Masks layer-by-layer are inspected by foundry personnel.
- Inspection of each mask layer can reveal information and data to an untrusted person to re-create the IC design.
- Remedies: a) a USG-trusted person can oversee the operations, while the flow proceeds "as is"; b) derived data can be stored in a secure media; and c) mask house, if separate from foundry, can perform these operations instead of foundry.

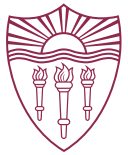
➢ USG & foundry can reach a mutually agreeable assured process.

Altering IC's circuitry is not practical, but an IC can be made inoperable ➡ metrology will identify root-cause of the problem

- Information/data can be obtained revealing IC's design and/or functionality.
- Remedies: either a USG-designated person oversees the process and has cognizance and control of the data, or USG receives the wafers and performs the metrology in a USG-accredited entity.

In cooperation with foundry, a revised process can be established to produce "assured ICs" without altering the pre-arranged foundry's established wafer flow.

Concluding Remarks



- DoD needs regular access to advanced foundries to develop next generation military systems with emerging technologies (AI, ML, etc.).
- The usual foundry-centric trusted model appears to be difficult to implement in the current landscape of advanced foundries – new models and approaches must be thought.
- Establishing "trust" between DoD and advanced foundries is essential; also, many lessons can be leaned from foundry's existing practices, which, if tailored to DoD needs, can provide acceptable assured ICs.
- Not every possible vulnerability can be handled, but it appears that key vulnerabilities during mask generation and fabrication can be mitigated.
- Advanced foundries are reluctant to divulge process IP to any outside source; thus, models need to be thought to overcome these sensitivities (e.g., OPC performed by foundry personnel approved by USG).
- If successful, this approach holds promise to yield assured ICs with an acceptable level of confidence at prices of commercial settings.

Agenda – Access to State of the Art Commercial Technology

• Introduction	Morgan Thoma
• Secure Design – Trusted Silicon Stratus (TSS)	Len Orlando
• Front Door Foundry Access	Morgan Thoma
• User Experience	Saverio Fazzari
• Access to GlobalFoundries/TAPO	Aman Gahoonia
• Access to SOTA • Technology Exploration and Engagement	John Damoulakis
• Q&A - Discussion	Panel

Agenda – Access to State of the Art Commercial Technology

Q&A -

Discussion