Trusted and Assured Microelectronics Program

Create a Robust and Resilient Pipeline

SLIDES ONLY
NO SCRIPT PROVIDED

Matthew Casto, Ph.D.
Program Director, Trusted and Assured Microelectronics

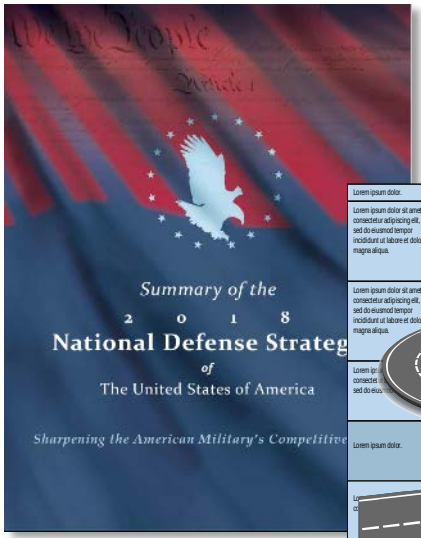
DARPA ERI Summit

August 2020

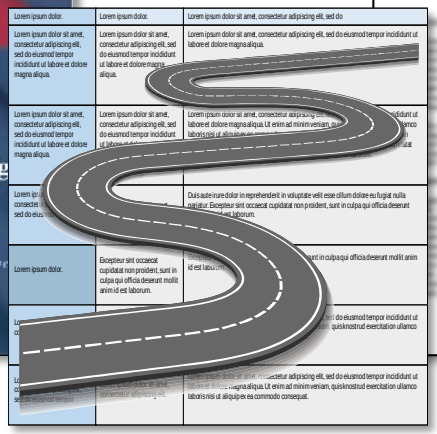
https://www.CTO.mil *@DoDCTO*

Strategic Guidance

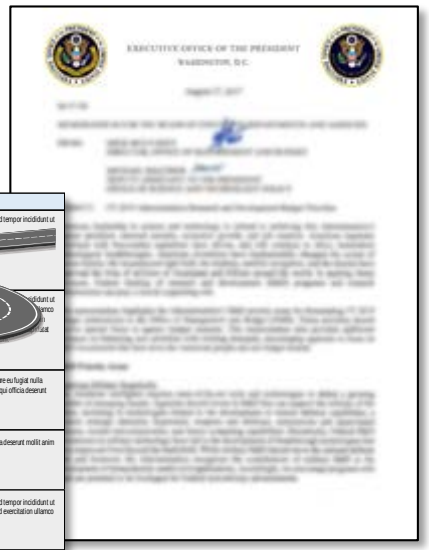
2018 National Defense Strategy



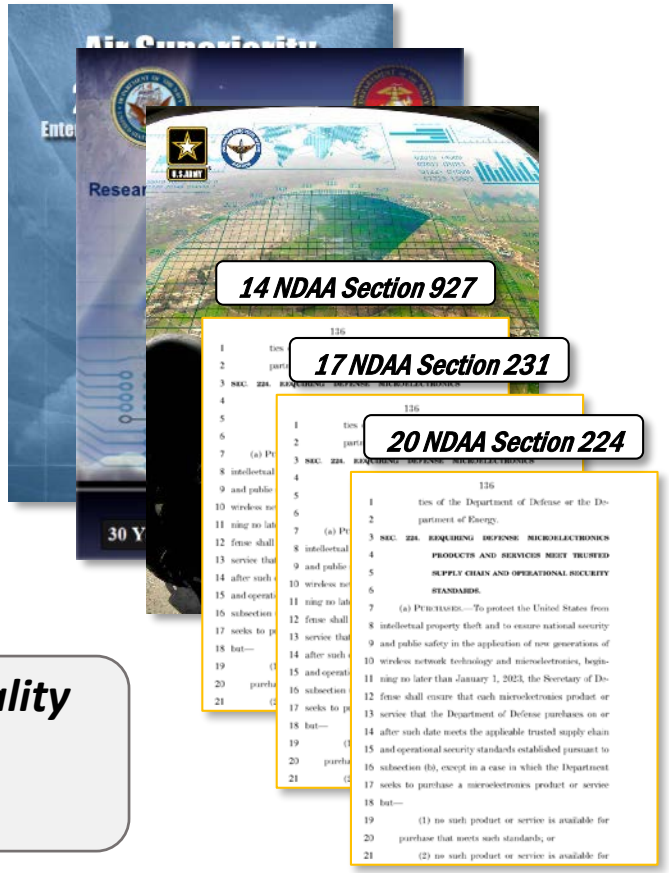
Microelectronics Roadmap



FY19 OMB/OSTP



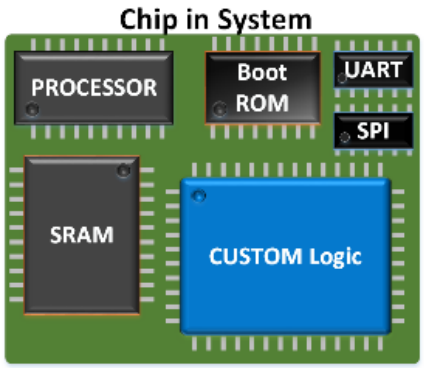
Service2030+

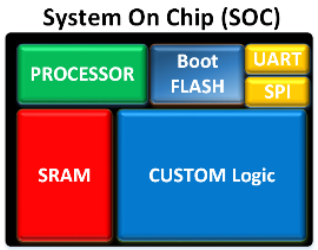


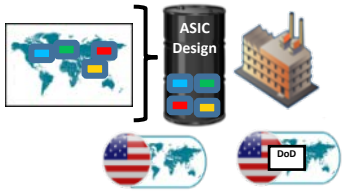
Drive reformation and Form Alliances to Enhance Lethality
Promote, Protect, Partner
Modernization priorities to rapidly create advantage

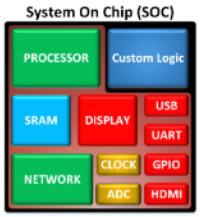
Microelectronics is DoD's Top Modernization Priority!

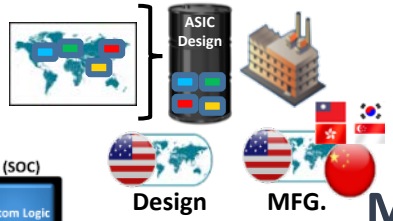
Assured Microelectronics Evolution

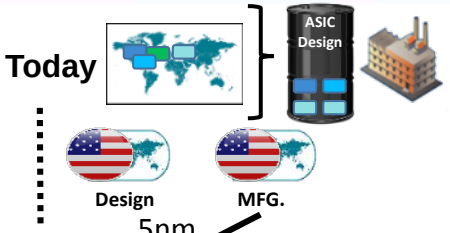


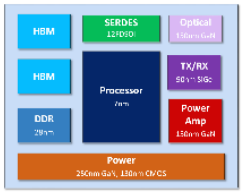


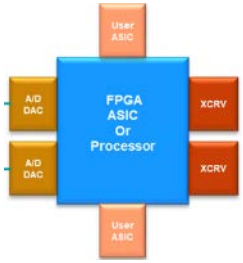












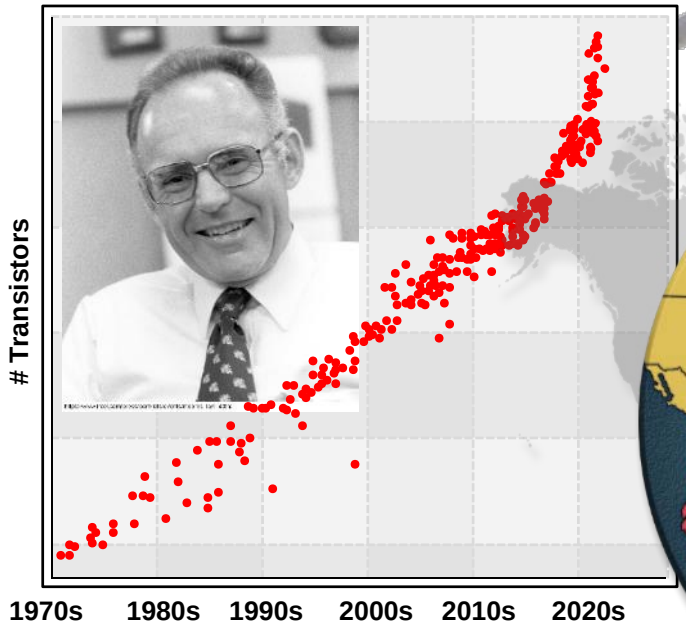
MINSEC – Microelectronics Innovation for National Security and Economic Competitiveness
T&AM – Trusted & Assured Microelectronics
TAPO – Trusted Access Program Office
SEMATECH – Semiconductor Manufacturing Technology
MIMIC – Microwave/Millimeter Monolithic Integrated Circuits
VHSIC - Very High Speed Integrated Circuits

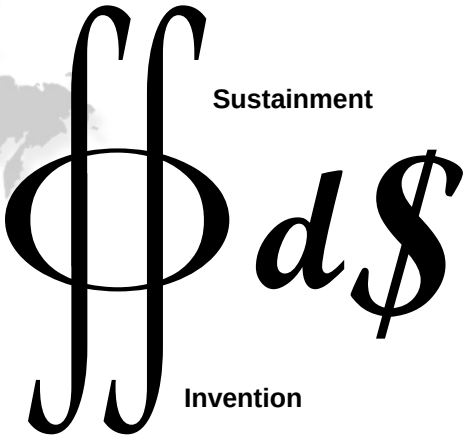
T&AM/MINSEC Program is developing the secure ecosystem to assure SOTA performance for Modernization

Microelectronics Landscape

Joint Strike Fighter uses 100+ different process IP

Risk





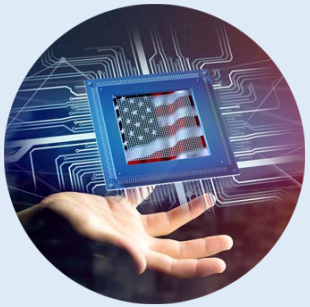
Specialization of Electronics – Risk in Global Supply – Changing the Lifecycle Speed & Cost Efficiency

Trusted and Assured Microelectronics Strategic Approach

Microelectronics - DoD's Top Modernization Priority

We cannot expect success fighting tomorrow's conflicts with yesterday's weapons or equipment.

-National Defense Strategy

	 **Access to State of the Art Commercial Technology**	 **Data Driven Quantifiable Assurance**	 **Address DoD Unique Needs**	 **Create a Resilient and Robust Pipeline**
Gaps:	DoD lags commercial CMOS ecosystem/ infrastructure	Threats to design and manufacturing in global supply chain	Increased sources for national strategic defense	Domestic and Allied Ecosystem to rapidly and securely mature emerging advanced technology
Approach:	Establish best practices for secure design, assembly, packaging, and test capabilities to support DIB and co-development of dual use electronics	Secure full lifecycle confidentiality, Integrity, verification & validation, and supply chain for assured warfighters electronics	Develop sustainable sources of mission essential niche rad-hard electronics capabilities, and specialized radio frequency and electro-optic components	Invigorate secure pipeline for disruptive R&D transition, supply chain aware technology development, education and workforce.

Current T&AM Challenges

- Lower barriers to specialization and innovation in advanced IC technologies; Tools, Intellectual Property, Fabrication
- Attract, recruit and retain talented STEM workforce with knowledge of DoD-specific challenges
- Identify & mitigate supply chain threats to improve assurance & resilience of microelectronics
- Rapidly mature, co-develop, and transition new and emerging technologies with assurance and security for program adoption

Create a Resilient and Robust Pipeline

Invigorate secure pipeline for disruptive R&D transition, supply chain aware technology development, education and workforce.

DARPA

Innovation Accelerators

- *Engage with non-traditional technology sources to cultivate a SOTA microelectronics ecosystem, built on a foundation of assurance*
- *Technology for DoD Asymmetric Advantage*
- *DoD Asymmetric Advantage; Sustainable US company*

NAVY

Education and Workforce Development

- *Outreach to universities to develop US-based semiconductor-focused education pipelines; Semiconductor Fab, Security/Assurance, Design, Package, and Test*
- *Education and Training for DoD and DIB*

NAVY

Supply Chain Awareness and Security

- *Addressing security to risk supply chain through tech development, V&V, and CI awareness ; Briefings to DIB partners and industry*
- *Improve Supply Chain Awareness*
- *Intelligence prep of the Battlespace*
- *Counterintelligence Execution*

U.S.ARMY

Technology Development

- *Leverage SOTA commercial technology to co-develop assured solutions*
- *Adapt SOTA technology to enable DoD Unique solutions*
- *Accelerate on shore availability and development for adoption in DoD PoR*
- *Compute Platforms, Domain Specific Tech, Supply Chain Solutions, Programmable Logic*

Program* Development & Capabilities → **PPP*/ CPI** → **Design** → **Verify** → **Mask** → **Fabrication** → **Pack. & test** → **Verify & validate** → **Config./ prog. SW** → **Integrate & test** → **Operation & maint.**

T&AM: Create a Robust and Resilient Microelectronics Pipeline Panel Agenda

- 1415 - 1435 Introduction
  - Dr. Matthew Casto, T&AM Program Director
- 1425 – 1600 Education and Workforce Development Consortium Panel
  - Allison Smith, Naval Surface Weapons Center – Crane, T&AM Technical Execution Lead
  - Panel Members NSS IECRC, Universities Cincinnati, Purdue, Florida and Ohio
- 1600 - 1615 AFTERNOON BREAK
- 1615 - 1645 OSD and AF Microelectronics Design and Prototype Challenge
  - Vipul J. Patel, AFRL, Sr. Electronics Engineer
- 1645 – 1715 Technology Development
  - Peter O'Donnell, Army Combat Capabilities Combat Command, T&AM Technical Execution Area
- 1715 – 1745 Supply Chain Awareness and Security
  - Adam Hauch, Naval Surface Weapons Center – Crane, Technical Execution Area Lead
- 1745 – 1845 Virtual Demo & Poster Session

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ELECTRONICS RESURGENCE INITIATIVE
ERI SUMMIT
& MTO Symposium
2020 Seattle, WA August 18-20

Education & Workforce Development Panel

Session: Trusted and Assured Microelectronics (T&AM): Create a Resilient and Robust Microelectronics Pipeline

Panel Discussions - Housekeeping

- **If you have non-technical issues, please contact the CO-HOSTS identified as FACILITATORS**
- **All conversations must remain at Distribution A level (no classified, FOUO, CUI, etc.)**
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      - **Wireless Connection Issues: https://support.zoom.us/hc/en-us/articles/201362463-Wireless-WiFi-Connection-Issues**
    - **Connect with the ERI Team desk via the 6Connex platform**

Dr. Alison Smith

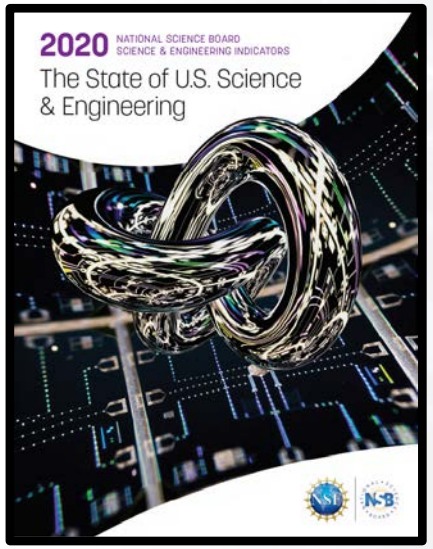
NAVAL SURFACE WARFARE CENTER, CRANE DIVISION (NSWC CRANE)

Mr. Len Orlando

AIR FORCE RESEARCH LABORATORY (AFRL)

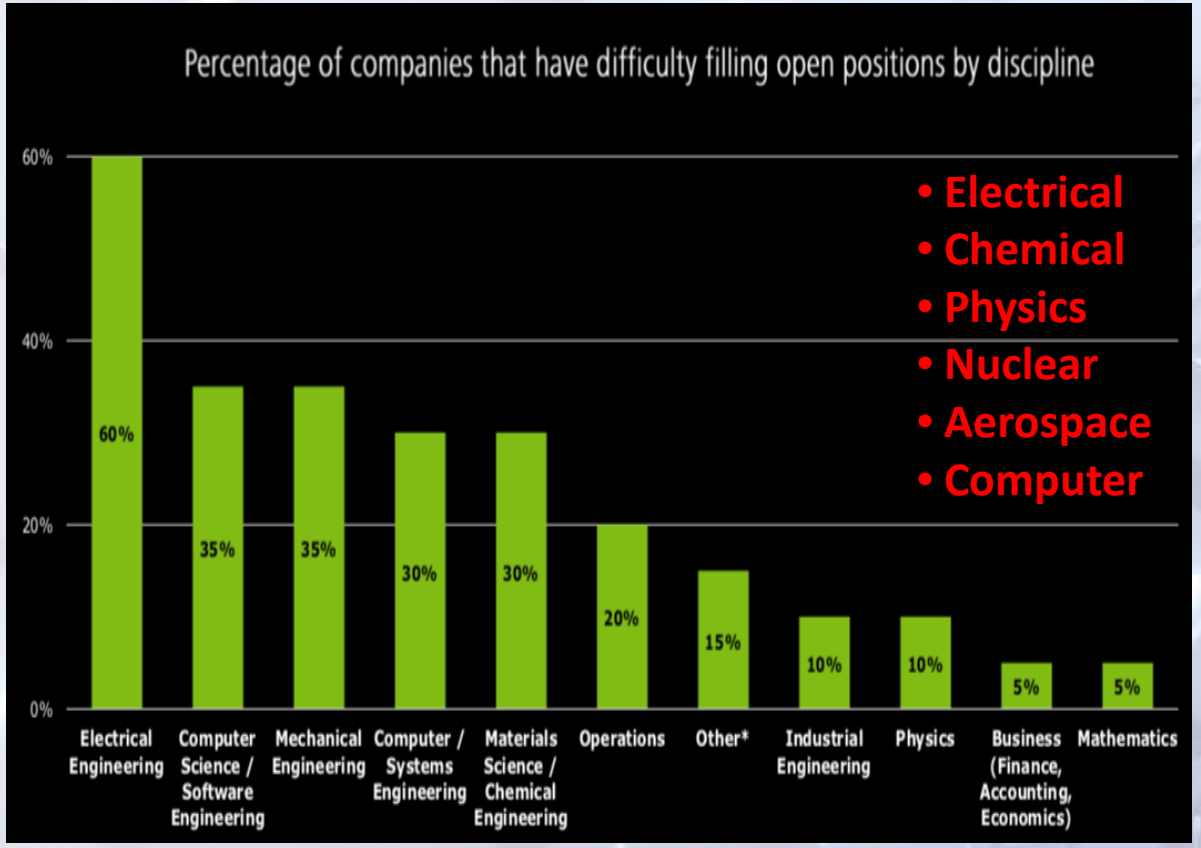
T&AM EDUCATION & WORKFORCE DEVELOPMENT EXECUTION CO-LEADS

The War for Talent



T&AM STEM Discipline Needs

- Lowest overall student representation
- Largest influx of international students



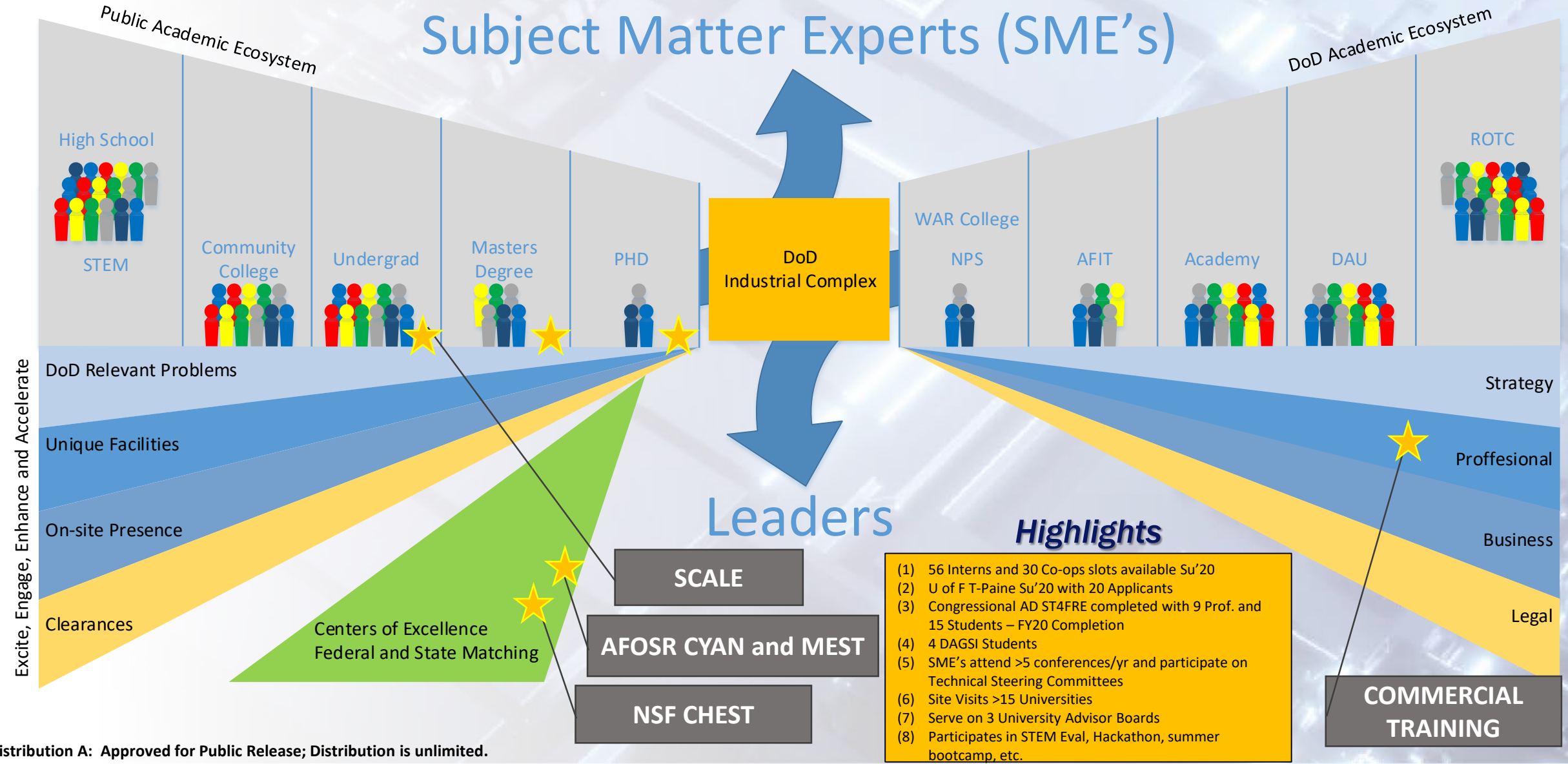
Source: Engineering Talent Shortage Now Top Risk Factor, Semiconductor Engineering, Deloitte Survey, Feb. 25, 2019

"As much as emerging technologies will define future conflict, ***the war for talent will likely play the central role*** in the outcome of long-term technological competition.

The National Security Innovation Base (NSIB) struggles to attract, recruit, and retain a workforce willing and able to tackle tough challenges and find innovative solutions. Universities are confronting a dearth in American talent generation and retention."

T&AM Has Unique Interdisciplinary Needs Within A Competitive STEM Market

T&AM Education & Workforce Development



Highlights

(1) 56 Interns and 30 Co-ops slots available Su'20
(2) U of F T-Paine Su'20 with 20 Applicants
(3) Congressional AD ST4FRE completed with 9 Prof. and 15 Students – FY20 Completion
(4) 4 DAGSI Students
(5) SME's attend >5 conferences/yr and participate on Technical Steering Committees
(6) Site Visits >15 Universities
(7) Serve on 3 University Advisor Boards
(8) Participates in STEM Eval, Hackathon, summer bootcamp, etc.

Education & Workforce Development Panel

- **Prof. Marty Emmert**, NSF IUCRC CHEST (Center for Hardware and Embedded System Security and Trust)
- **Prof. Mark Tehranipoor and Prof. Waleed Khalil**, AFOSR MEST/CYAN (The National Microelectronics Security Training Center and the Center for Enabling Cyber Defense in Analog and Mixed Signal Domain)
- **Dr. Praveen Chawla**, Edaptive Computing Inc.
- **Ms. Cheyanne Harshman**, Centauri Corp.
- **Prof. Peter Bermel**, SCALE (Scalable Asymmetric Lifecycle Engagement)
- **Prof. Carolyn Goerner**, Best Practices in Talent Management

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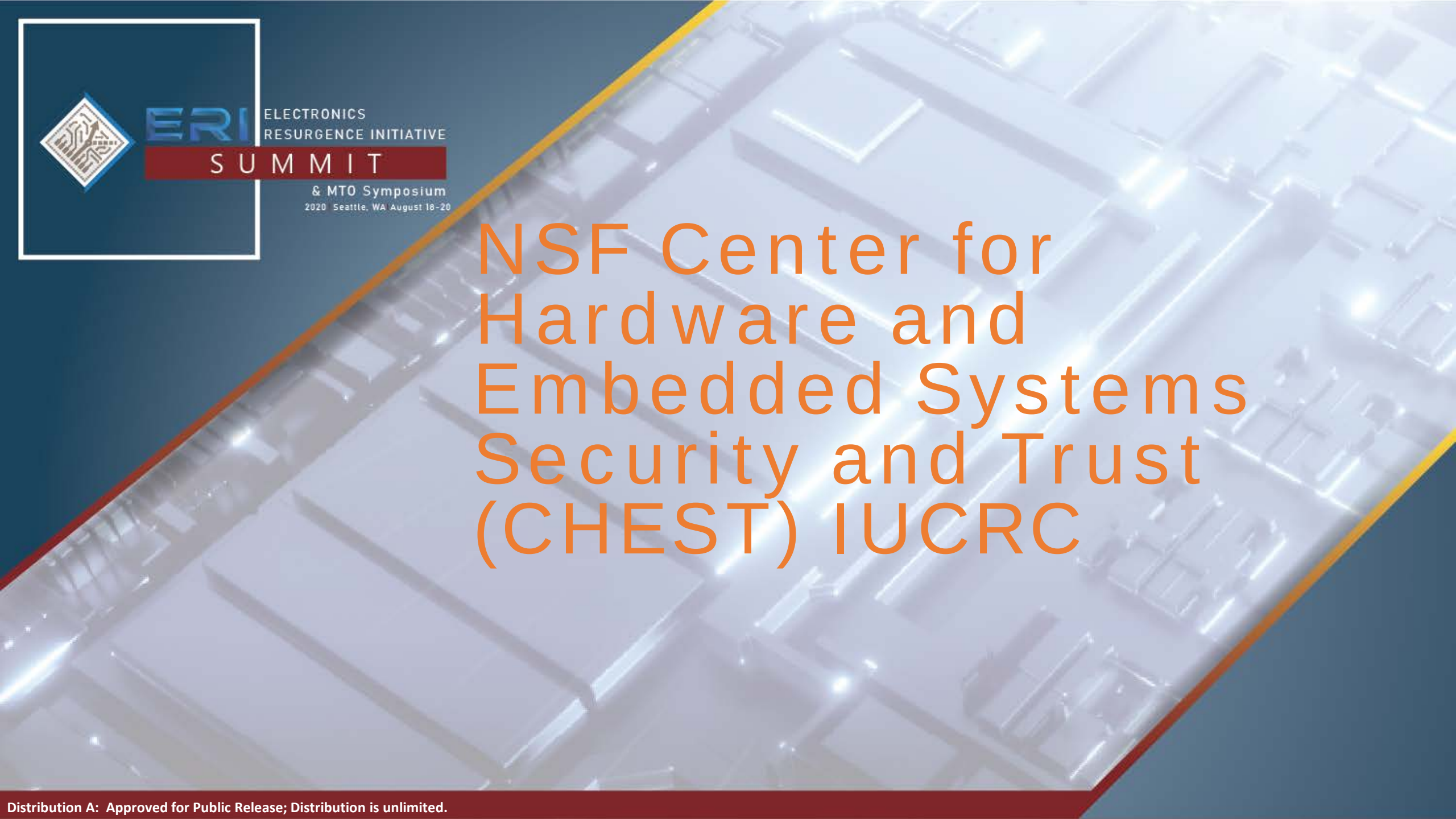


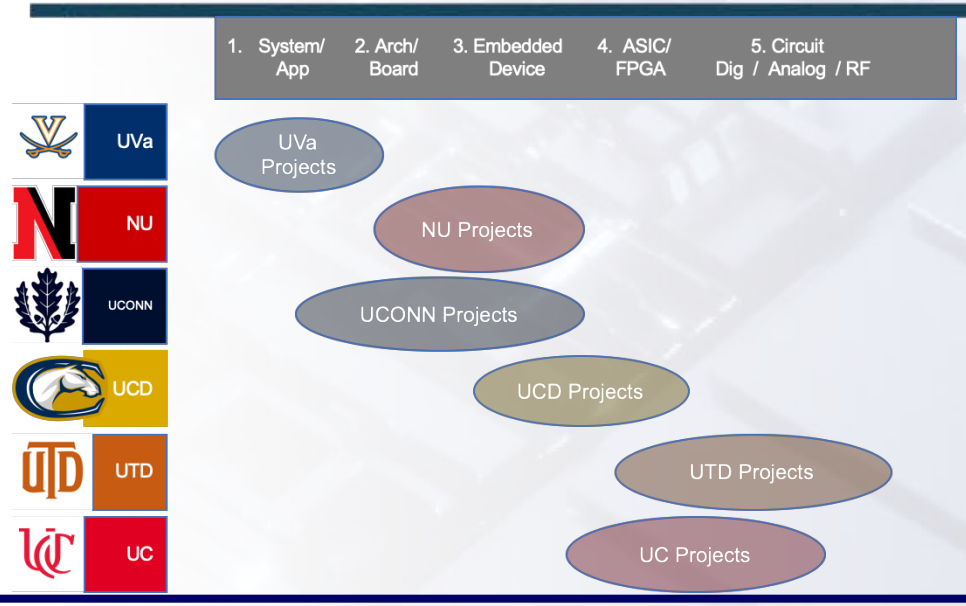
NSF Center for Hardware and Embedded Systems Security and Trust (CHEST) IUCRC

John (Marty) EMMERT

PROFESSOR, UNIVERSITY OF CINCINNATI
DIRECTOR, CHEST IUCRC

NSF CHEST IUCRC

CENTER FOR HARDWARE AND EMBEDDED SYSTEMS SECURITY AND TRUST



Funding Overview & Key Partnerships

POC: Dr. J. M. Emmert (Marty), University of Cincinnati
email: John.Emmert@uc.edu
Mr. Luis Concha, University of Cincinnati
Email: Luis.Concha@uc.edu

	2020	2021	2022	2023	2024
Fee	$50k	$50k	$50k	$50k	$50k

Requirements: Membership Support, IAB Oversite, Data
IAB Leads: Len Orlando and Brian Dupaix, AFRL
CHEST Team: Marty Emmert, Director (UC), Houman Homayoun (UC Davis), Yunsi Fei (NU), John Chandy (UCONN), Yiorgos Makris (UTD), James Lambert (UVa)

Description of Project and link to T&AM Mission

- Coordinates university-based research with needs of industry and government partners to advance knowledge of microelectronic security, assurance, and trust (SAT)
- Identification, detection, monitoring, mitigation, and elimination of vulnerabilities that affect electronic hardware and embedded systems

How is this better than current SOTA

- With industry oversite, the CHEST Center addresses a range of attack vectors across design, operation, manufacturing, supply chains, and integration of the HW, SW, and firmware
- Limited 10% overhead: 90% of all funds go directly to research
- Minimal time required to get projects “on contract”
- Educating the next generation of experts
- Collaborative environment: DoD / Industry / NSF / Academia

Approach

- Technical: The NSF CHEST Center addresses security, assurance, and trust across several levels: Large-scale systems, embedded systems, design and operations, requirements, standards, manufacturing, supply chains, and integrated circuits and boards.
- Contract: Vehicle: MIPR (DoD) or Check (Industry)
  https://www.nsf.gov/eng/iip/iucrc/government.jsp
  https://www.nsf.gov/eng/iip/iucrc/iaainstructions.jsp

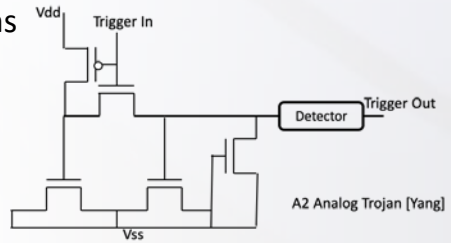
Benefits / Deliverables

- Monthly / Quarterly / Annual Reports and Updates
- Royalty free access to IP: Standard NSF IUCRC MOU
- HW / SW / Testbed Demonstrations
- WF Development: Next generation of SMEs in the area of Security, Assurance and Trust for Electronic HW and Embedded Systems

2020 CHEST Inaugural Projects

What types of problems does CHEST address?

- Any basic or applied research related to **SAT**
- SCA: detection, prevention, mitigation
- Trojan: detection, prevention, mitigation (eg. =>)
- Reverse engineering: ASIC (physical - destructive/nondestructive) and FPGA bitstreams
- Integrated circuit and silicon authentication
- Anti Tamper: detection, prevention, mitigation
- Countermeasure design / methodologies
- PUFs (physical unclonable functions)
- Intellectual Property: protection, anti-cloning, anti-counterfeiting, over-manufacturing, piracy etc.
- Assessment: metrics for levels of TRUST
- Embedded algorithm protection
- Legacy systems
- Etc.



P1_20: Asynchronous Design for Side Channel Avoidance ($100K); **J. M. Emmert (john.emmert@uc.edu)**, Ranga Vemuri (UC)

P2_20: Connectionless RFID based Secure Supply Chain Management ($50K); **Marten van Dijk (marten.van_dijk@uconn.edu)**, Ulrich Ruhrmair (UConn)

P3_20: Reverse Engineering Methodology for FPGA Bitstreams ($100K); James H. Lambert (UVa), Zachary Collier, **J. M. Emmert (john.emmert@uc.edu)**, Carla Purdy (UC)

P4_20: Additive Components for Hardware Integrity Monitoring ($100K); **Rashmi Jha (jhari@ucmail.uc.edu)**, Marc Cahay, Punit Boochand (UC)

P5_20: Cost-Effective Resource Allocation to Portfolios of Security Measures for Embedded Devices in a Large-Scale System ($25K); **James H. Lambert (jhl6d@virginia.edu)**, Dr. Zachary A. Collier, Mr. Thomas A. Polmateer (UVA)

P6_20: Trusted Enterprise Communications and Cyber-Physical Integration of Advanced Fleet Electrical Vehicle Chargers in a Mobile Electric Grid ($95K); **James H. Lambert (jhl6d@virginia.edu)**, Dr. Zachary A. Collier, Mr. Thomas A. Polmateer (UVa)

P7_20: CAD Flow Development for Design Obfuscation through Post-Fabrication Transistor-Level Programming (TRAP) ($100K); **Yiorgos Makris (yiorgos.makris@utdallas.edu)**, Carl Sechen, Benjamin Carrion Schaefer, William Swartz (UTD)

P8_20: Design Obfuscation and Performance Locking Solutions for Analog/RF ICs ($75K); **Yiorgos Makris (yiorgos.makris@utdallas.edu)**, Ken O, Andrew Marshall (UTD)

P9_20: Formal Security Evaluation of Executing Untrusted Binaries on Embedded Processors ($50K); Kevin Hamlen, **Yiorgos Makris (yiorgos.makris@utdallas.edu)** (UTD)

P10_20: Stochasticity, Polymorphism and Non-Volatility: Three Pillars of Security and Trust Intrinsic to Emerging Technologies ($50K); Joseph Friedman, **Yiorgos Makris (yiorgos.makris@utdallas.edu)** (UTD)

P11_20: Secure Design by RISC-V Framework ($70K); **Yunsi Fei (yfei@ece.neu.edu)**, David Kaeli (NU)

P12_20: Current Sensing Based On-chip Analog Trojan Detection Circuit Compatible with Chip Design and Validation Flow ($50K); **Aatmesh Shrivastva (aatmesh@ece.neu.edu)**, Yunsi Fei (NU)

P13_20: Cognitive Obfuscation: Securing Circuits by Graph Convolutional Networks ($100K); **Houman Homayoun (hhomayoun@ucdavis.edu)** (UC Davis), Venkatesh Akella (UC Davis)

P14_20: A Neural Network Assisted Timing Profiling for Hardware Trojans Detection ($75K); **Houman Homayoun(hhomayoun@ucdavis.edu)** (UC Davis)

P15_20: Embedded Systems Anti-Reverse Engineering using Transient Electronics ($50K); Lei Wang, **John Chandy (john.chandy@uconn.edu)** (UConn)

P16_20: Leveraging Hardware Isolation for Secure Execution of Safety-Critical Applications in Distributed Embedded Systems ($50K); **Omer Khan (khan@uconn.edu)** (UConn)

Waleed KHALIL

PROFESSOR – OHIO STATE UNIVERSITY
CO-DIRECTOR OF CYAN AND MEST CENTERS OF EXCELLENCE

Center of Excellence for Cyber Defense in the Analog and Mixed Signal (AMS) Domain (CYAN)

Research Program & Team

- Strong & diverse expertise in hardware security, AMS design, fabrication, test, electromagnetics, applied cryptography, machine learning and data analytics
- Holistic research approach in securing the design, fabrication, and operation of AMS technologies and analog emissions

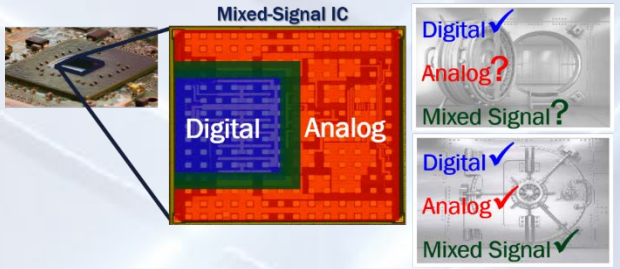
Education & Capacity Building

- New generation of workforce exposed to multidisciplinary environment of modern-day scientific research
- Target 20 PhD/MS students + 20 undergraduates (50% US)
- 18 PhD/MS students currently affiliated with the center: 11 receive direct CYAN funding and 7 from external sources (10 US students in total)

Government & Industry Partnership

- Consortium-led cooperation with national labs, commercial and defense industry
- Grow research funding to sustain CYAN beyond 5 years
- Leverage add'l funding to amplify the research: 1 funded project/ 5 pending

CYAN Thrust 1: Securing AMS Devices & Systems



- AMS Security Primitives
- AMS Obfuscation
- AMS Counterfeit & Trojan Detection/Prevention
- Analog Enabled Cryptography
- Securing Power Supplies

CYAN Thrust 2: Exploiting Analog Emanations for Cyber Defense

- RF and Process Authentication
- Electromagnetic Signatures from AMS Devices
- Program Analysis via Side-channel Signals
- Side Channel Assessment

Mark TEHRANIPOOR

INTEL CHARLES E. YOUNG ENDOWED CHAIR PROFESSOR – UNIVERSITY OF FLORIDA

DIRECTOR FOR FICS RESEARCH, CO-DIRECTOR FOR CYAN AND MEST CENTERS OF EXCELLENCE

MEST: National MicroElectronics Security Training Center

Research Program & Team

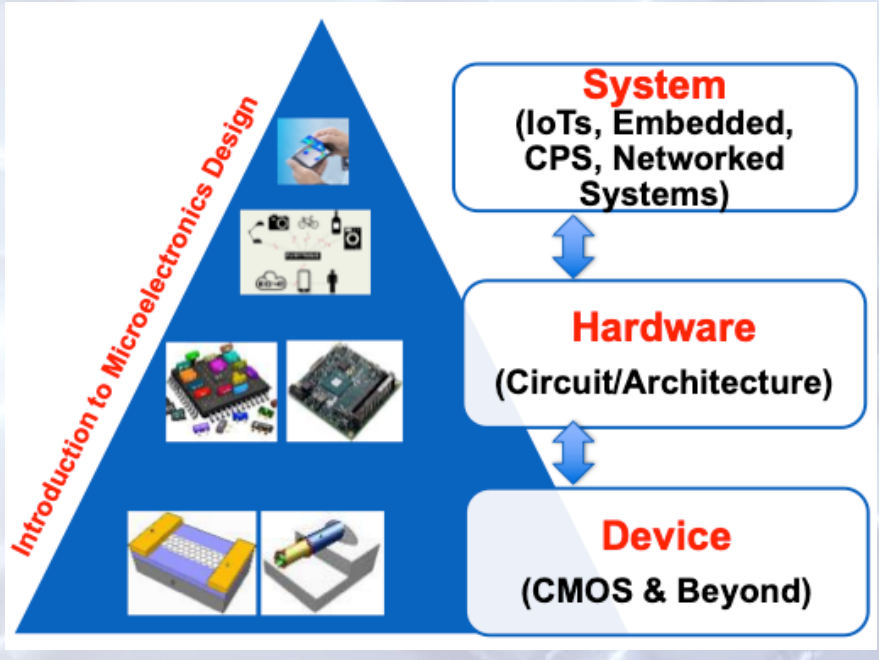
- Increasing demand for well-trained cybersecurity workforce in all government agencies, national labs, and industry sectors!
- MEST offers a comprehensive training effort in microelectronics security is a critical need
- Outstanding team of faculty and industry practitioners offering webinars, long, and short courses

Education & Capacity Building

- New generation of workforce exposed to multidisciplinary environment of modern-day scientific research
- Total attendees (Webinar + Certificate Trainings): **2000+**
- 16 webinars, 8 trainings, and 5 online courses developed so far

Government & Industry Partnership

- Develop and provide free training programs on microelectronics design and security to the Government and Defense Industrial Base
- We plan to establish a consortium of companies sponsoring MEST in the future



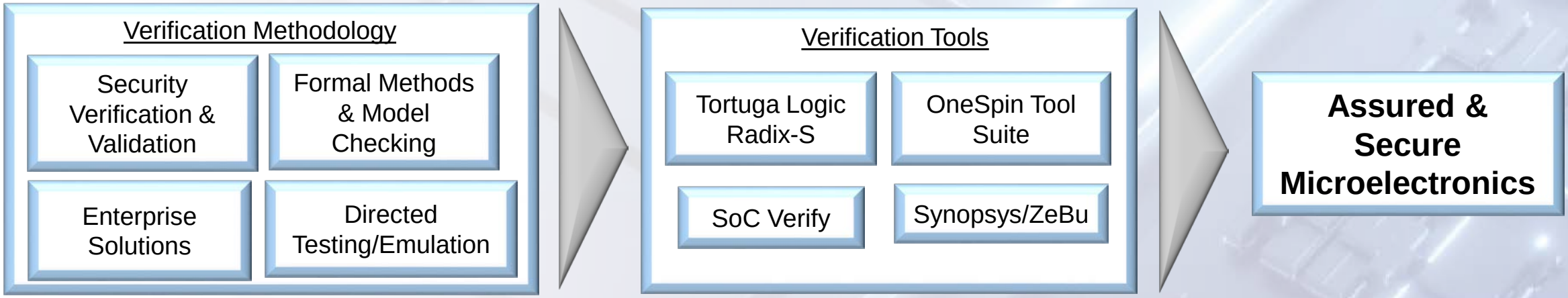
- Cybersecurity Case Studies
- Secure Architecture Design
- Automotive Security
- Cross Layered Systems Security
- Introduction to IoT Security
- Asynchronous Design Practices for Secure Hardware
- Introduction to Hardware Security and Trust
- Secure Architecture Design
- Physical Inspection
- Hardware Security Lab
- Advanced Topics in Hardware Security and Trust
- Physical Inspection
- Introduction to AMS Security

Praveen CHAWLA

PRESIDENT/CTO
EDAPTIVE COMPUTING, INC.

- **Workforce Development Goals:**
  - Transition students and industry professionals into the hardware security workforce for government agencies, national laboratories and industry sectors
  - Apply automation tools to ease transition and increase efficiency of workforce entry into verification engineering for assuring and securing microelectronics
- **Workforce Development Architecture:**
  - Holistic and integrated approach to both train the next generation of hardware security engineers and develop comprehensive, enterprise tools and solutions for assured and secure microelectronics

Application Engineer Training:



Technical Transition:

University of Florida:	University of Cincinnati:	Edaptive Computing:	DARPA IDEA/POSH:

• FICS SoC Trust & Validation (STV)
• FICS AutoBOM – Automatic Bill of Materials for PCB
	• Memometer – Generation and interrogation of a digital signature of an FPGA/ASIC/PLD
	• FACETS – Formal Assertions and Security Monitoring for Trusted SoCs
		• SoC Verify – Enterprise Verification Management
		• Synopsys Emulation accessible and enabled through cloud
			• Support ZS3 Emulation
			  • University of Michigan
			  • Princeton University
			  • Washington University

Current Workforce Training Numbers:

Active Accounts on TSS:	OneSpin Trainees:	Radix-S Trainees:	Synopsys Tools Trainees:
108	96	24	17

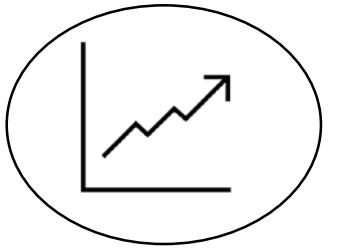
Current 2020 OneSpin Training Schedule:

Class:	Date:
Online OneSpin EC Course	August 5th
Online OneSpin FIA/FPA Course	August 19th
Online OneSpin 360 DV Apps Course	September 9th
Online OneSpin ABV & MDV Course	October 7th
Online OneSpin EC Course	October 28th
Online OneSpin 360 DV Apps Course	November 4th
Online OneSpin FIA/FPA Course	November 18th
OneSpin 3-Day Intro Course (ECI)	December 15th – 17th

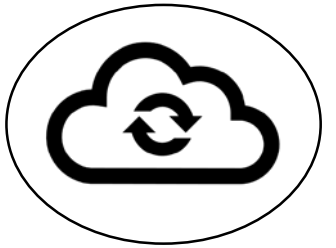
- **Online Tortuga Logic Radix-S Training Class:**
  - 1st Class: July 2020
  - Additional Classes: September-October 2020
- **OneSpin/ECI Formal Verification Certification Intro Training Class**
  - September 2020
- **Synopsys Verdi and ZS Platform Training**
  - Fall 2020

Success Checks:

Training Program Certification



Track Student Training Attendance



Tool Usage in Cloud Environment

Technical Support Services

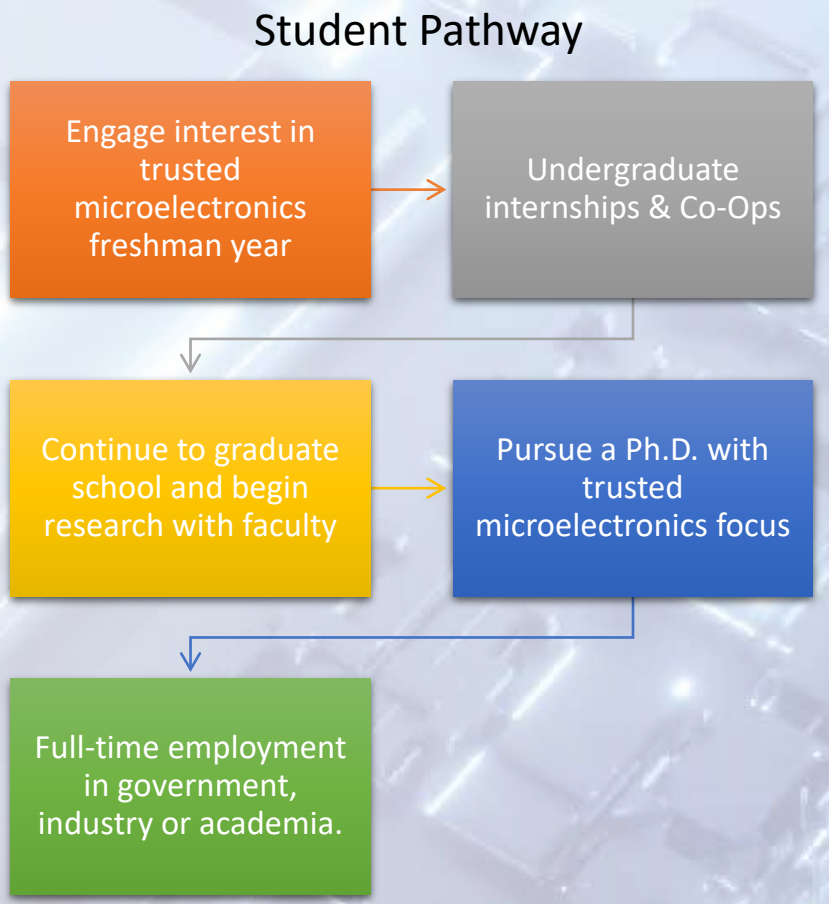
For Education & Workforce Development Panel: Centauri Educational Outreach and Partnerships

Cheyanne HARSHMAN

CENTAURI
WORKFORCE DEVELOPMENT LEAD

University Engagement

- Centauri is focused on creating a national approach to interacting with universities and additional academic institutions to engage undergraduate, graduate, and Ph.D students in collaboration with faculty members to promote and foster interest and skills in trusted and assured microelectronics through:
  - Internships
  - Co-Ops
  - Employment
  - Faculty Research
  - Student mentorship/collaboration
  - Onsite visibility
- Develop long term partnerships with universities to create self-sustaining pipeline
- Topics developed include microelectronic design, fabrication, logistics, testing, and analysis.



Author's Own

Military Academies and Institutions

- Increase Military members with Degrees
  - Improve AFIT/NPS research quality
  - Improve pipelines for military students to civilian schools
- Targeted Short Courses
  - Knowledge and skill development for the DoD workforce involved in design, fab, logistics, testing, analysis, and assurance techniques.
- Proposed Trust in Microelectronics Ph.D. program
  - For the students to understand the synergistic nature of the many aspects of microelectronics trust and to be able to develop solutions to both current and future challenges to the security of the microelectronics environment.
  - Key areas of knowledge include:
    - Electronics architecture and manufacturing
    - Test and Evaluation of microelectronics
    - Supply Chain management
    - Systems Engineering management
    - Complex Systems analysis
  - Two students at Air Force Institute of Technology (AFIT)
  - Two students at Navy Postgraduate School (NPS)

Thank You

Questions?

Education & Workforce Development Panel: SCALE (Scalable Asymmetric Lifecycle Engagement)

Peter BERMEL

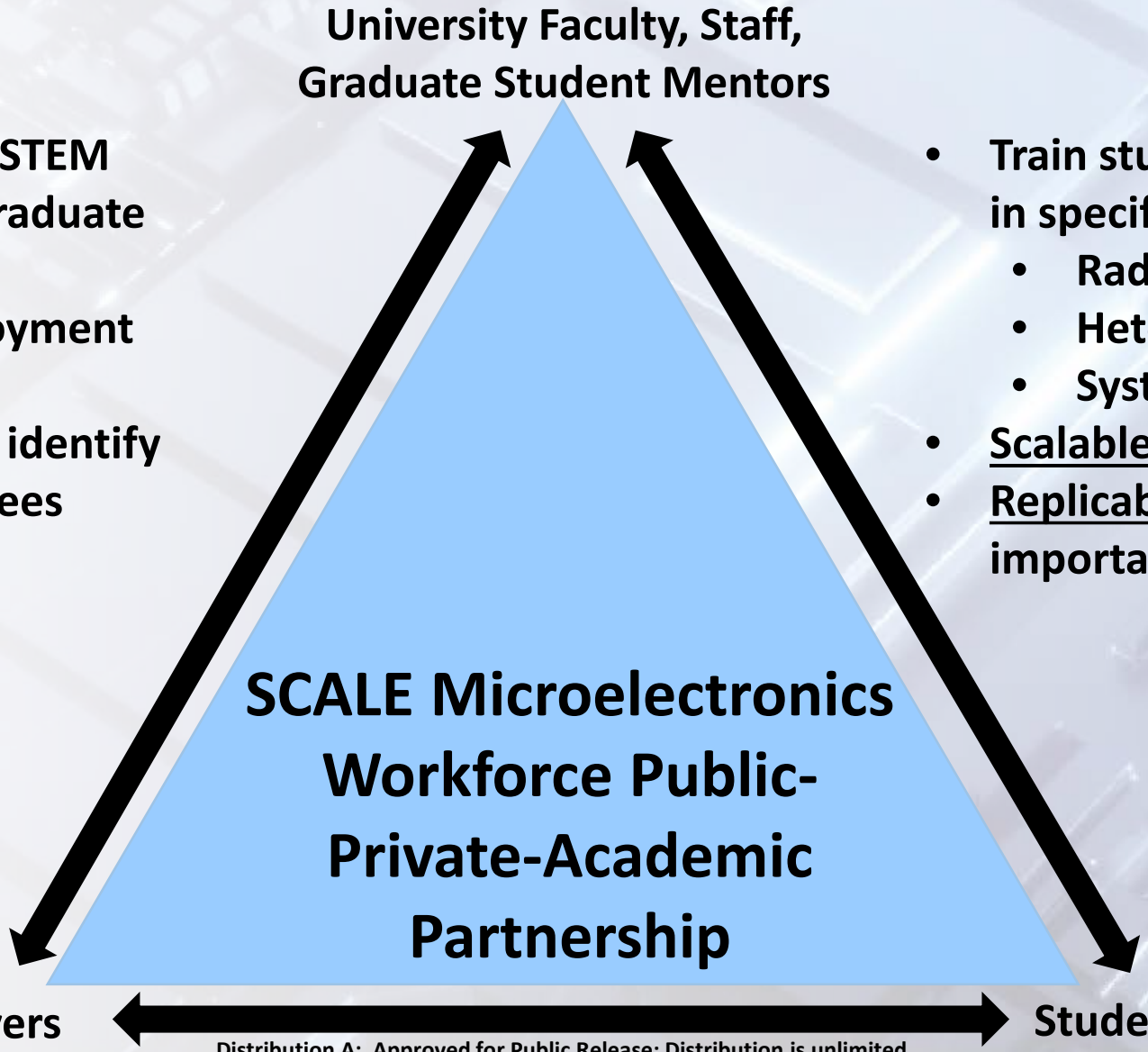
SCALE PRINCIPAL INVESTIGATOR

ASSOCIATE PROFESSOR OF ELECTRICAL & COMPUTER ENGINEERING

PURDUE UNIVERSITY

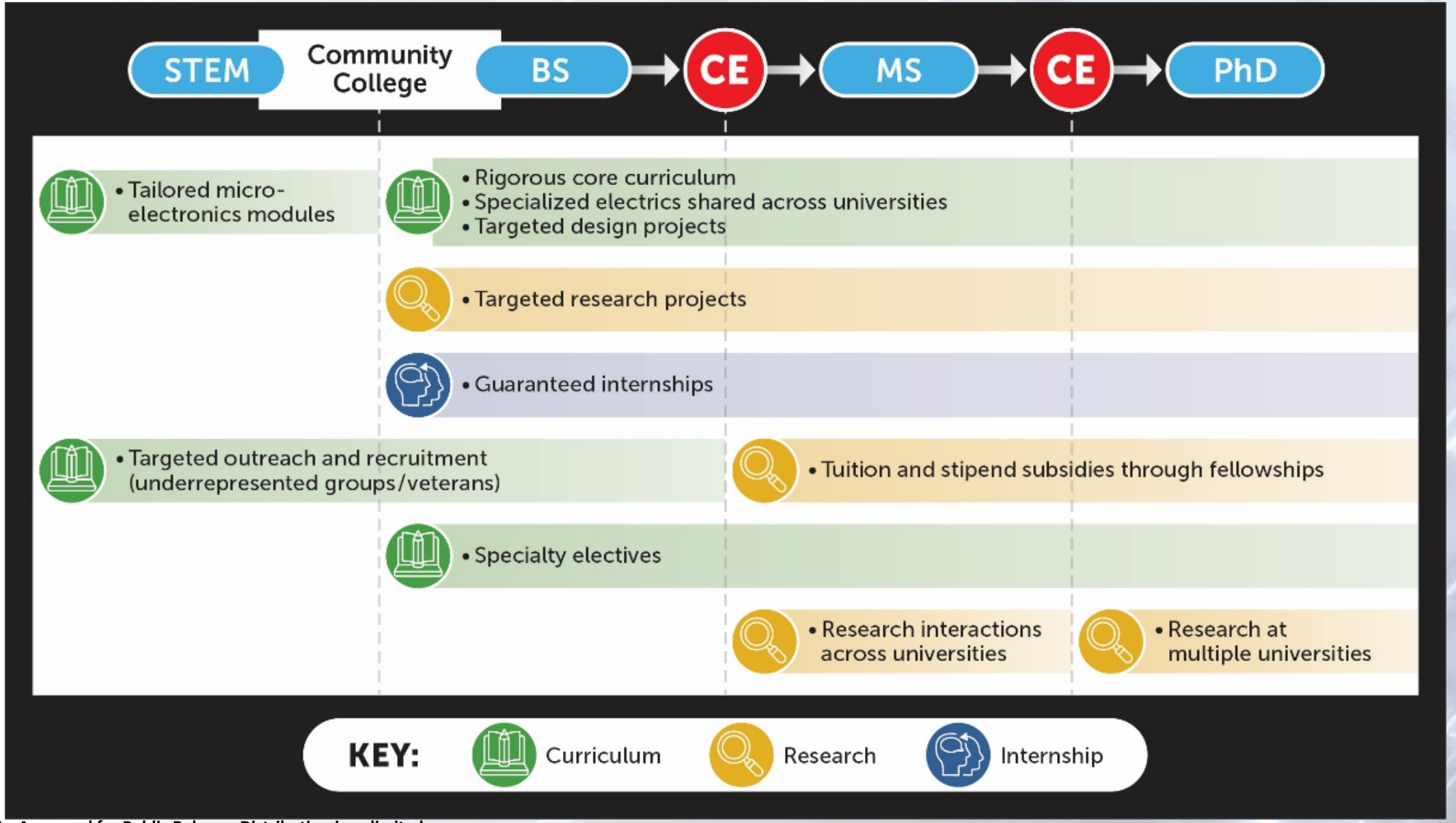
SCALE provides the US with an asymmetric workforce advantage in microelectronics

- To motivate talented STEM undergraduate and graduate students to choose DOD/GOV/DIB employment
- For DOD/GOV/DIB to identify and hire new employees

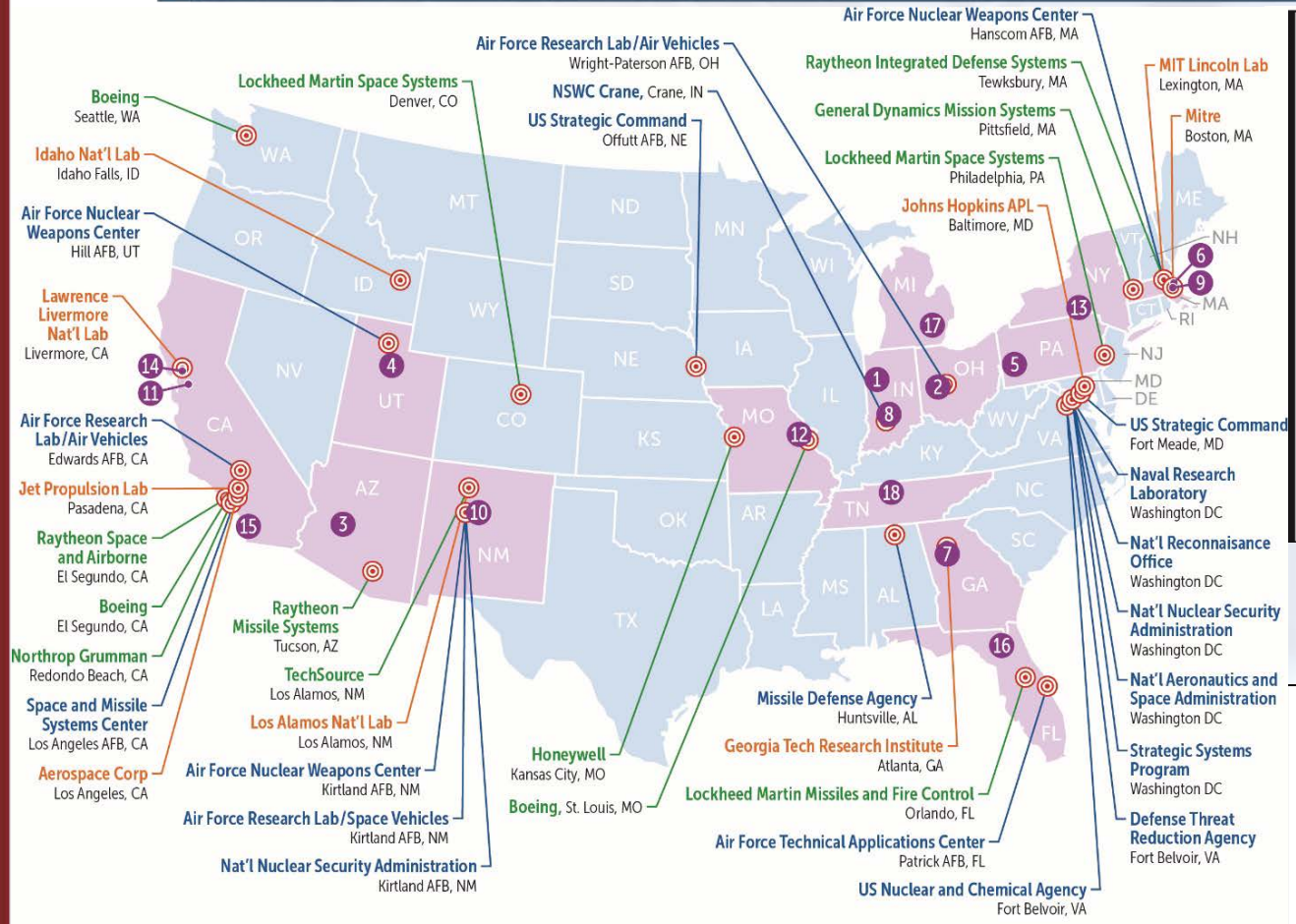


- Train students and support faculty in specific technical areas:
  - Radiation-hardening
  - Heterogeneous integration
  - System-on-Chip
- Scalable to multiple universities
- Replicable to additional topics important to the DOD/GOV/DIB

SCALE rigorously develops key KSAs through courses, projects, research, and internships



SCALE is a nationally coordinated network of partners, regionally executed



Target Institutions

Government | Federally Funded Research and Development Centers | Industry

Partners (Institution Topic Areas*)

1. Purdue University, West Lafayette, IN (RH, HIAP, SC, ESS, SC)
2. Air Force Institute of Technology, Wright-Patterson Air Force Base, OH (RH)
3. Arizona State University, Tempe, AZ (RH, HIAP, SC)
4. Brigham Young University, Provo, UT (RH)
5. Carnegie Mellon University, Pittsburgh, PA (ESS, SoC)
6. Draper Laboratory, Campridge, MA (RH)
7. Georgia Institute of Technology, Atlanta, GA (RH, HIAP, SC, ESS, SoC)
8. Indiana University, Bloomington, IN (ESS, SoC)
9. Massachusetts Institute of Technology, Boston, MA (ESS, SoC)
10. Sandia National Laboratory, Albuquerque, NM (RH)
11. Sandia National Laboratory, Livermore, CA (RH)
12. St. Louis University (RH)
13. State University of New York at Binghamton, NY (HIAP)
14. University of California, Berkeley, CA (ESS, SoC)
15. University of California, San Diego, CA (ESS)
16. University of Florida, Gainesville, FL (SC)
17. University of Michigan, Ann Arbor, MI (RH)
18. Vanderbilt University, Nashville, TN (RH)

*RH = Radiation Hardened, HIAP = Heterogeneous Integration/Advanced Packaging, SC = Supply Chain, ESS = Embedded Systems Security, SoC = System on Chip)

SCALE PPAP National Network

Technical Verticals

Radiation-hardened technology:

1. Vanderbilt
2. Air Force Institute of Technology
3. St. Louis University
4. Brigham Young University
5. Arizona State University
6. Georgia Tech
7. Purdue University

Heterogeneous integration and advanced packaging:

1. Purdue University
2. Georgia Tech
3. SUNY-Binghamton
4. Arizona State University

System on Chip:

1. Ohio State University
2. Georgia Tech
3. Purdue University
4. UC-Berkeley

Best Practices in Talent Management

Carolyn GOERNER

CLINICAL PROFESSOR OF MANAGEMENT

KELLEY SCHOOL OF BUSINESS,
INDIANA UNIVERSITY-BLOOMINGTON

Best Practices in Talent Management

- **Recruiting/Selection**
  - Realistic Job Previews (RJPs)
  - Long-term relationships
  - “Success Profiles”

- **Performance Management**
  - Regular feedback cycles (vs. annual reviews)
  - Customized, goal-driven assessments
  - Coaching

Best Practices in Talent Management

- Emphasize company culture
- Rapid Talent Allocation
- Psychologically safe work environment

Thank You

Questions and Open Panel Discussion

T&AM: Create a Robust and Resilient Microelectronics Pipeline Panel

AFTERNOON BREAK
1600 - 1615

T&AM: Create a Robust and Resilient Microelectronics Pipeline Panel Agenda

- 1415 - 1435 Introduction
  - Dr. Matthew Casto, T&AM Program Director
- 1425 – 1600 Education and Workforce Development Consortium Panel
  - Allison Smith, Naval Surface Weapons Center – Crane, T&AM Technical Execution Lead
  - Panel Members NSS IECRC, Universities Cincinnati, Purdue, Florida and Ohio
- 1600 - 1615 AFTERNOON BREAK

- 1615 - 1645 OSD and AF Microelectronics Design and Prototype Challenge
  - Vipul J. Patel, AFRL, Sr. Electronics Engineer
- 1645 – 1715 Technology Development
  - Peter O'Donnell, Army Combat Capabilities Combat Command, T&AM Technical Execution Area
- 1715 – 1745 Supply Chain Awareness and Security
  - Adam Hauch, Naval Surface Weapons Center – Crane, Technical Execution Area Lead
- 1745 – 1845 Virtual Demo & Poster Session

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SLIDES ONLY

NO SCRIPT PROVIDED

Trusted and Assured Microelectronics (T&AM) Technology Development Technical Execution Area (TEA)

Peter O'Donnell

Army Combat Capabilities Development Command Aviation & Missile Center (CCDC AvMC)

DARPA Electronics Resurgence Initiative (ERI)

August 19, 2020

Technology Development TEA Overview

Develop a pipeline of robust and resilient microelectronics technologies that are vital to U.S. battlefield advantage and critical to U.S. infrastructure

- ***Leverages*** State-Of-The-Art (SOTA) commercial technology to co-develop assured solutions
- ***Adapts*** SOTA commercial technology to enable Department of Defense (DoD) unique solutions
- ***Accelerates*** development of SOTA technology enabling earlier adoption into DoD Programs with lower risk
- Sub-Areas:
  - Compute Platforms
  - Domain Specific Technologies
  - Programmable Logic
  - Supply Chain Solutions

- Enables rapid acquisition and deployment of SOTA commercial microelectronics
- Early access to technology enables modernized warfighting capability
- SOTA Requirements and Market Pull enabling Assurance & Security Tech Insertion

Technology Development TEA Overview

Inputs

- DoD Programs & Program Executive Offices (PEOs)
- T&AM Broad Agency Announcement
- T&AM Technical Execution Areas (TEAs)
- Industry Engagement
- Disruptive Technology
- Threat Information
- DARPA ERI

Technology Development

Industry

Government

Size, Weight, and Power (SWaP) / Performance	Compute Platforms	• High Performance • Artificial Intelligence • Board Consortium
	Programmable Logic	• Field Programmable Gate Array (FPGA) • Embedded FPGA (eFPGA)
Access / Availability Obsolescence	Design & Integration	• Commercial Off the Shelf (COTS) Co-Development
	Supply Chain Solutions	• Traceability
Security	Assurance / Protection	
DoD Unique Specialization	Domain Specific Technologies	• 5G / Communications • Positioning, Navigation, and Timing (PNT) • Autonomy

Results

- Tech early access
- Risk buy down / Tech Maturation
- Transition & Partnerships
- Economic Competitiveness
- Ecosystem of DoD Solutions

Technology Development TEA Overview

Develop a pipeline of robust and resilient microelectronics technologies that are vital to U.S. battlefield advantage and critical to U.S. infrastructure

Workshop Panelist:

1. Peter O'Donnell – T&AM Technical Execution Lead, Army CCDC, Protective Technologies Division Chief
2. Thomas Dalrymple – Technical Advisor, Sensor Subsystems, AFRL Sensors Directorate
3. Sam Wanis, PhD – Research Program Manager, Advanced Electronics, Northrop Grumman Corporation
4. Scott Suko – Tech Subject Matter Expert, Northrop Grumman Corporation
5. Ryan Close, PhD (ST) – Chief Scientist, Signal and Image Processing, C5ISR Center, Night Vision and Electronic Sensors Directorate (NVESD), U.S. Army Combat Capabilities Development Command (DEVCOM)

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Automated Microelectronics Analysis and Reports Optimization Tool

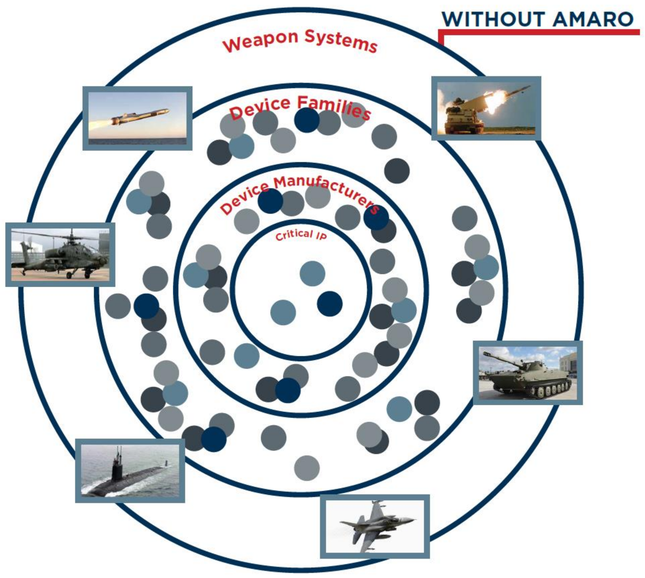
NSWC Crane, KSM Consulting

AMARO

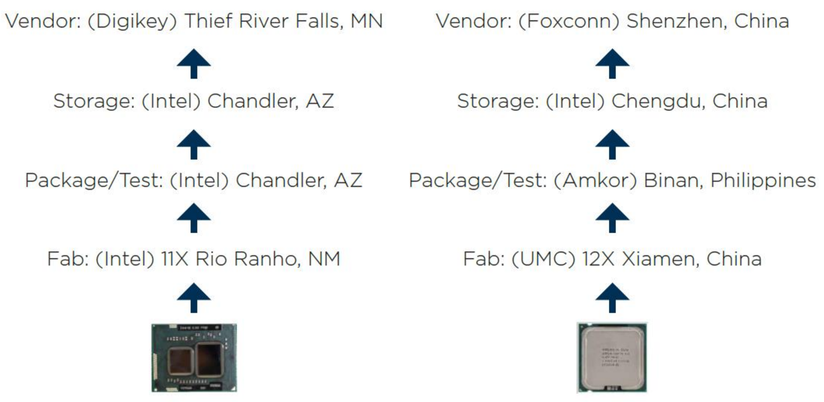
T&AM Program/Supply Chain Awareness and Security

The Challenge Today

Supply chain tools on the market today only look at the risk of the overall manufacturer; which is insufficient for the needs of the Department of Defense



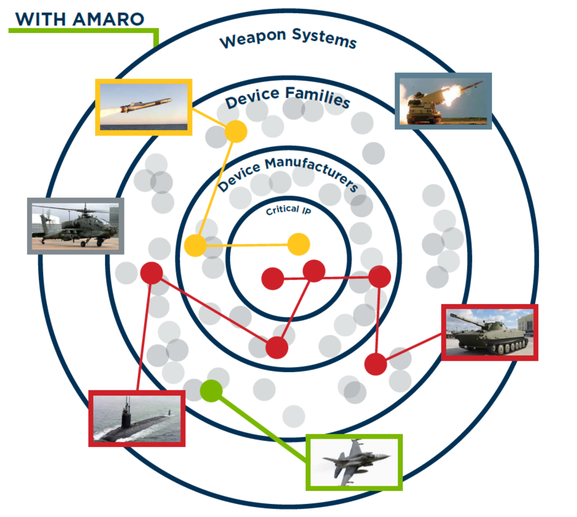
Same company; different risk profiles for individual parts



Strategic analysis of microelectronics issues is a manual, time intensive process. The Department of Defense requires the capability to assess the fragility of the various semiconductor segments, and the ability to forecast the impacts of events like COVID-19, earthquakes, foundry closures, and acquisitions

Solution

AMARO automates and enhances the proactive identification of supply chain risk by digesting thousands of structured and unstructured government and non-government datasets, applying advanced analytics, and formulating easy-to-digest displays

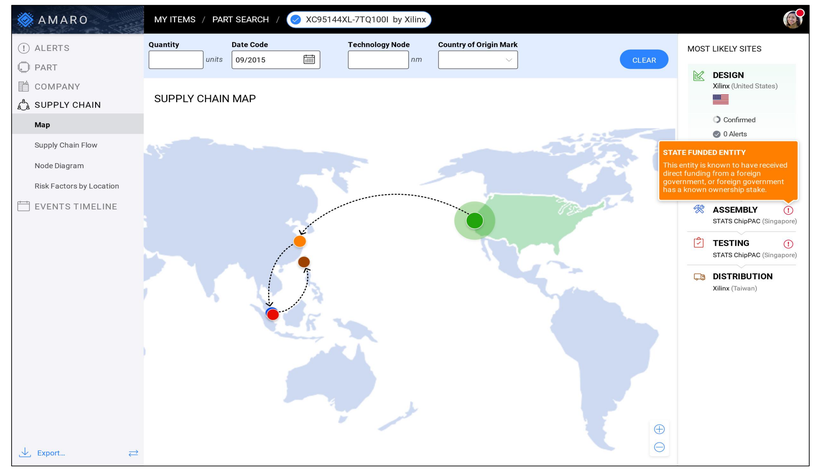


Strategic Analysis Capabilities

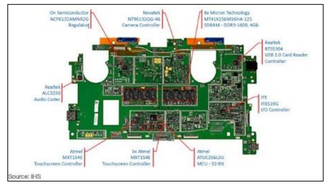
- What parts are potentially impacted if the operations of specific sites are interrupted due to global events, such as the Coronavirus outbreak?
- Can we look across thousands of BOMs to identify an overreliance on specific suppliers or sites/locations?
- Are there suppliers or supply chain sites that are owned or funded by a foreign government?
- How can I track a threat or vulnerability through the supply chain to determine the impacted weapon systems?
- What all parts in the DoD supply chain could be impacted if a trade war escalates with a foreign country?

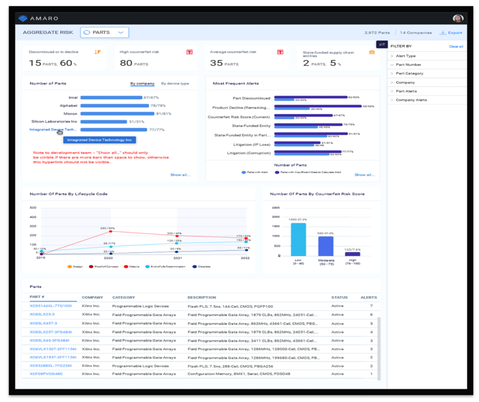
AMARO Capabilities

Part-Centric Supply Chain Analysis

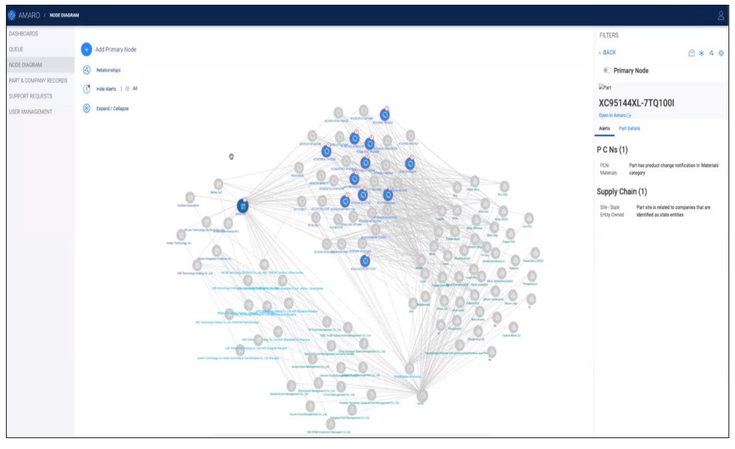


Bill of Materials / Aggregate Risk Analysis





Proactive Strategic Analysis Features



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