Trusted and Assured Microelectronics Program

Create a Robust and Resilient Pipeline

Matthew Casto, Ph.D.
Program Director, Trusted and Assured Microelectronics

DARPA ERI Summit
August 2020

https://www.CTO.mil
@DoDCTO

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Distribution Statement A: Approved for public release; DOPSR Case # 20-S-1903 applies. Distribution is unlimited.
Drive reformation and Form Alliances to Enhance Lethality
Promote, Protect, Partner
Modernization priorities to rapidly create advantage

Microelectronics is DoD’s Top Modernization Priority!
T&AM/MINSEC Program is developing the secure ecosystem to assure SOTA performance for Modernization
Microelectronics Landscape

Specialization of Electronics – Risk in Global Supply – Changing the Lifecycle Speed & Cost Efficiency

Joint Strike Fighter uses 100+ different process IP

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## Trusted and Assured Microelectronics

### Strategic Approach

**Data Driven**

- Quantifiable Assurance

**Secure full lifecycle confidentiality, integrity, verification & validation, and supply chain for assured warfighters electronics**

**Address DoD Unique Needs**

- Increased sources for national strategic defense

**Create a Resilient and Robust Pipeline**

- Domestic and Allied Ecosystem to rapidly and securely mature emerging advanced technology

### Gaps:

<table>
<thead>
<tr>
<th>Access to State of the Art Commercial Technology</th>
<th>Data Driven Quantifiable Assurance</th>
<th>Address DoD Unique Needs</th>
<th>Create a Resilient and Robust Pipeline</th>
</tr>
</thead>
<tbody>
<tr>
<td>DoD lags commercial CMOS ecosystem/ infrastructure</td>
<td>Threats to design and manufacturing in global supply chain</td>
<td>Increased sources for national strategic defense</td>
<td>Domestic and Allied Ecosystem to rapidly and securely mature emerging advanced technology</td>
</tr>
</tbody>
</table>

### Approach:

| Establish best practices for secure design, assembly, packaging, and test capabilities to support DIB and co-development of dual use electronics | Secure full lifecycle confidentiality, Integrity, verification & validation, and supply chain for assured warfighters electronics | Develop sustainable sources of mission essential niche rad-hard electronics capabilities, and specialized radio frequency and electro-optic components | Invigorate secure pipeline for disruptive R&D transition, supply chain aware technology development, education and workforce. |

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**Microelectronics - DoD’s Top Modernization Priority**

*We cannot expect success fighting tomorrow’s conflicts with yesterday’s weapons or equipment.*

-National Defense Strategy

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**Access to State of the Art Commercial Technology**

- DoD lags commercial CMOS ecosystem/ infrastructure

**Data Driven Quantifiable Assurance**

- Threats to design and manufacturing in global supply chain

**Address DoD Unique Needs**

- Increased sources for national strategic defense

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Current T&AM Challenges

• Lower barriers to specialization and innovation in advanced IC technologies; Tools, Intellectual Property, Fabrication
• Attract, recruit and retain talented STEM workforce with knowledge of DoD-specific challenges
• Identify & mitigate supply chain threats to improve assurance & resilience of microelectronics
• Rapidly mature, co-develop, and transition new and emerging technologies with assurance and security for program adoption
Create a Resilient and Robust Pipeline

Invigorate secure pipeline for disruptive R&D transition, supply chain aware technology development, education and workforce.

**Innovation Accelerators**
- Engage with non-traditional technology sources to cultivate a SOTA microelectronics ecosystem, built on a foundation of assurance
- Technology for DoD Asymmetric Advantage
- DoD Asymmetric Advantage; Sustainable US company

**Education and Workforce Development**
- Outreach to universities to develop US-based semiconductor-focused education pipelines; Semiconductor Fab, Security/Assurance, Design, Package, and Test
- Education and Training for DoD and DIB

**Supply Chain Awareness and Security**
- Addressing security to risk supply chain through tech development, V&V, and CI awareness; Briefings to DIB partners and industry
- Improve Supply Chain Awareness
- Intelligence prep of the Battlespace
- Counterintelligence Execution

**Technology Development**
- Leverage SOTA commercial technology to co-develop assured solutions
- Adapt SOTA technology to enable DoD Unique solutions
- Accelerate on-shore availability and development for adoption in DoD PoR
- Compute Platforms, Domain Specific Tech, Supply Chain Solutions, Programmable Logic

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T&AM: Create a Robust and Resilient Microelectronics Pipeline Panel Agenda

- **1415 - 1435 Introduction**
  - Dr. Matthew Casto, T&AM Program Director

- **1425 – 1600 Education and Workforce Development Consortium Panel**
  - Allison Smith, Naval Surface Weapons Center – Crane, T&AM Technical Execution Lead
  - Panel Members NSS IECRC, Universities Cincinnati, Purdue, Florida and Ohio

- **1600 - 1615 AFTERNOON BREAK**

- **1615 - 1645 OSD and AF Microelectronics Design and Prototype Challenge**
  - Vipul J. Patel, AFRL, Sr. Electronics Engineer

- **1645 – 1715 Technology Development**
  - Peter O’Donnell, Army Combat Capabilities Combat Command, T&AM Technical Execution Area

- **1715 – 1745 Supply Chain Awareness and Security**
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- **1745 – 1845 Virtual Demo & Poster Session**
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Education & Workforce Development Panel

Session: Trusted and Assured Microelectronics (T&AM): Create a Resilient and Robust Microelectronics Pipeline
Panel Discussions - Housekeeping

- If you have non-technical issues, please contact the **CO-HOSTS** identified as **FACILITATORS**

- All conversations must remain at Distribution A level (no classified, FOUO, CUI, etc.)

- Microphones will be muted and videos disabled for attendees.

- For questions or comments to the panel members, please use the Q&A Feature

  - If you have a question for the speaker or would like to share insights, please use the “Q&A Feature”.
    - The presenter will answer your question or comment on your insights.
    - You will have 60 seconds to ask your question or share your insights.

  - If you dial-in separately using your phone, please link the phone connection with your assigned participant ID
    - The participant ID is the 6 numbers seen by clicking on the in the upper left of the Zoom screen
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      - Wireless Connection Issues: https://support.zoom.us/hc/en-us/articles/201362463-Wireless-WiFi-Connection-Issues
    - Connect with the ERI Team desk via the 6Connex platform
Dr. Alison Smith
NAVAL SURFACE WARFARE CENTER, CRANE DIVISION (NSWC CRANE)

Mr. Len Orlando
AIR FORCE RESEARCH LABORATORY (AFRL)

T&AM EDUCATION & WORKFORCE DEVELOPMENT EXECUTION CO-LEADS
“As much as emerging technologies will define future conflict, the war for talent will likely play the central role in the outcome of long-term technological competition.

The National Security Innovation Base (NSIB) struggles to attract, recruit, and retain a workforce willing and able to tackle tough challenges and find innovative solutions. Universities are confronting a dearth in American talent generation and retention.”

T&AM Has Unique Interdisciplinary Needs Within A Competitive STEM Market

Source: Engineering Talent Shortage Now Top Risk Factor, Semiconductor Engineering, Deloitte Survey, Feb. 25, 2019
T&AM Education & Workforce Development

Subject Matter Experts (SME’s)

DoD Industrial Complex

WAR College
NPS
AFIT
Academy
DAU

DoD Relevant Problems
Unique Facilities
On-site Presence
Clearances
Centers of Excellence
Federal and State Matching

SCALE
AFOSR CYAN and MEST
NSF CHEST

Leaders

Public Academic Ecosystem

DoD Academic Ecosystem

Inform, Integrate, and Acquire

Strategy
Professional
Business
Legal

Highlights

COMMERCIAL TRAINING

(1) 56 Interns and 30 Co-ops slots available Su’20
(2) U of F T-Paine Su’20 with 20 Applicants
(3) Congressional AD STAFFRE completed with 9 Prof. and
15 Students – FY20 Completion
(4) 4 DAGSI Students
(5) SME’s attend >5 conferences/yr and participate on Technical Steering Committees
(6) Site Visits >15 Universities
(7) Serve on 3 University Advisor Boards
(8) Participates in STEM Eval, Hackathon, summer bootcamp, etc.

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Education & Workforce Development Panel

- **Prof. Marty Emmert**, NSF IUCRC CHEST (Center for Hardware and Embedded System Security and Trust)
- **Prof. Mark Tehranipoor and Prof. Waleed Khalil**, AFOSR MEST/CYAN (The National Microelectronics Security Training Center and the Center for Enabling Cyber Defense in Analog and Mixed Signal Domain)
- **Dr. Praveen Chawla**, Edaptive Computing Inc.
- **Ms. Cheyanne Harshman**, Centauri Corp.
- **Prof. Peter Bermel**, SCALE (Scalable Asymmetric Lifecycle Engagement)
- **Prof. Carolyn Goerner**, Best Practices in Talent Management
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NSF Center for Hardware and Embedded Systems Security and Trust (CHEST) IUCRC
John (Marty) EMMERT

PROFESSOR, UNIVERSITY OF CINCINNATI
DIRECTOR, CHEST IUCRC
Funding Overview & Key Partnerships

POC: Dr. J. M. Emmert (Marty), University of Cincinnati  
email: John.Emmert@uc.edu  
Mr. Luis Concha, University of Cincinnati  
Email: Luis.Concha@uc.edu

<table>
<thead>
<tr>
<th>Year</th>
<th>Fee</th>
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<tbody>
<tr>
<td>2020</td>
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<tr>
<td>2021</td>
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<td>2023</td>
<td>$50k</td>
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<tr>
<td>2024</td>
<td>$50k</td>
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Requirements: Membership Support, IAB Oversight, Data
IAB Leads: Len Orlando and Brian Dupax, AFRL
CHEST Team: Marty Emmert, Director (UC), Houman Homayoun (UC Davis), Yunsi Fei (NU), John Chandy (UCONN), Yiorgos Makris (UTD), James Lambert (UVa)

Approach

• Technical: The NSF CHEST Center addresses security, assurance, and trust across several levels: Large-scale systems, embedded systems, design and operations, requirements, standards, manufacturing, supply chains, and integrated circuits and boards.
• Contract: Vehicle: MIPR (DoD) or Check (Industry)  
  https://www.nsf.gov/eng/iip/iucrc/government.jsp  
  https://www.nsf.gov/eng/iip/iucrc/iaainstructions.jsp
• Monthly / Quarterly / Annual Reports and Updates
• Royalty free access to IP: Standard NSF IUCRC MOU
• HW / SW / Testbed Demonstrations
• WF Development: Next generation of SMEs in the area of Security, Assurance and Trust for Electronic HW and Embedded Systems

Description of Project and link to T&AM Mission

• Coordinates university-based research with needs of industry and government partners to advance knowledge of microelectronic security, assurance, and trust (SAT)
• Identification, detection, monitoring, mitigation, and elimination of vulnerabilities that affect electronic hardware and embedded systems

How is this better than current SOTA

• With industry oversite, the CHEST Center addresses a range of attack vectors across design, operation, manufacturing, supply chains, and integration of the HW, SW, and firmware
• Limited 10% overhead: 90% of all funds go directly to research
• Minimal time required to get projects “on contract”
• Educating the next generation of experts
• Collaborative environment: DoD / Industry / NSF / Academia

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What types of problems does CHEST address?

- Any basic or applied research related to SAT
- SCA: detection, prevention, mitigation
- Trojan: detection, prevention, mitigation (eg. =>)
- Reverse engineering: ASIC (physical -destructive/nondestructive) and FPGA bitstreams
- Integrated circuit and silicon authentication
- Anti Tamper: detection, prevention, mitigation
- Countermeasure design / methodologies
- PUFs (physical unclonable functions)
- Intellectual Property: protection, anti-cloning, anti-counterfeiting, over-manufacturing, piracy etc.
- Assessment: metrics for levels of TRUST
- Embedded algorithm protection
- Legacy systems
- Etc.
Waleed KHALIL

PROFESSOR – OHIO STATE UNIVERSITY
CO-DIRECTOR OF CYAN AND MEST CENTERS OF EXCELLENCE
Center of Excellence for Cyber Defense in the Analog and Mixed Signal (AMS) Domain (CYAN)

Research Program & Team

- Strong & diverse expertise in hardware security, AMS design, fabrication, test, electromagnetics, applied cryptography, machine learning and data analytics
- Holistic research approach in securing the design, fabrication, and operation of AMS technologies and analog emissions

Education & Capacity Building

- New generation of workforce exposed to multidisciplinary environment of modern-day scientific research
- Target 20 PhD/MS students + 20 undergraduates (50% US)
- 18 PhD/MS students currently affiliated with the center: 11 receive direct CYAN funding and 7 from external sources (10 US students in total)

Government & Industry Partnership

- Consortium-led cooperation with national labs, commercial and defense industry
- Grow research funding to sustain CYAN beyond 5 years
- Leverage add’l funding to amplify the research: 1 funded project/ 5 pending

CYAN Thrust 1: Securing AMS Devices & Systems

- AMS Security Primitives
- AMS Obfuscation
- AMS Counterfeit & Trojan Detection/Prevention
- Analog Enabled Cryptography
- Securing Power Supplies

CYAN Thrust 2: Exploiting Analog Emanations for Cyber Defense

- RF and Process Authentication
- Electromagnetic Signatures from AMS Devices
- Program Analysis via Side-channel Signals
- Side Channel Assessment
Mark TEHRANIANPOOR

INTEL CHARLES E. YOUNG ENDOWED CHAIR PROFESSOR – UNIVERSITY OF FLORIDA

DIRECTOR FOR FICS RESEARCH, CO-DIRECTOR FOR CYAN AND MEST CENTERS OF EXCELLENCE
MEST: National MicroElectronics Security Training Center

Research Program & Team

- Increasing demand for well-trained cybersecurity workforce in all government agencies, national labs, and industry sectors!
- MEST offers a comprehensive training effort in microelectronics security is a critical need
- Outstanding team of faculty and industry practitioners offering webinars, long, and short courses

Education & Capacity Building

- New generation of workforce exposed to multidisciplinary environment of modern-day scientific research
- Total attendees (Webinar + Certificate Trainings): 2000+
- 16 webinars, 8 trainings, and 5 online courses developed so far

Government & Industry Partnership

- Develop and provide free training programs on microelectronics design and security to the Government and Defense Industrial Base
- We plan to establish a consortium of companies sponsoring MEST in the future

System
(iots, Embedded, CPS, Networked Systems)

Hardware
(Circuit/Architecture)

Device
(CMOS & Beyond)

- Cybersecurity Case Studies
- Secure Architecture Design
- Automotive Security
- Cross Layered Systems Security
- Introduction to IoT Security
- Asynchronous Design Practices for Secure Hardware
- Introduction to Hardware Security and Trust
- Secure Architecture Design
- Physical Inspection
- Hardware Security Lab
- Advanced Topics in Hardware Security and Trust
- Physical Inspection
- Introduction to AMS Security
Workforce Development
Application Engineer Training & Technical Transition
Praveen CHAWLA
PRESIDENT/CTO
EDAPTIVE COMPUTING, INC.
• Workforce Development Goals:
  • Transition students and industry professionals into the hardware security workforce for government agencies, national laboratories and industry sectors
  • Apply automation tools to ease transition and increase efficiency of workforce entry into verification engineering for assuring and securing microelectronics

• Workforce Development Architecture:
  • Holistic and integrated approach to both train the next generation of hardware security engineers and develop comprehensive, enterprise tools and solutions for assured and secure microelectronics

Application Engineer Training:

Verification Methodology
- Security Verification & Validation
- Formal Methods & Model Checking
- Directed Testing/Emulation

Verification Tools
- Tortuga Logic Radix-S
- OneSpin Tool Suite
- SoC Verify
- Synopsys/ZeBu

Assured & Secure Microelectronics

Technical Transition:

<table>
<thead>
<tr>
<th>University of Florida:</th>
<th>University of Cincinnati:</th>
<th>Edaptive Computing:</th>
<th>DARPA IDEA/POSH:</th>
</tr>
</thead>
<tbody>
<tr>
<td>• FICS SoC Trust &amp; Validation (STV)</td>
<td>• Memometer – Generation and interrogation of a digital signature of an FPGA/ASIC/PLD</td>
<td>• SoC Verify – Enterprise Verification Management</td>
<td>• Support ZS3 Emulation</td>
</tr>
<tr>
<td>• FICS AutoBOM – Automatic Bill of Materials for PCB</td>
<td>• FACETS – Formal Assertions and Security Monitoring for Trusted SoCs</td>
<td>• Synopsys Emulation accessible and enabled through cloud</td>
<td>• University of Michigan</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Princeton University</td>
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<td>• Washington University</td>
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Distribution A: Approved for Public Release; Distribution is unlimited.
Active Accounts on TSS:  
OneSpin Trainees:  
Radix-S Trainees:  
Synopsys Tools Trainees:  

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<tr>
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<th>Radix-S Trainees</th>
<th>Synopsys Tools Trainees</th>
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<tr>
<td>108</td>
<td>96</td>
<td>24</td>
<td>17</td>
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Current Workforce Training Numbers:

Current 2020 OneSpin Training Schedule:

<table>
<thead>
<tr>
<th>Class:</th>
<th>Date:</th>
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</thead>
<tbody>
<tr>
<td>Online OneSpin EC Course</td>
<td>August 5th</td>
</tr>
<tr>
<td>Online OneSpin FIA/FPA Course</td>
<td>August 19th</td>
</tr>
<tr>
<td>Online OneSpin 360 DV Apps Course</td>
<td>September 9th</td>
</tr>
<tr>
<td>Online OneSpin ABV &amp; MDV Course</td>
<td>October 7th</td>
</tr>
<tr>
<td>Online OneSpin EC Course</td>
<td>October 28th</td>
</tr>
<tr>
<td>Online OneSpin 360 DV Apps Course</td>
<td>November 4th</td>
</tr>
<tr>
<td>Online OneSpin FIA/FPA Course</td>
<td>November 18th</td>
</tr>
<tr>
<td>OneSpin 3-Day Intro Course (ECI)</td>
<td>December 15th-17th</td>
</tr>
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</table>

Success Checks:

- Training Program Certification
- Track Student Training Attendance
- Tool Usage in Cloud Environment
- Technical Support Services

- Online Tortuga Logic Radix-S Training Class:
  - 1st Class: July 2020
  - Additional Classes: September-October 2020

- OneSpin/ECI Formal Verification Certification Intro Training Class
  - September 2020

- Synopsys Verdi and ZS Platform Training
  - Fall 2020
For Education & Workforce Development Panel: Centauri Educational Outreach and Partnerships
University Engagement

• Centauri is focused on creating a national approach to interacting with universities and additional academic institutions to engage undergraduate, graduate, and Ph.D students in collaboration with faculty members to promote and foster interest and skills in trusted and assured microelectronics through:
  • Internships
  • Co-Ops
  • Employment
  • Faculty Research
  • Student mentorship/collaboration
  • Onsite visibility
• Develop long term partnerships with universities to create self-sustaining pipeline
• Topics developed include microelectronic design, fabrication, logistics, testing, and analysis.
Military Academies and Institutions

• Increase Military members with Degrees
  • Improve AFIT/NPS research quality
  • Improve pipelines for military students to civilian schools

• Targeted Short Courses
  • Knowledge and skill development for the DoD workforce involved in design, fab, logistics, testing, analysis, and assurance techniques.

• Proposed Trust in Microelectronics Ph.D. program
  • For the students to understand the synergistic nature of the many aspects of microelectronics trust and to be able to develop solutions to both current and future challenges to the security of the microelectronics environment.
  • Key areas of knowledge include:
    • Electronics architecture and manufacturing
    • Test and Evaluation of microelectronics
    • Supply Chain management
    • Systems Engineering management
    • Complex Systems analysis
  • Two students at Air Force Institute of Technology (AFIT)
  • Two students at Navy Postgraduate School (NPS)
Questions?
Education & Workforce Development Panel: SCALE (Scalable Asymmetric Lifecycle Engagement)
Peter BERMEL
SCALE PRINCIPAL INVESTIGATOR
ASSOCIATE PROFESSOR OF ELECTRICAL & COMPUTER ENGINEERING
PURDUE UNIVERSITY
SCALE provides the US with an asymmetric workforce advantage in microelectronics

University Faculty, Staff, Graduate Student Mentors

- To motivate talented STEM undergraduate and graduate students to choose DOD/GOV/DIB employment
- For DOD/GOV/DIB to identify and hire new employees

SCALE Microelectronics Workforce Public-Private-Academic Partnership

- Train students and support faculty in specific technical areas:
  - Radiation-hardening
  - Heterogeneous integration
  - System-on-Chip
- Scalable to multiple universities
- Replicable to additional topics important to the DOD/GOV/DIB

DOD/GOV/DIB Employers

Students

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SCALE rigorously develops key KSAs through courses, projects, research, and internships

**STEM**
- Tailored micro-electronics modules

**Community College**
- Rigorous core curriculum
- Specialized electrics shared across universities
- Targeted design projects
- Targeted research projects
- Guaranteed internships

**BS**
- **Curriculum**

**CE**
- **Research**
- Tuition and stipend subsidies through fellowships

**MS**
- **Research**
- Research interactions across universities

**CE**
- **Internship**
- Research at multiple universities

**PhD**

**KEY:**
- Curriculum
- Research
- Internship

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SCALE is a nationally coordinated network of partners, regionally executed.

Technical Verticals

Radiation-hardened technology:
1. Vanderbilt
2. Air Force Institute of Technology
3. St. Louis University
4. Brigham Young University
5. Arizona State University
6. Georgia Tech
7. Purdue University

Heterogeneous integration and advanced packaging:
1. Purdue University
2. Georgia Tech
3. SUNY-Binghamton
4. Arizona State University

System on Chip:
1. Ohio State University
2. Georgia Tech
3. Purdue University
4. UC-Berkeley

SCALE PPAP National Network

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Best Practices in Talent Management
Best Practices in Talent Management

• Recruiting/Selection
  • Realistic Job Previews (RJPs)
  • Long-term relationships
  • “Success Profiles”

• Performance Management
  • Regular feedback cycles (vs. annual reviews)
  • Customized, goal-driven assessments
  • Coaching
Best Practices in Talent Management

• Emphasize company culture

• Rapid Talent Allocation

• Psychologically safe work environment
Thank You

Questions and Open Panel Discussion
T&AM: Create a Robust and Resilient Microelectronics Pipeline Panel

AFTERNOON BREAK
1600 - 1615
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Trusted and Assured Microelectronics (T&AM) Technology Development Technical Execution Area (TEA)

Peter O’Donnell
Army Combat Capabilities Development Command Aviation & Missile Center (CCDC AvMC)
DARPA Electronics Resurgence Initiative (ERI)
August 19, 2020
Technology Development TEA Overview

Develop a pipeline of robust and resilient microelectronics technologies that are vital to U.S. battlefield advantage and critical to U.S. infrastructure

- **Leverages** State-Of-The-Art (SOTA) commercial technology to co-develop assured solutions
- **Adapts** SOTA commercial technology to enable Department of Defense (DoD) unique solutions
- **Accelerates** development of SOTA technology enabling earlier adoption into DoD Programs with lower risk

Sub-Areas:
- Compute Platforms
- Domain Specific Technologies
- Programmable Logic
- Supply Chain Solutions

- Enables rapid acquisition and deployment of SOTA commercial microelectronics
- Early access to technology enables modernized warfighting capability
- SOTA Requirements and Market Pull enabling Assurance & Security Tech Insertion
Technology Development TEA Overview

Technology Development

Inputs
- DoD Programs & Program Executive Offices (PEOs)
- DARPA ERI
- T&AM Technical Execution Areas (TEAs)
- Threat Information
- Industry Engagement
- T&AM Broad Agency Announcement

DoD Unique Specialization
- Domain Specific Technologies
  - 5G / Communications
  - Positioning, Navigation, and Timing (PNT)
  - Autonomy

Access / Availability Obsolescence
- Supply Chain Solutions
  - Traceability

Security
- Assurance / Protection

Size, Weight, and Power (SWaP) / Performance
- Programmable Logic
  - Field Programmable Gate Array (FPGA)
  - Embedded FPGA (eFPGA)

Compute Platforms
- High Performance
- Artificial Intelligence
- Board Consortium

Design & Integration
- Commercial Off the Shelf (COTS) Co-Development

Results
- Tech early access
- Risk buy down / Tech Maturation
- Transition & Partnerships
- Economic Competitiveness
- Ecosystem of DoD Solutions

Government

Industry
Technology Development TEA Overview

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*Develop a pipeline of robust and resilient microelectronics technologies that are vital to U.S. battlefield advantage and critical to U.S. infrastructure*

**Workshop Panelist:**

2. Thomas Dalrymple – Technical Advisor, Sensor Subsystems, AFRL Sensors Directorate
3. Sam Wanis, PhD – Research Program Manager, Advanced Electronics, Northrop Grumman Corporation
4. Scott Suko – Tech Subject Matter Expert, Northrop Grumman Corporation
5. Ryan Close, PhD (ST) – Chief Scientist, Signal and Image Processing, C5ISR Center, Night Vision and Electronic Sensors Directorate (NVESD), U.S. Army Combat Capabilities Development Command (DEVCOM)
T&AM: Create a Robust and Resilient Microelectronics Pipeline Panel Agenda

- **1415 - 1435 Introduction**
  - Dr. Matthew Casto, T&AM Program Director
- **1425 – 1600 Education and Workforce Development Consortium Panel**
  - Allison Smith, Naval Surface Weapons Center – Crane, T&AM Technical Execution Lead
  - Panel Members NSS IECRC, Universities Cincinnati, Purdue, Florida and Ohio
- **1600 - 1615 AFTERNOON BREAK**
- **1615 - 1645 OSD and AF Microelectronics Design and Prototype Challenge**
  - Vipul J. Patel, AFRL, Sr. Electronics Engineer
- **1645 – 1715 Technology Development**
  - Peter O’Donnell, Army Combat Capabilities Combat Command, T&AM Technical Execution Area
- **1715 – 1745 Supply Chain Awareness and Security**
  - Adam Hauch, Naval Surface Weapons Center – Crane, Technical Execution Area Lead
- **1745 – 1845 Virtual Demo & Poster Session**
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