ERI ELECTRONICS RESURGENCE INITIATIVE SUMMIT & MTO Symposium

WORKSHOP: ASIC Functional Verification

PROGRAM MANAGER: Serge Leef	
DATE: Tuesday, October 19, 2021	**TIME:** 3:15pm – 5:30pm
ROOM NAME: Julian Warchall	

DESCRIPTION

Brief presentations from industry and academia on the state-of-the-art and commercial needs in the ASIC functional verification space, followed by a panel discussion moderated by Program Manager Serge Leef that will encourage audience/panelist brainstorming on future functional verification challenges and solutions.

AGENDA

3:15pm-3:30pm	***Kickoff Presentation - ASIC Functional Verification*** Serge Leef, DARPA
3:30pm-3:45pm	***Industry Presentation - Verifying Accelerated Computing Platforms: Challenges and Opportunities*** Brucek Khailany, NVIDIA
3:45pm-4:00pm	***Industry Presentation - Questa ASIC Functional Verification Strategy*** Dennis Brophy, Siemens EDA
4:00pm-4:15pm	***Academic Presentation - Uniform Processor/Accelerator/Device Specification for Simulation-Based/Formal Verification*** Professor Sharad Malik, Princeton
Afternoon Break: 4:15pm-4:30pm	
4:30pm-4:45pm	***Academic Presentation - Rapid Design Verification with High-Level Synthesis*** Professor Jason Cong, UCLA
4:45pm-5:00pm	***Academic Presentation - Accelerating Simulation through Novel Hardware Architectures*** Professor Daniel Sanchez, MIT
5:00pm-5:30pm	***Panel Discussion - ASIC Functional Verification*** All presenters with audience participation
Workshops Conclude at 5:30pm	

QUESTIONS

Please contact Julian Warchall for more information following this workshop at julian.warchall.ctr@darpa.mil.