# ERI SUMMIT

ELECTRONICS RESURGENCE INITIATIVE

& MTO Symposium

MTO MICROSYSTEMS TECHNOLOGY OFFICE

DARPA

# SERGE LEEF

**PROGRAM MANAGER**
DARPA/MTO

ERI ELECTRONICS RESURGENCE INITIATIVE
SUMMIT
& MTO Symposium

# WORKSHOP INTRO: THE FUTURE OF OPEN-SOURCE CHIP DESIGN TOOLS

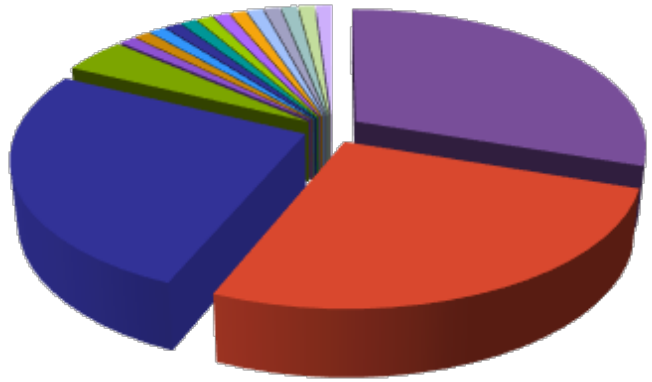
## ADVANCEMENTS IN OPEN-SOURCE ELECTRONIC DESIGN AUTOMATION

# Chip Design Challenge / Response

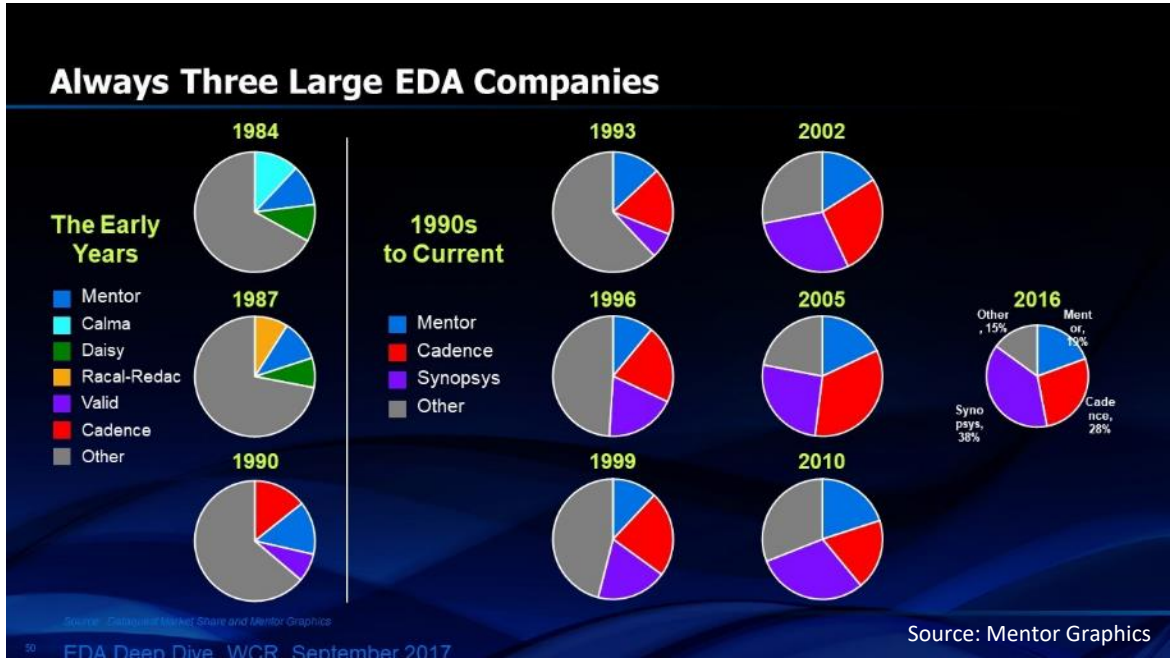

Source: https://vlkswgn.adsbit.site/volkswagen-manufacturing-country/

- **Challenge:** Product is half-sized every 1.5 years
- Need new factories for every new product
- Need new tooling to design each product
  - If cars followed the chip design rules, by 2013 the 1965 VW Beetle would be 1/1,000,000 inch long and travel 1/8 the speed of light

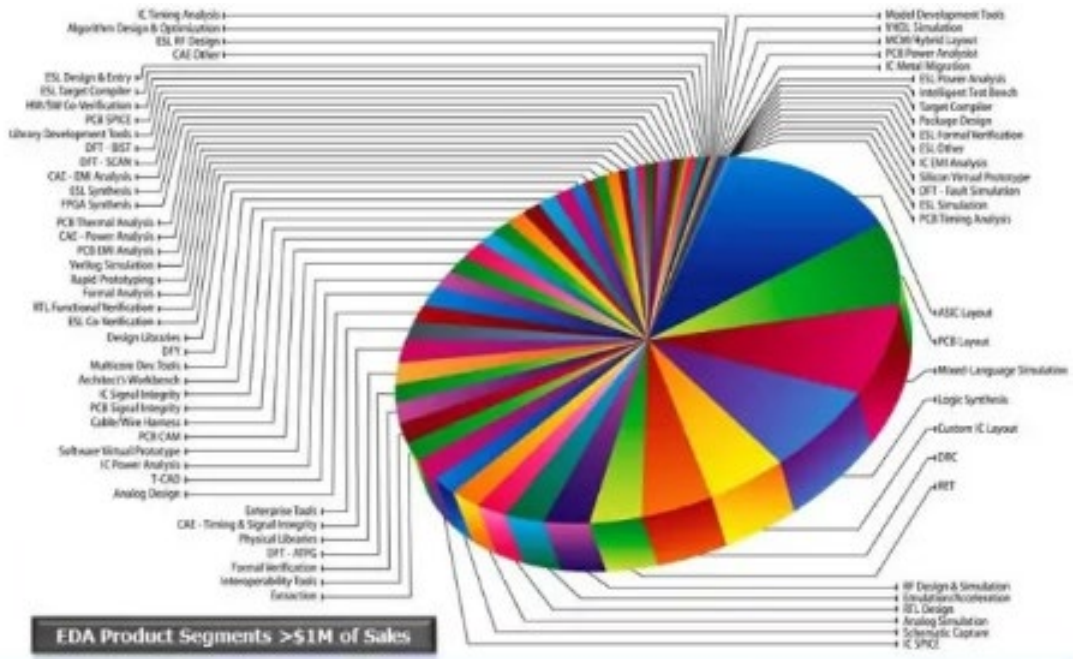
- **Response:** Electronic Design Automation (EDA)
  - Constantly innovating to keep up with technology
  - Three companies represent 75% of all revenue
  - Average EDA company (excluding the Big 3) generates $2 million annually



# EDA Industry



Source: Mentor Graphics



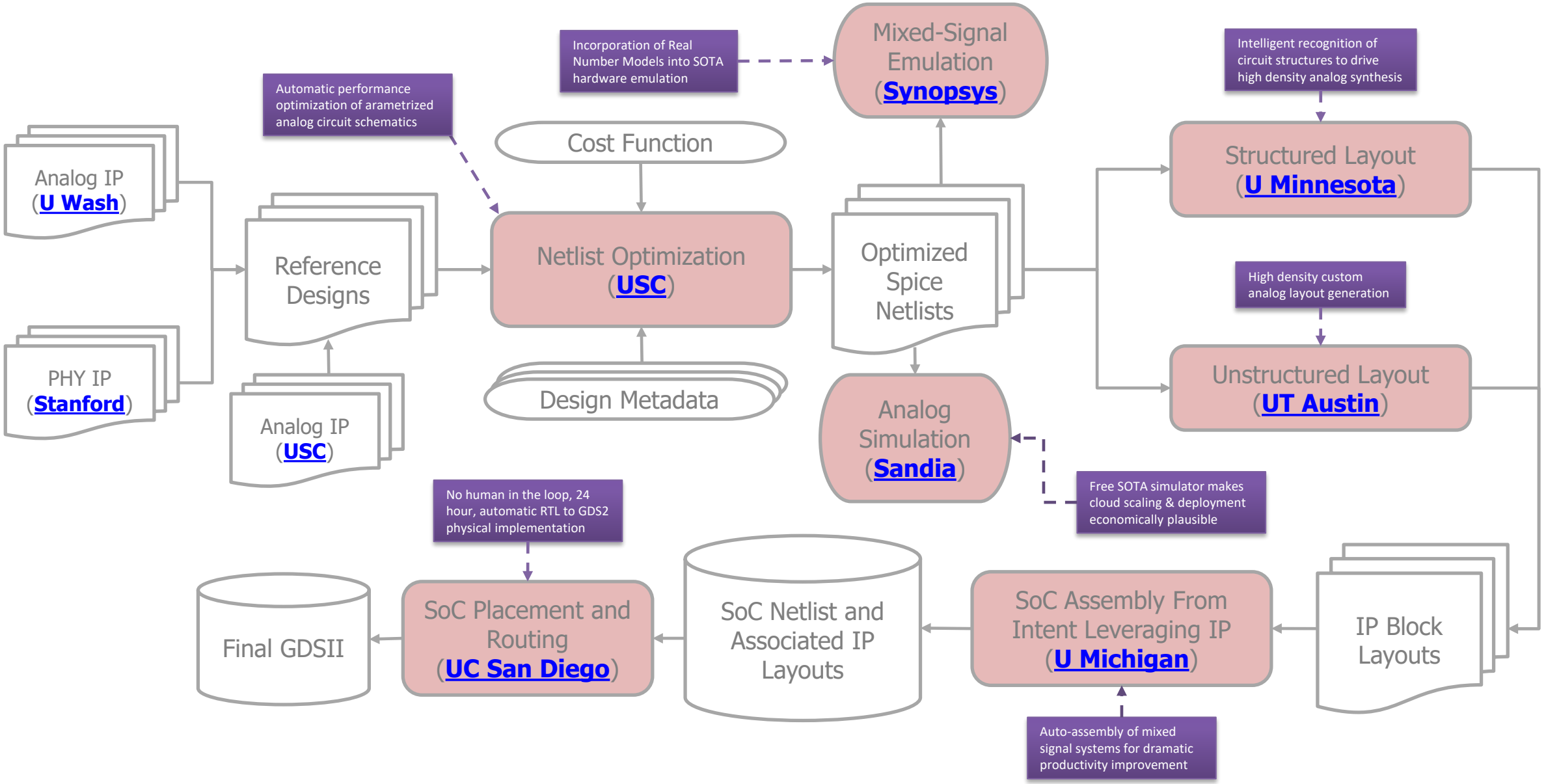
Source: Mentor Graphics

- EDA market has always had 3 major companies and MANY small startups that are likely to be acquired by the Big 3
- Occasionally a challenger (Viewlogic, Avanti, Magma) grows to $100M+ in revenue only to be acquired
- There are many segments and the Big 3 normally allow the start-ups to explore the new markets before acquiring
- EDA startups can't attract venture financing as they can only grow to about $10M before needing a global sales channel
- These forces result in **high prices** and **innovation stagnation** and there have been few transformative technical advances since 1988

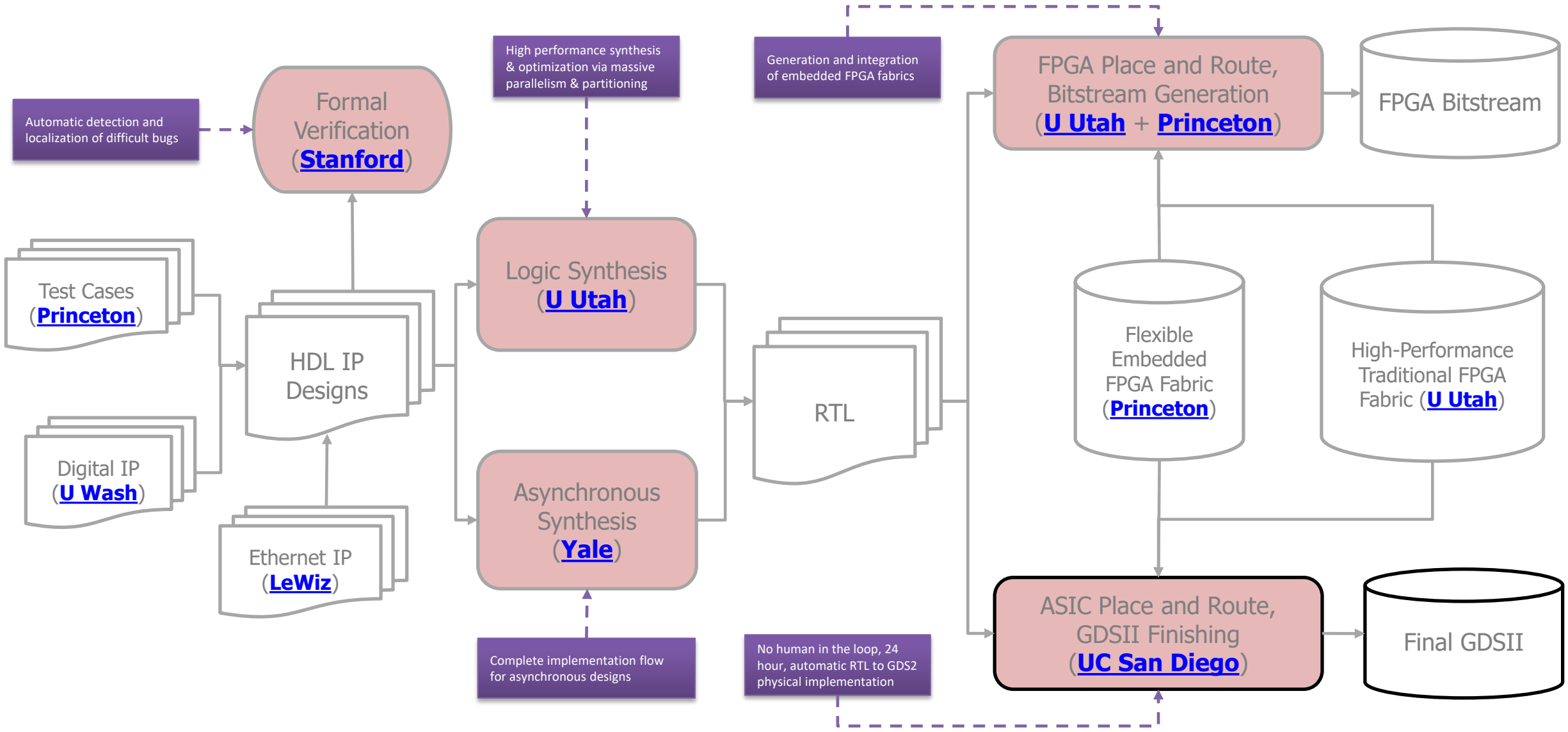
**Can DARPA improve access and fuel advances through open-source EDA technologies?**

**Economics** **Innovation**

# IDEA/POSH Analog Flow

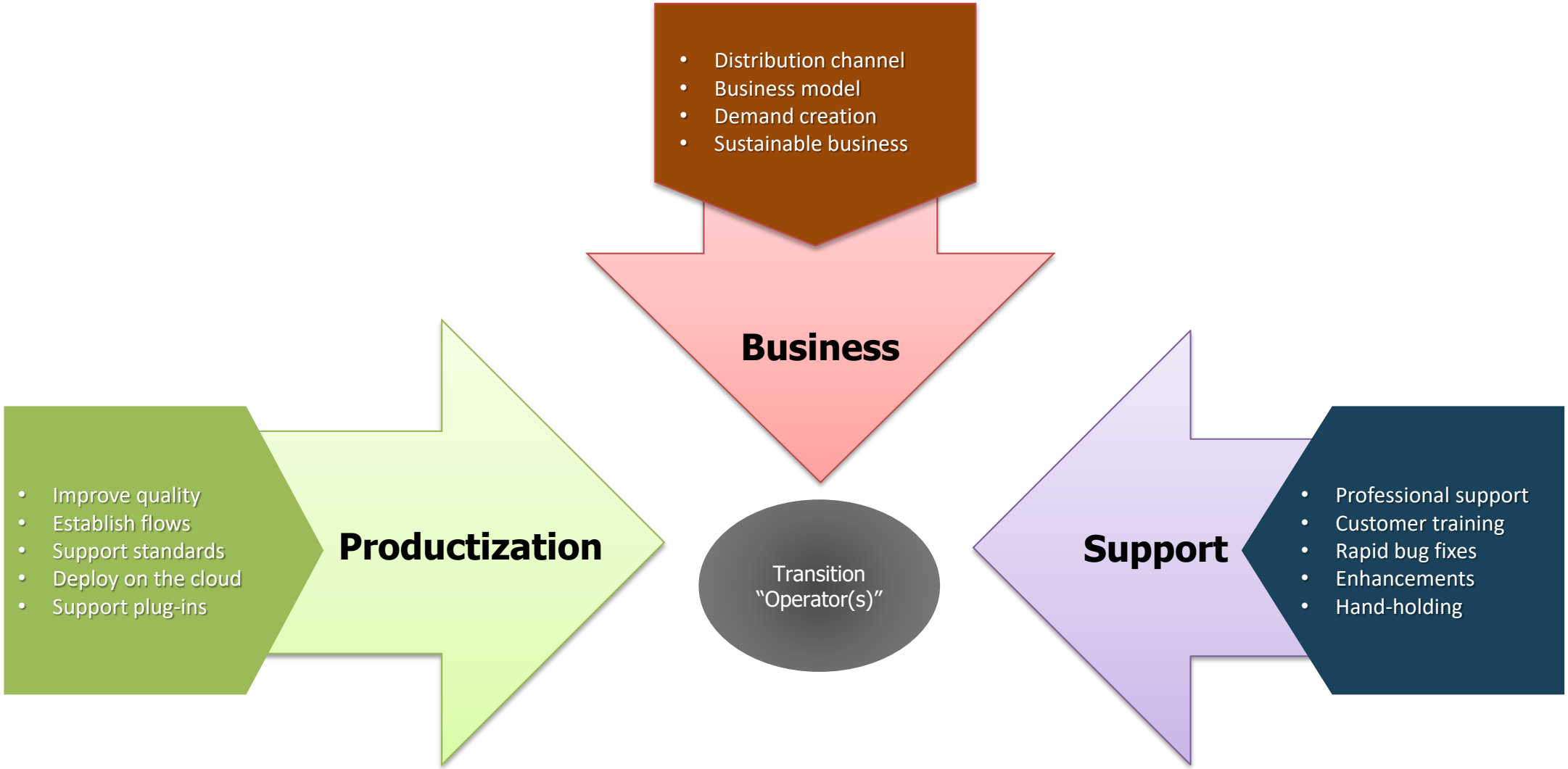


# IDEA/POSH Digital Flow



# Possible Transition Strategy

Enable **creation & initial operation** of entities capable of sustained & scalable **delivery & support** to the government & commercial customers of **productized, cloud-based EDA & IP solutions** originating from open source



# Open Source EDA Business Strategies and Operator Types

**Cloud-based deployment is essential for performance scaling and to limit adversary access**

- **Horizontal** – solutions that appeal to multiple market segments and use cases
  - Broad – Develop a comprehensive EDA/IP business to directly challenge the Big 3 across all flows
  - Narrow – Productize full or partial digital or analog flows or sub-flows

- **Vertical** – individual products or packages to address specific markets and use cases
  - Broad – Productize a sub-flow for customers with perceived design similarities (ex: analog for Gov't Labs)
  - Narrow – Productize a collection of tools an IP for a specific use case (ex: mixed-signal for Electronic Warfare)

**Small EDA PCB Company as an Operator**
- Leverage existing support infrastructure
- Expand business into chip design tools
- Use current distribution channel
- Piggyback on-going demand creation activities

**Defense Contractor**
- Create in-house flows to support internal needs
- Select relevant technologies and adapt
- Support in-house promotion and deployment
- Establish a semi-custom in-house tools

**DoD Domain Specialist Company**
- Construct a flow around particular domain
- Productize only tools relevant to the domain
- Productize domain-relevant IP
- Develop and deliver specialized training & support

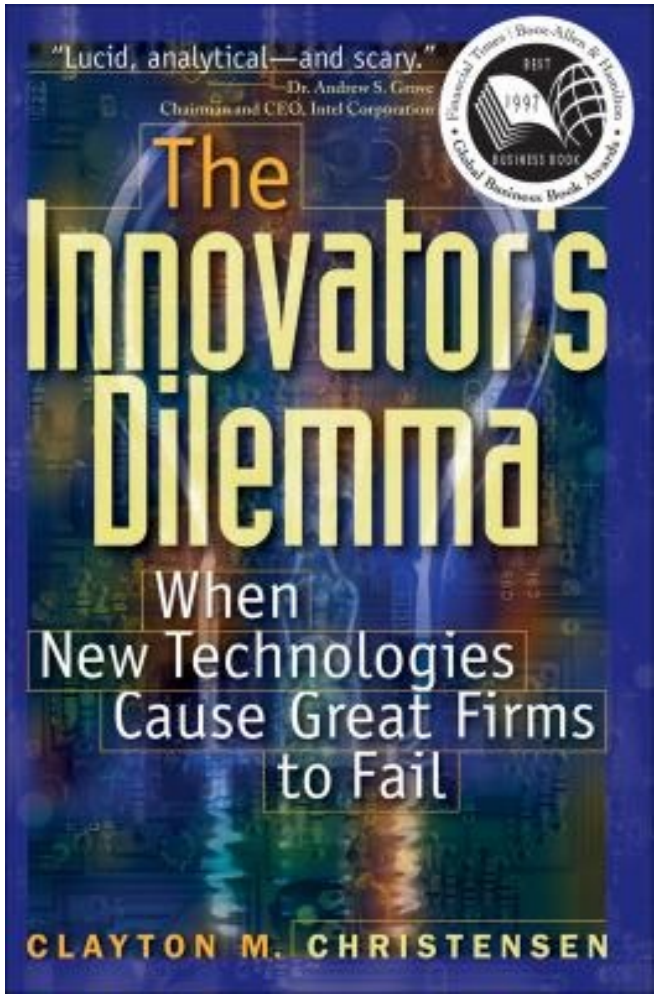
**Major Cloud Provider as an Operator**
- Loss leader to drive cloud utilization growth
- Use only digital marketing strategies
- Build a team to drive and fund next gen EDA
- Outsource support to offshore operators

**Specialty Design Services Company**
- Identify and industrialize relevant products
- Integrate into flows and combine with IP
- Develop packed products and deliver training
- Use services to drive product business

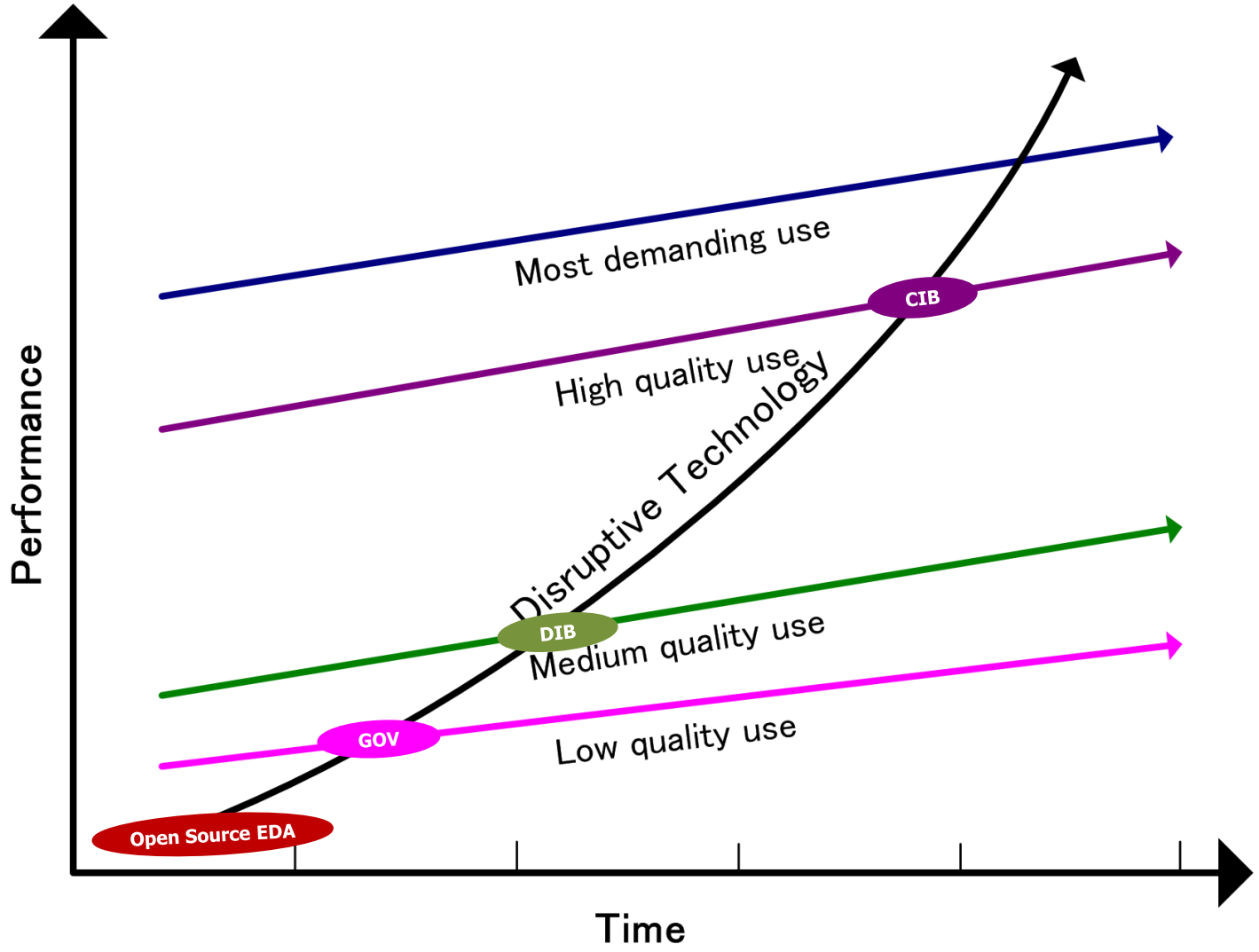
**Open Source Distributor**
- Productize standalone point tools
- Selection may be based on greatest interest
- Develop subscription centric business models
- Provide curation and facilitation services

# "Innovator's Dilemma" Disruption Strategy?

Government Ecosystem → Defense Industrial Base (DIB) → Commercial Industrial Base (CIB)




Source: www.amazon.com




# OPENFPGA:

## OPENFPGA: FROM POSH/IDEA TO THE OPEN-SOURCE FPGA FOUNDATION

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

# PIERRE-EMMANUEL GAILLARDON

**PROF. AT THE UNIVERSITY OF UTAH**
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT

# WHY OPENFPGA?

- FPGA is essential to modern high-performance computing systems

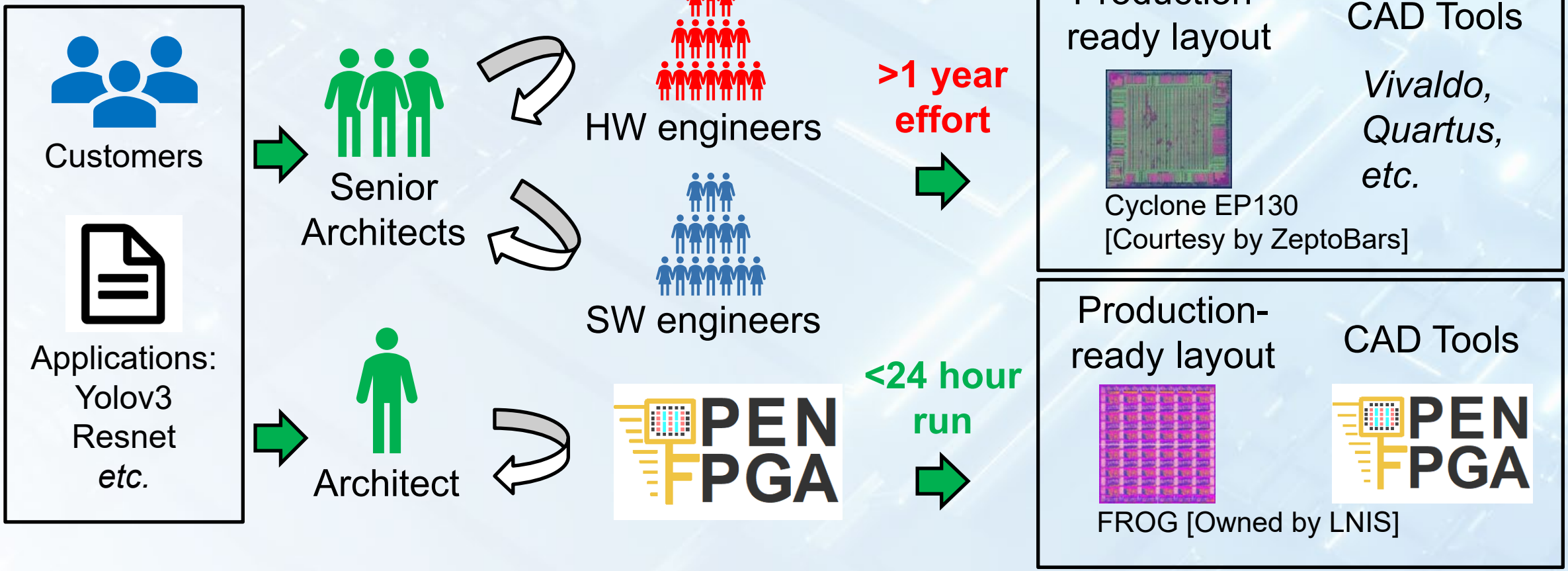
Wired and wireless communications

Audio and video broadcasting

Data center

- Domain-specific applications may demand on a specific type of computing resources of FPGA
  - AI applications are typically DSP-hungry
  - Commercial FPGAs could be sub-optimal since they are tailored for generic applications
- Designing FPGA fabrics is traditionally a cumbersome process
  - Considerable manual layout (Groups of hardware engineers)
  - Ad-hoc design tool development (Groups of software engineers)
  - **Year-long development cycles**

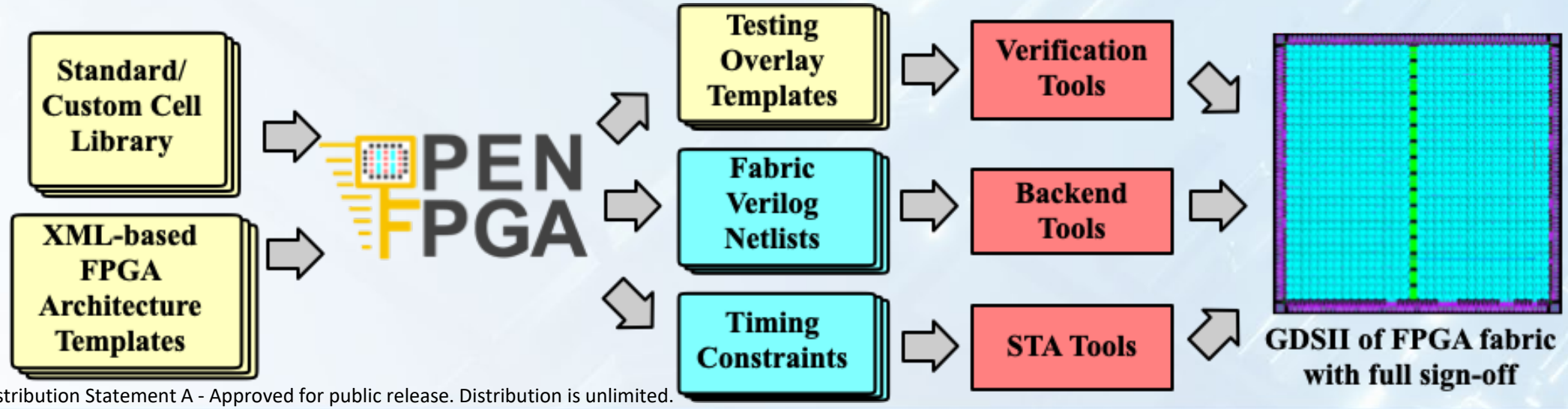
# WHY OPENFPGA?




- Complete FPGA and eFPGA generation (4 tape-outs in 2020)
- Fully customizable modern architecture (100+ tested)
- Optimized for fast physical design (150k-LUT+ FPGA requires < 24 hr)

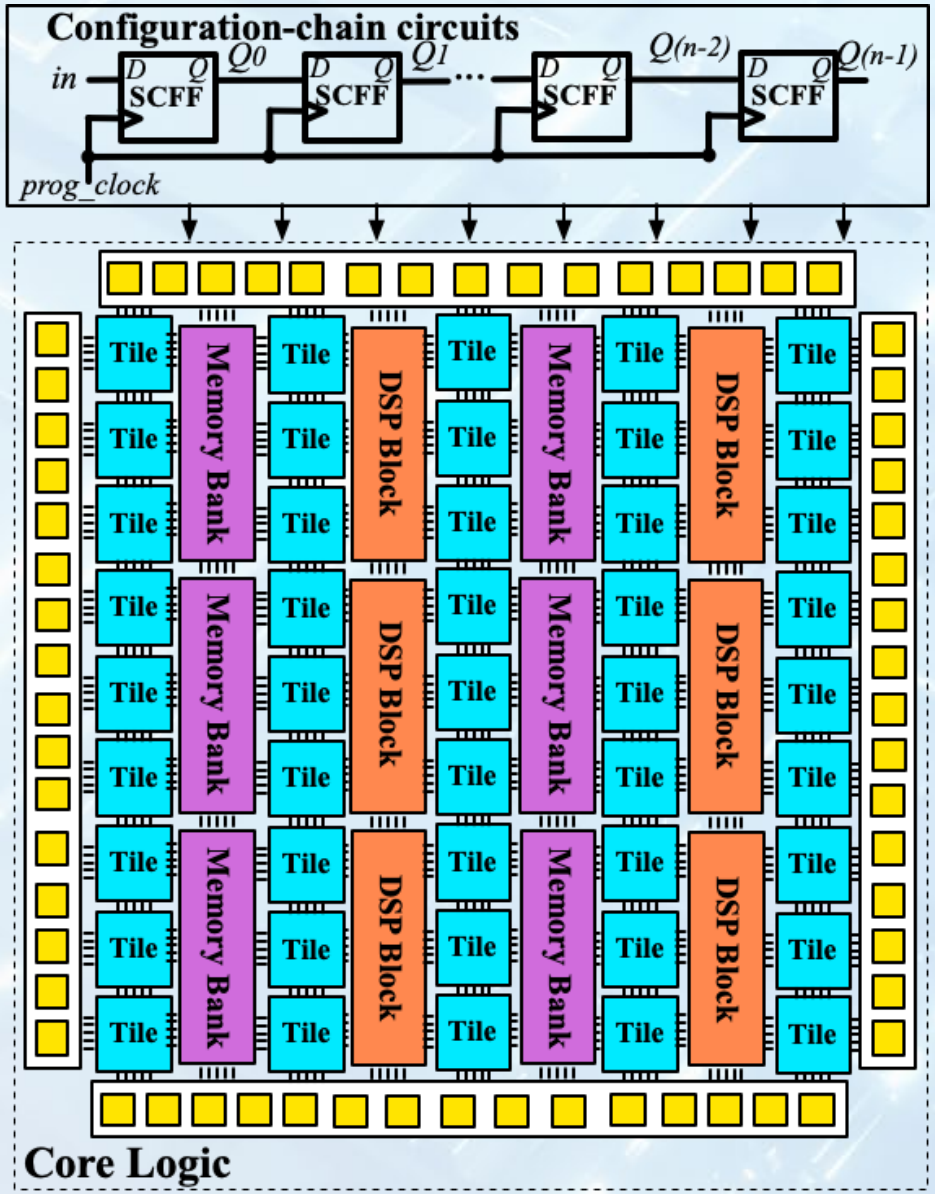
# AUTOMATIC FPGA PROTOTYPING

- Abstracting the design complexity of FPGA fabrics using high-level description
  - Achieved FPGA layout up to 32×32 array size
  - Tested PDKs: GF12nm, 130nm; TSMC 40nm, 180nm; ASAP 7nm
  - Verilog generation: ~5 minutes
  - Bitstream generation: a few sec.
  - Backend runtime: <24 hours
- Out-of-the-box Verilog-to-Bitstream support for users
  - Auto-tuned for customized architecture



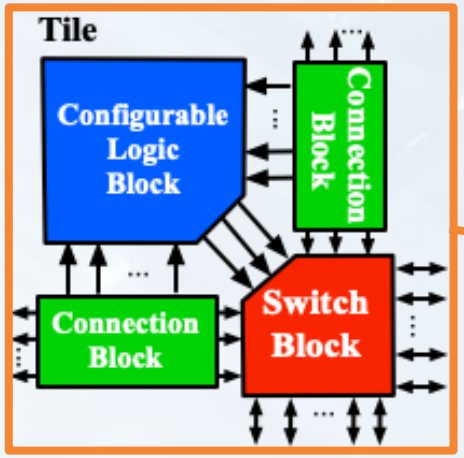
# HOW CUSTOMIZABLE IT COULD BE?

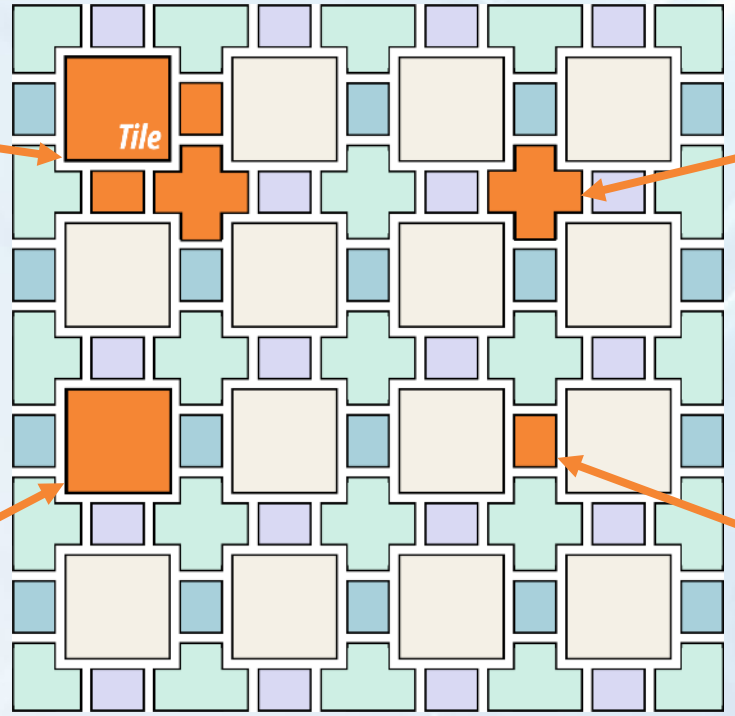
- **Portable across technology nodes**
  - Days of workload (was ~1 year in conventional ways)
  - Opportunities in radiation-harden FPGAs
- **Heterogeneous and Homogeneous FPGAs**
  - FPGA chip/chiplets
  - Embedded FPGA (eFPGA)
- **Versatile multi-mode CLB architectures**
  - Fracturable Look-Up Tables
  - Fully customizable interconnecting patterns
- **Versatile tileable routing architecture**
  - Multi-length wires
  - Mixed interconnecting patterns
- **Flexible Function Block (FFB)**
  - Block RAM (BRAM)
  - DSP Block
  - Any other user-defined IPs

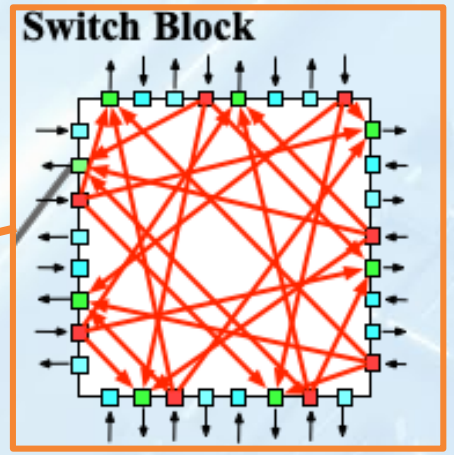


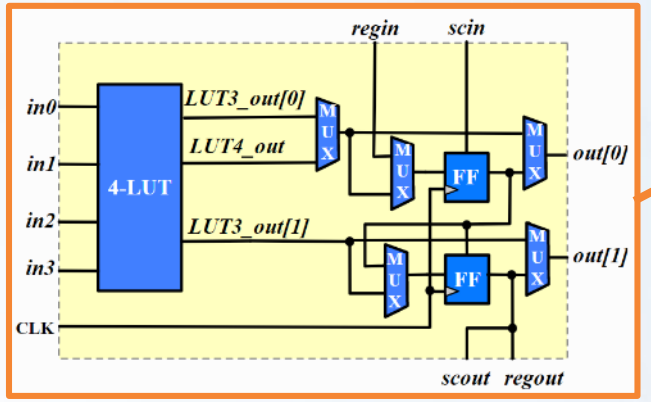
# PHYSICAL DESIGN OF THE FPGA FABRIC

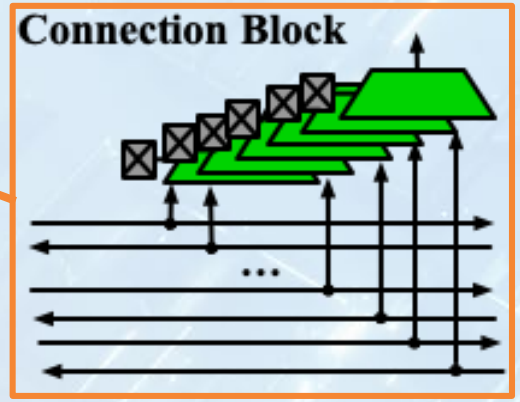
- Island-style tillable homogeneous FPGA architecture
- This can be easily extended to heterogeneous  architecture



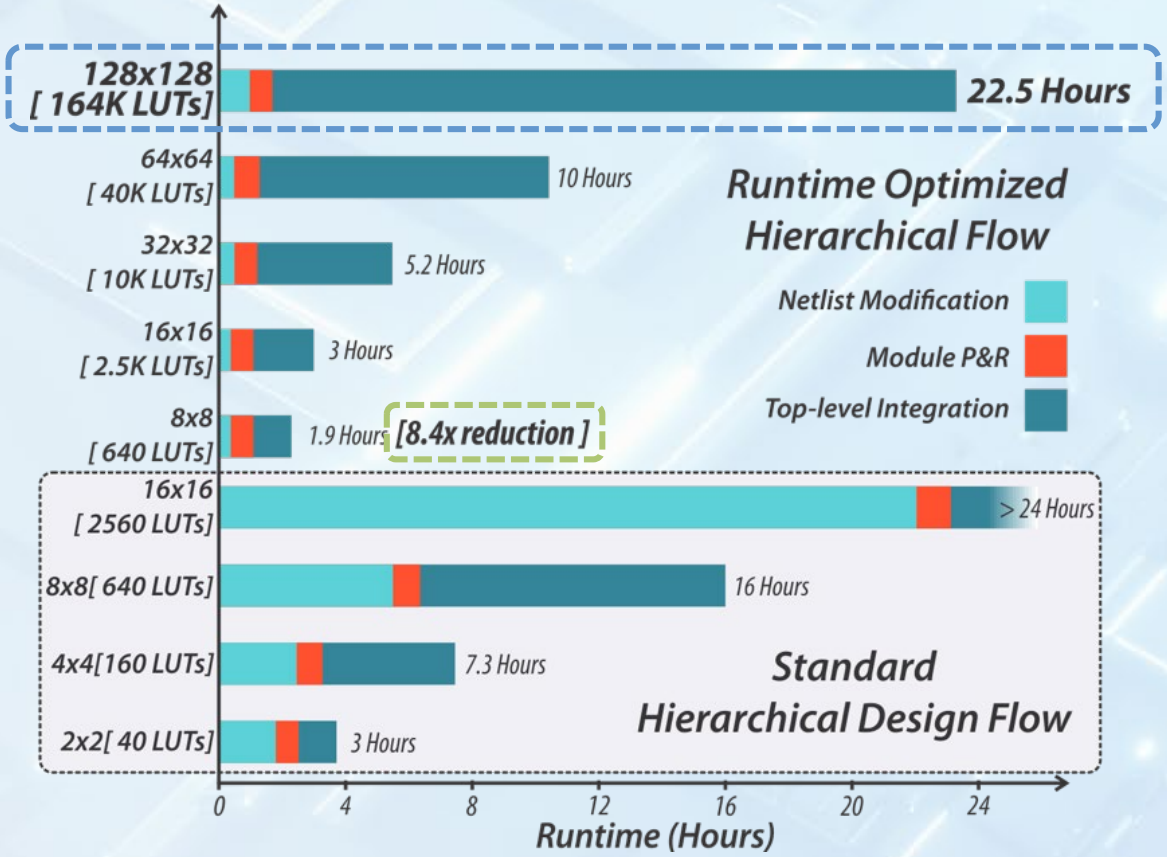



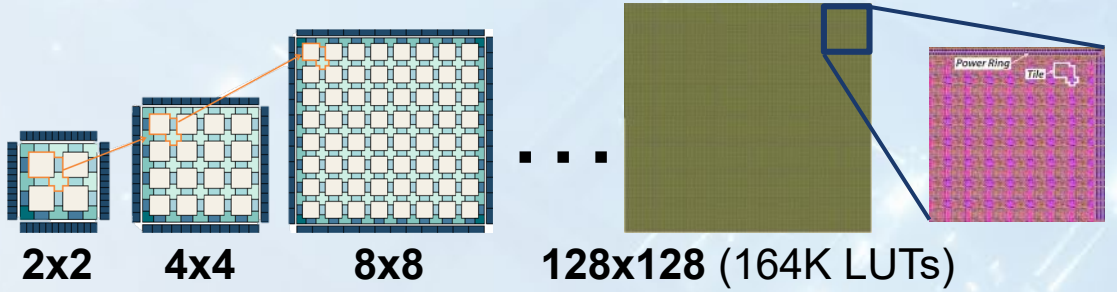



# RUNTIME AND PERFORMANCE METRICS

- Over **8.4x** runtime improvement for small fabrics (8x8 with 640 LUTs)
- **100K+** LUTs design achievable in **<24hours**



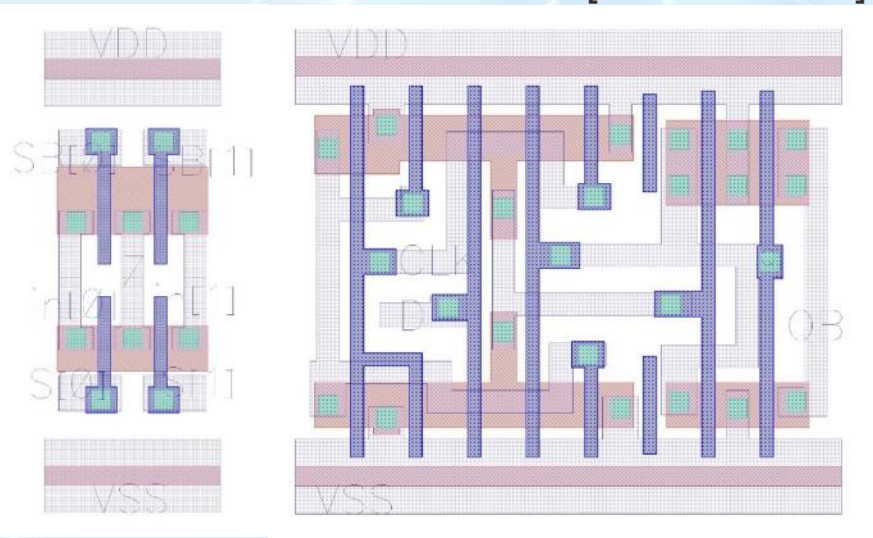

***Ref:*** *Ganesh Gore, et.al. A Scalable and Robust Hierarchical Floorplanning to Enable 24-hour Prototyping for 100k-LUT FPGAs.(ISPD '21)*

# ROAD TO HIGH-PERFORMANCE FPGAS

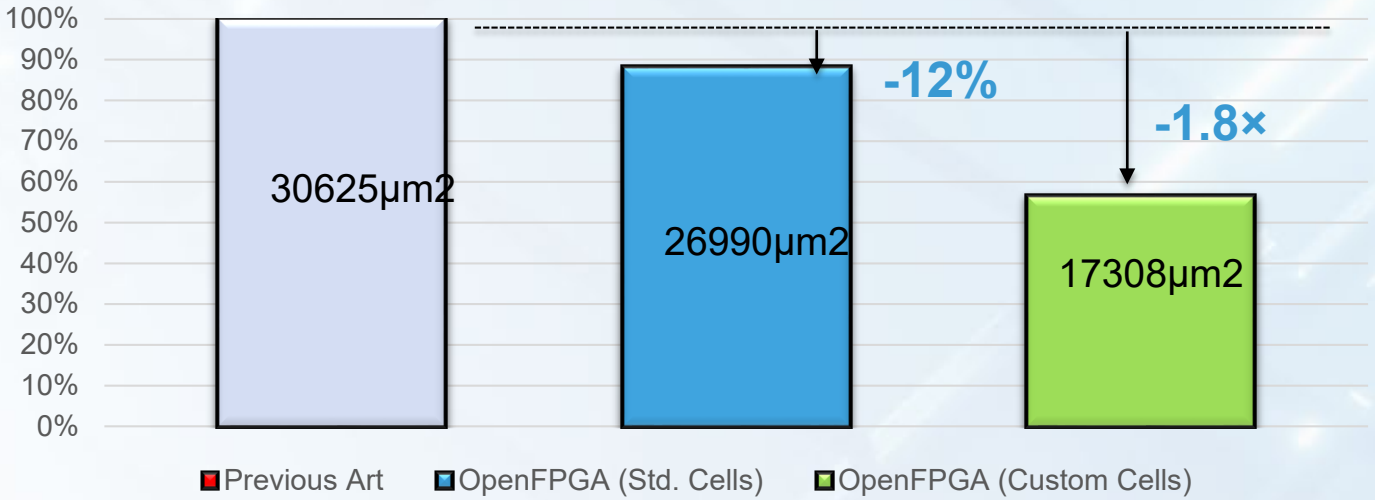
## OpenFPGA optimizes the critical blocks of FPGAs

- 90% of the FPGA is made of:
  - Transmission-gate-based multiplexers
  - Configuration chain flip-flops (CCFFs)
- Post tech. mapping technology allows to construct complex elements out of few custom standard cells

[Author's Own]




MUX2 CCFF



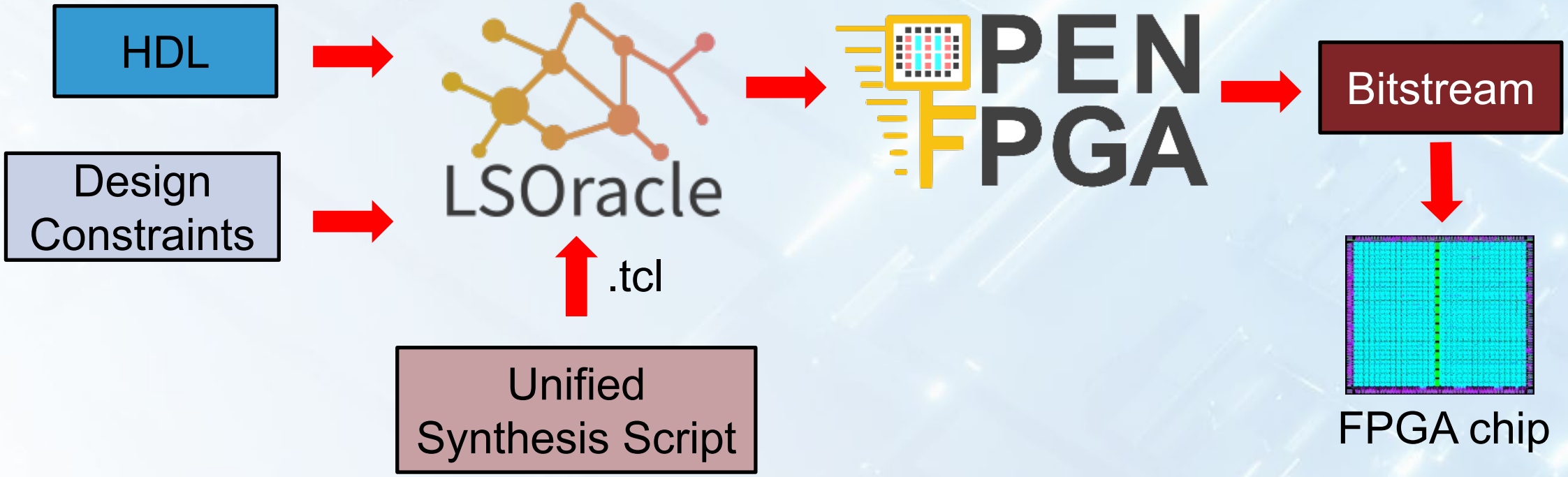

Area per tile

**2× area reduction**
**3× delay improvement!**

[1] B. Grady et al., Synthesizable Heterogeneous FPGA Fabrics, IEEE International Conference on FPT, 2018, pp. 1-8.

# END-TO-END EDA SUPPORT

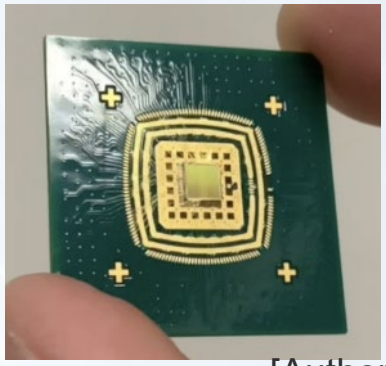
- Open-source Verilog-to-Bitstream support for end-users
  - Non-recurring engineering on EDA toolchains for every FPGA
  - Continous QoR improvement empowered by community support



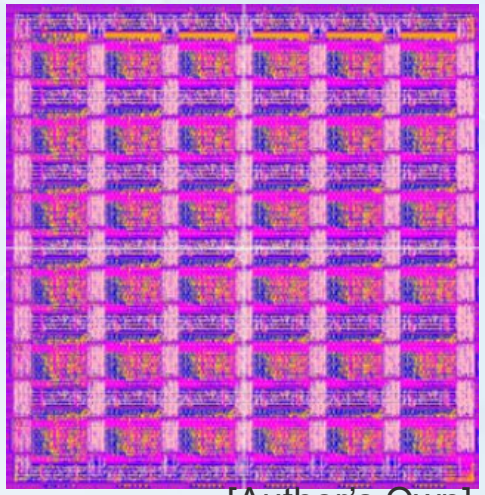
# OPENFPGA IS SILICON PROVEN

## *FROG – First Reconfigurable Open-source Gate array*

***12nm GlobalFoundries***
***Effort 2.5 person.month***



[Author's Own]



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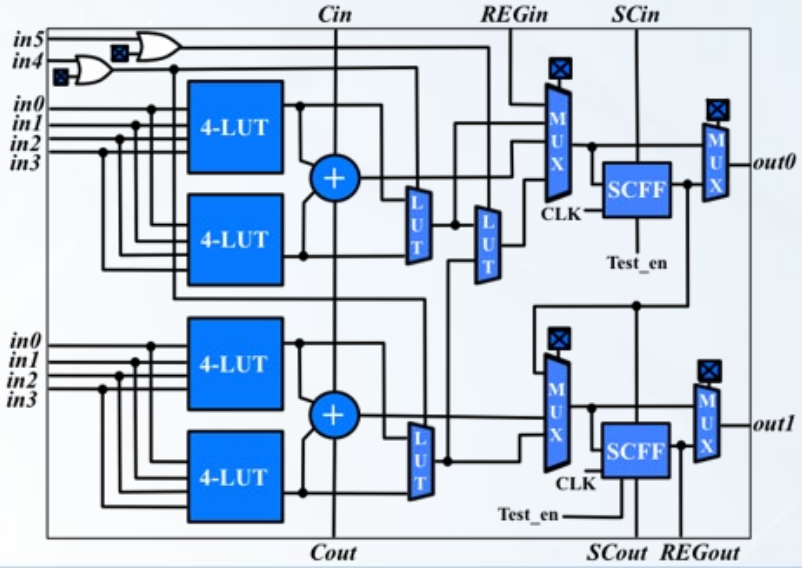
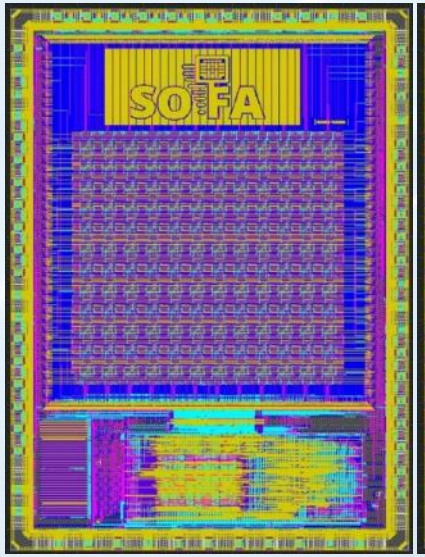


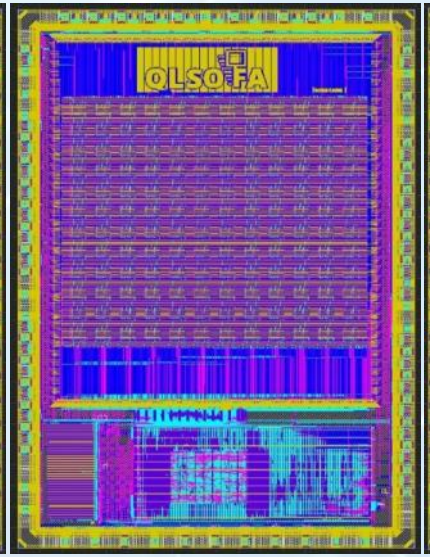

Modern logic element architecture

## *SOFA – Skywater Open-source FpgA*

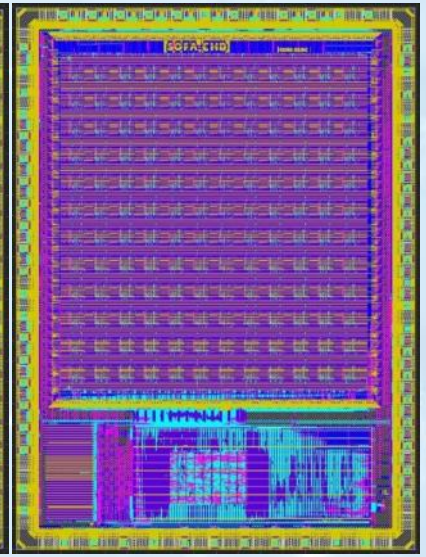
***Google + Efabless.com***
***Integration to Caravel SoC***
***130nm Skywater***
***Effort 1 person.month***




SOFA HD
**Base design**




QLSOFA HD
**Arithmetic-enhanced**




SOFA CHD
**Performance-optimized**

# THE OPENFPGA PROJECT

- **OpenFPGA** is a **leading open-source FPGA IP generator**
  - Support highly customizable FPGA architecture design
  - Provide most complete open-source EDA support
  - Enable 24-hour development cycle to prototype FPGAs
- **Open-Source FPGA foundation** launched in March 2021
  - Democratize FPGA technology by providing an open, user-focused, and collaborative environment
  - OpenFPGA is a project under the OSFPGA

OPEN FPGA **is now part of** OSFPGA FOUNDATION

**OpenFPGA Github**: https://github.com/lnis-uofu/OpenFPGA
**Open-Source FPGA Foundation**: https://www.osfpga.org

# WHY OPENING A FOUNDATION?

Technology alone doesn't guarantee adoption!


But a healthy ecosystem does

## QuickLogic Announces Australis™ eFPGA IP Generator

-- Built on the OpenFPGA open-source framework that enables rapid prototyping of customizable FPGA architectures

-- Integrates QuickLogic's best practices for performance, power, and area optimizations, ensuring low risk and low cost for eFPGA IP licensees

-- Automation capability enables custom-parameterized eFPGA IP within days in some cases


# AN OPEN-SOURCE ASIC FLOW FOR ASYNCHRONOUS LOGIC

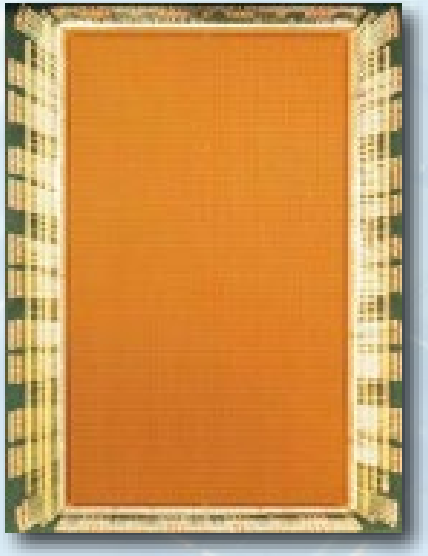
This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

# RAJIT MANOHAR

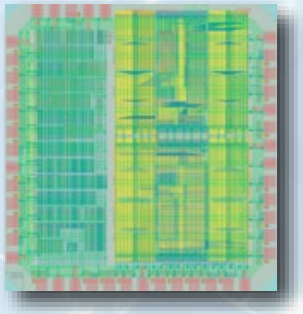
**YALE UNIVERSITY**
COMPUTER SYSTEMS LAB

# ASYNCHRONOUS LOGIC

- **Many design examples demonstrating benefits**
  - … but only limited adoption
- **How were these chips designed?**
  - "Very carefully…."
  - Hand design (full custom) : too time-consuming for a modern ASIC
  - "Fake out" synchronous tools
    - Error-prone
    - Every logic family is different
    - Inaccurate timing
    - Restrict components used
- **Enormous effort v/s standard synchronous logic**



TrueNorth neuromorphic chip

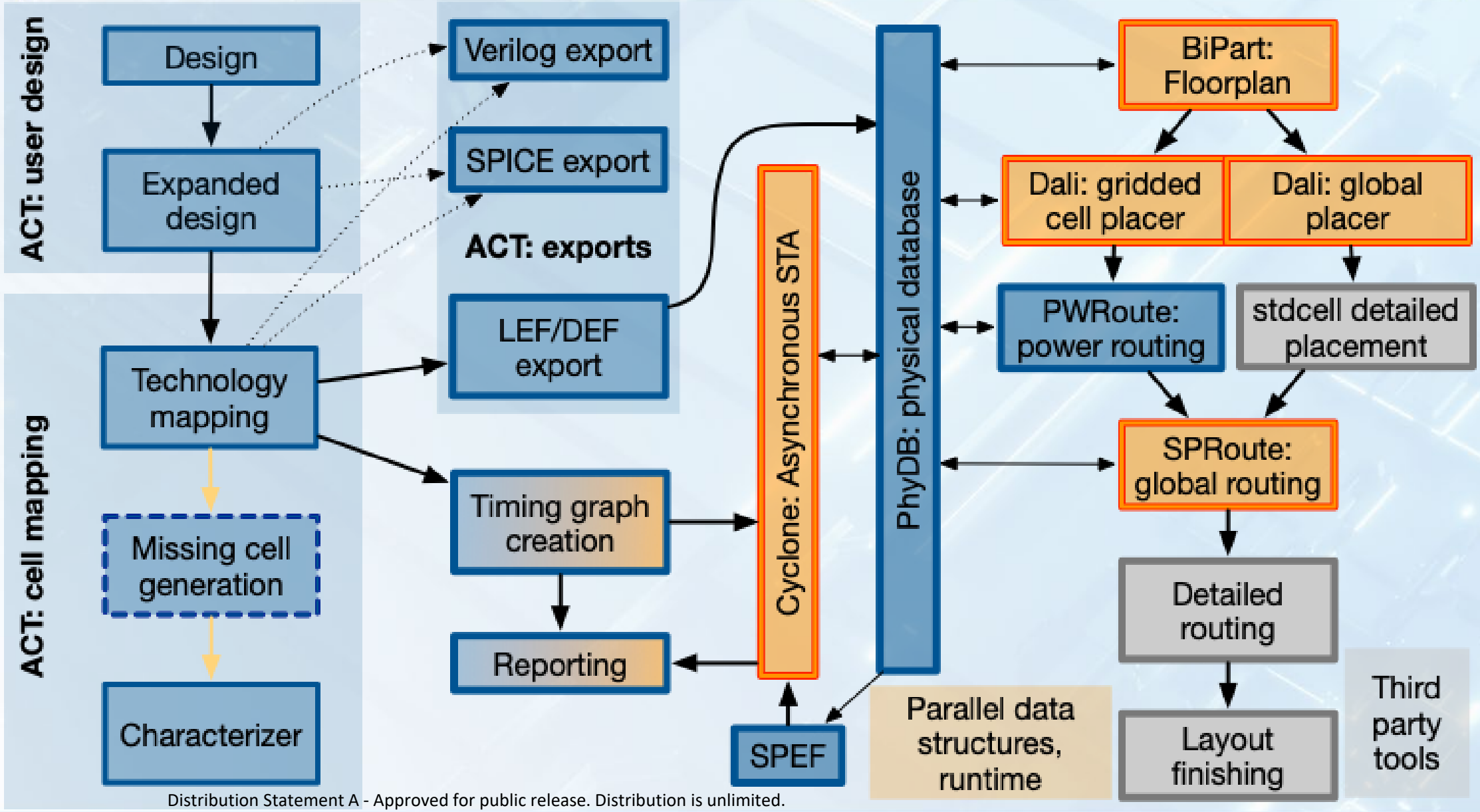


ULSNAP event-driven CPU

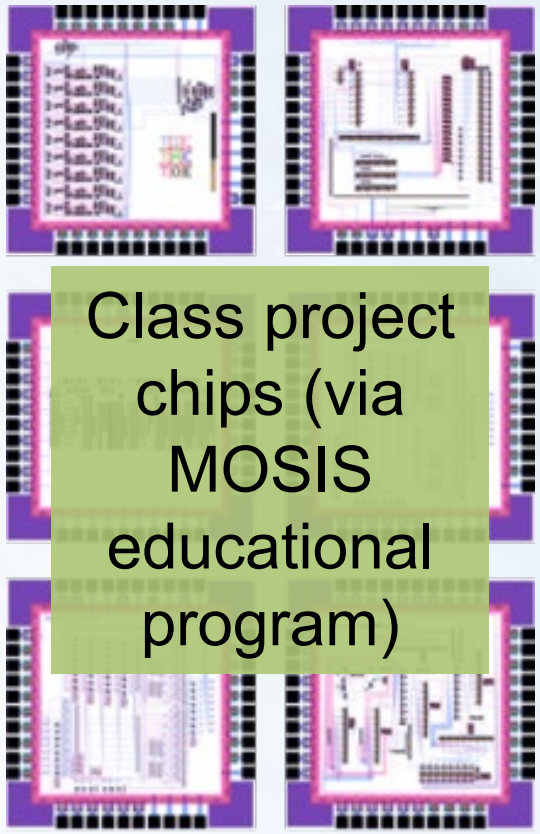
# AN ASIC FLOW FOR ASYNCHRONOUS LOGIC

- Why now?
  - Enabling theory for asynchronous circuits
    - Recent results on universal timing constraints
    - Recent results on timing analysis theory for asynchronous circuits
  - Maturity of design methodology
    - Convergence of circuit families
- Why open source?
  - Stagnation of major changes in the industrial EDA community
  - A clean-slate implementation

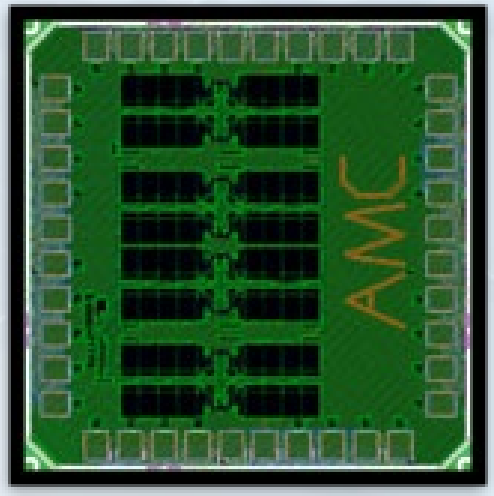
# KEY COMPONENTS DEVELOPED



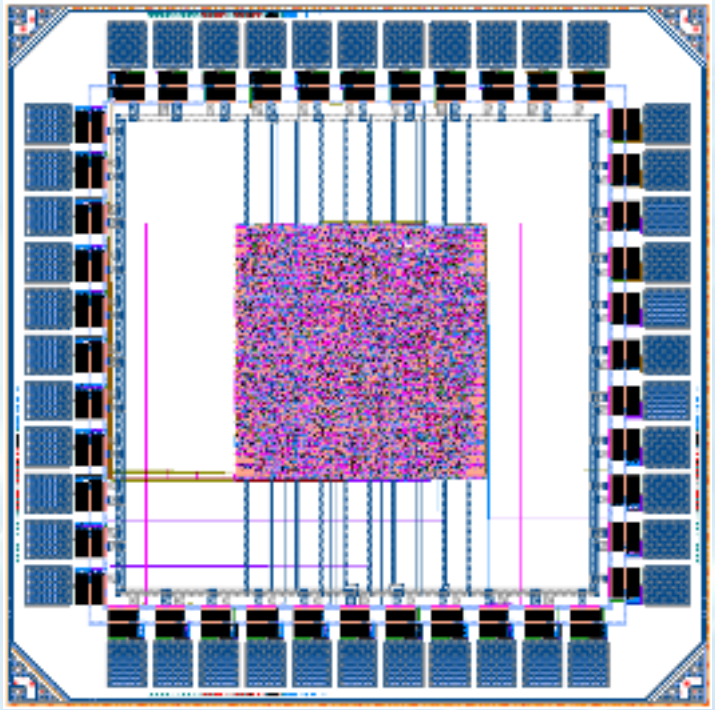
# TAPE OUTS WITH THE FLOW



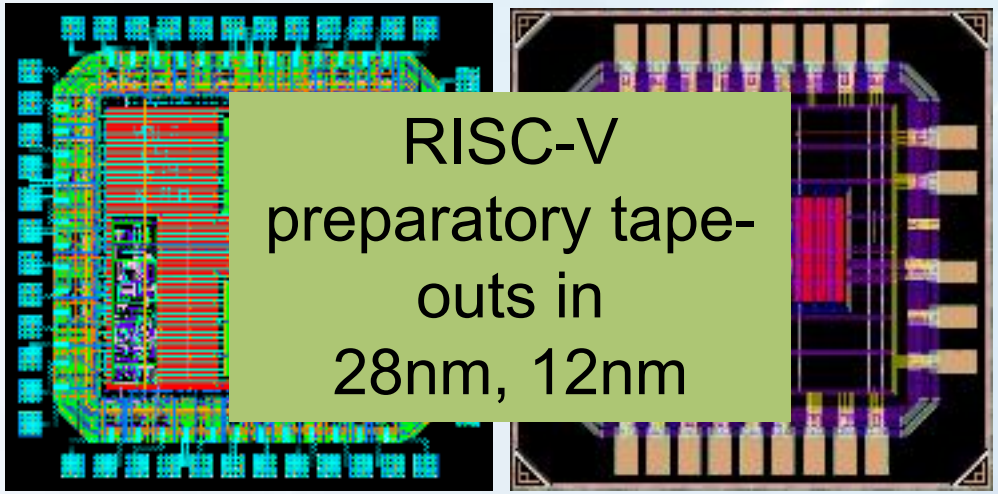
Class project chips (via MOSIS educational program)




Memory validation (65nm)



First 65nm tape-out with ASIC flow (async stack machine)



RISC-V preparatory tape-outs in 28nm, 12nm

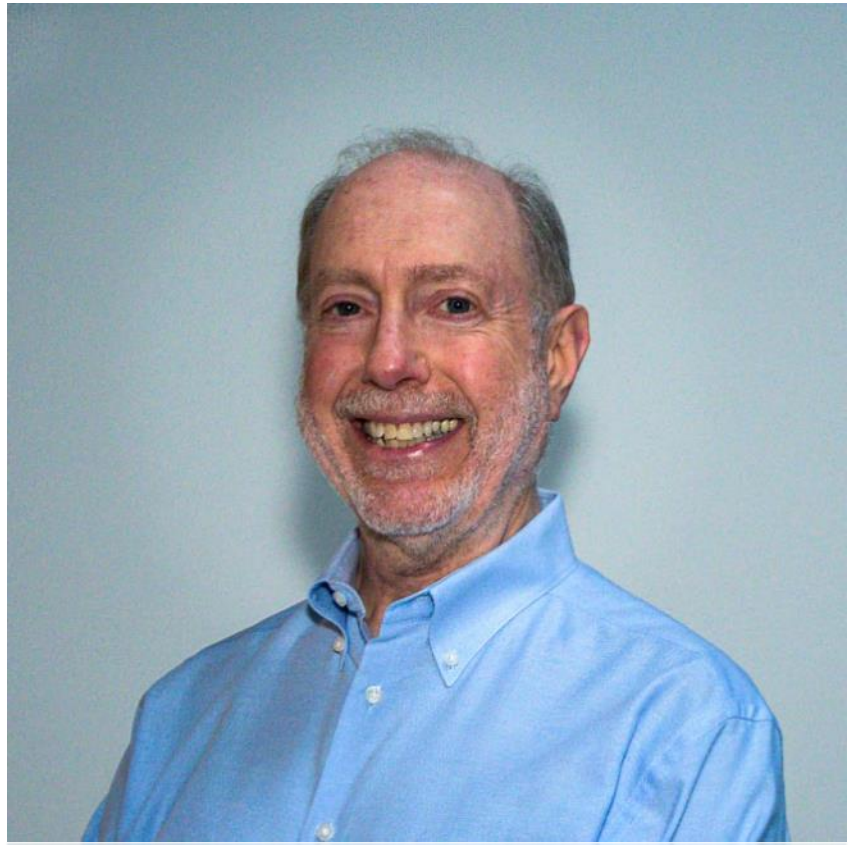
In progress: Skywater 130, sub-10nm

# TRANSITION POSSIBILITIES

- Non-option #1 : traditional EDA company
- Option #2 : standard software model
  - Freemium : open-source software, charge for support
- Option #3 : services
  - Example: optimize power consumption of a component
  - Design service to improve metric X
- Option #4 : enabling technology for asynchronous IP and soft cores
- Option #5 : chip company enabled by tools
  - Pick an application domain where asynchronous shines


# ACCELERATING AMS SOC VERIFICATION PERFORMANCE

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).



# DALE DONCHIN

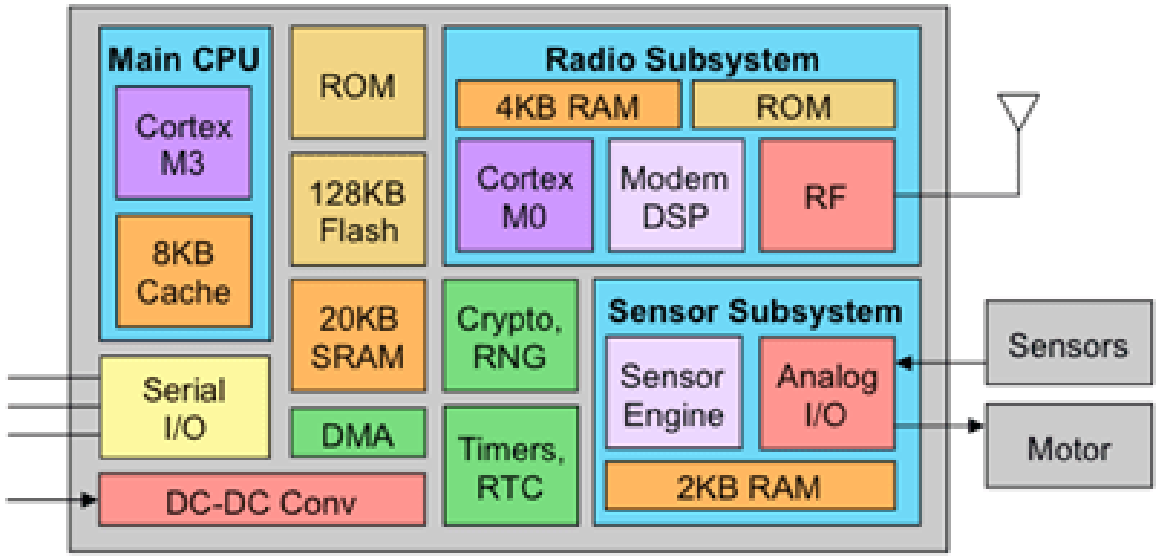
**SYNOPSYS, INC.**
SENIOR PROGRAM MANAGER

# SOC VERIFICATION CHALLENGES

- Presence of many analog hardware components
- Firmware required to calibrate AMS components such as SERDES
- Need for full system (HW + SW) validation pre-silicon

R. Collett and D. Pyle, "What Happens When Chip-Design Complexity Outpaces Development Productivity," McKinsey & Company, Inc., 2013.

## Example: TI CC26XX




Source: The Linley Group, “Low-Power Design Using NoC Technology”; TI

# ANALOG VERIFICATION LAGS DIGITAL ADVANCES


Formal Verification

Static Verification


Debug for Design & Verification

High-Performance Simulation & VIP

Low Power

Source: Synopsys, Inc.

# RELATIONSHIP TO OPEN SOURCE

**Build** upon existing open industry standards

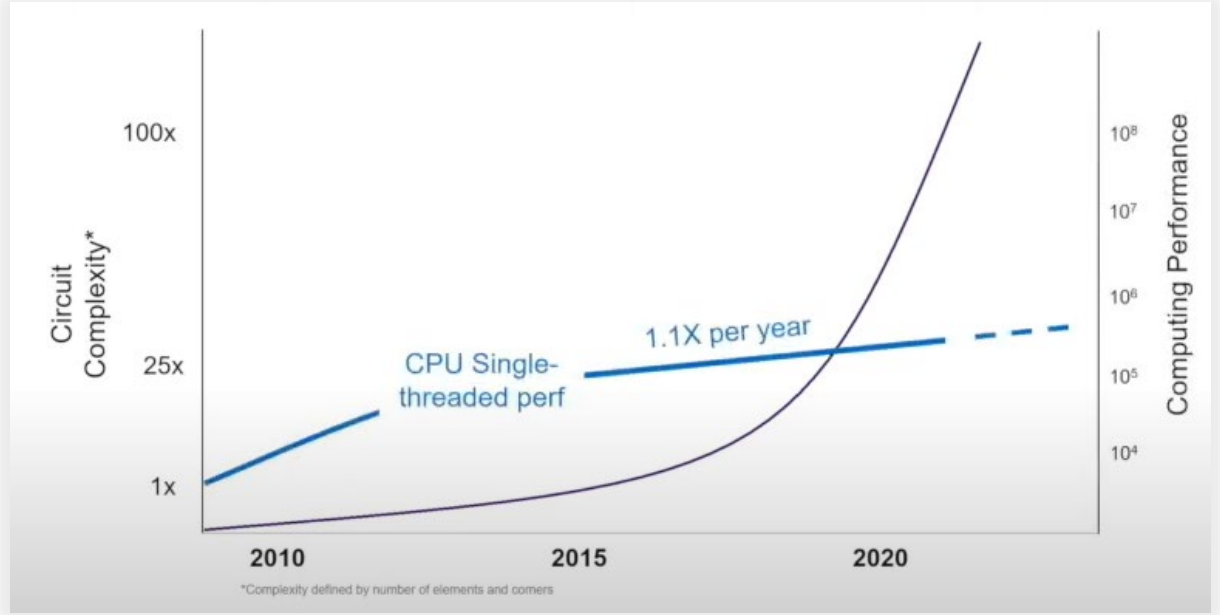
- Real Number Models
- SPICE netlist format(s)
- Waveform data representation

**Collaborate** with standards bodies where standards don't exist

- Work with Accellera to define AMS assertion syntax
- Propose open-source Python as language
- Enable open-source tool development based on approved standard

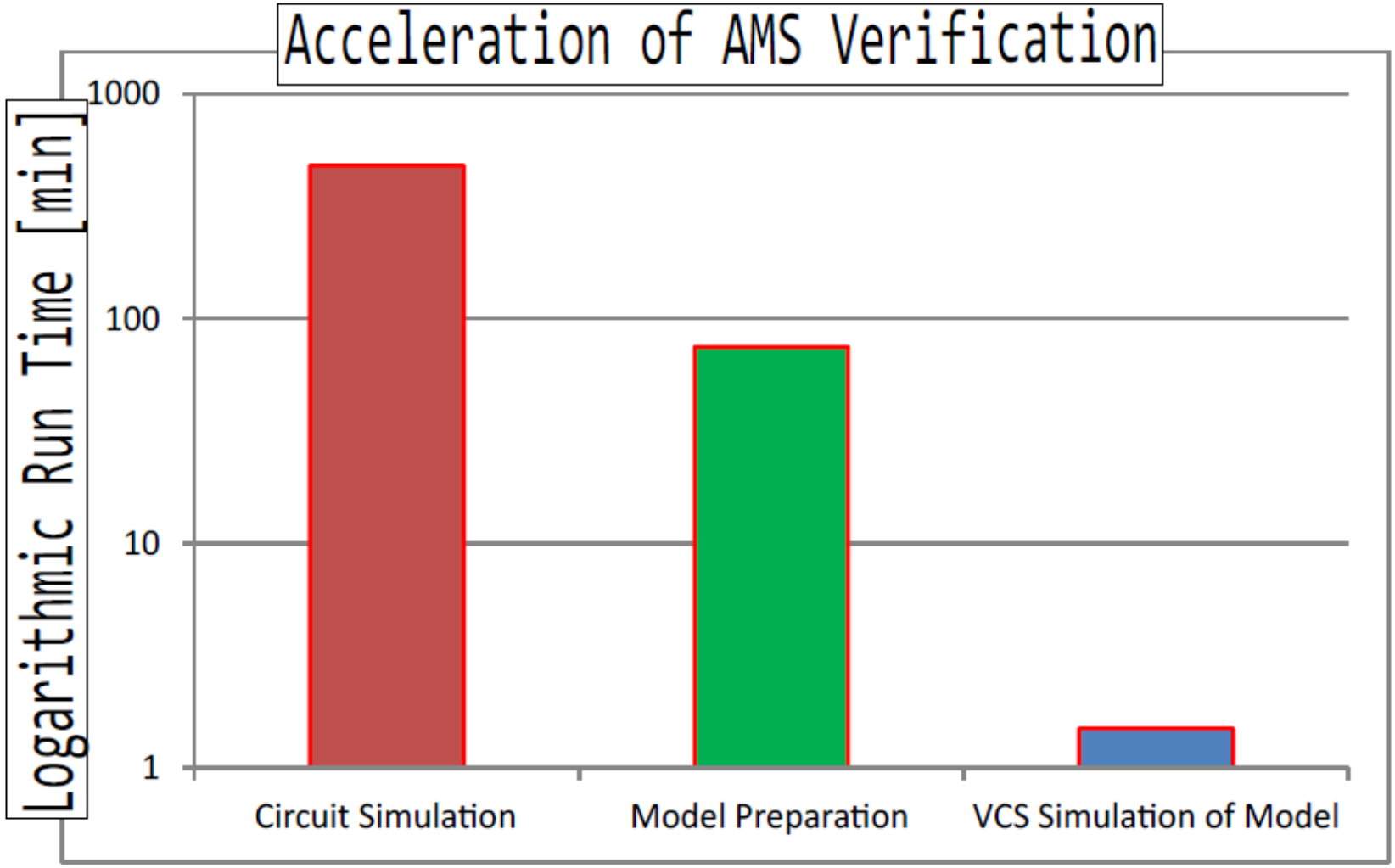
# ANALOG DESIGN VERIFICATION CHALLENGES

- Few significant speedups in SPICE analog solvers
- Many “Fast” SPICE tools are only “fast” relative to SPICE
- Difficulty verifying the analog circuitry operating with the digital design portion (AMS)




Source: Synopsys, Inc.

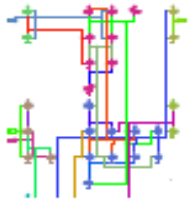
# NEW APPROACH TO AMS DESIGN VERIFICATION (1)




Source: Synopsys, Inc.

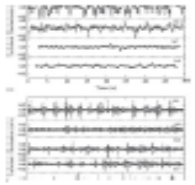
# NEW APPROACH TO AMS DESIGN VERIFICATION (2)

SPICE Netlist



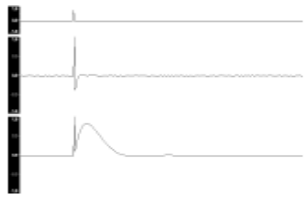
Specifications

Waveforms

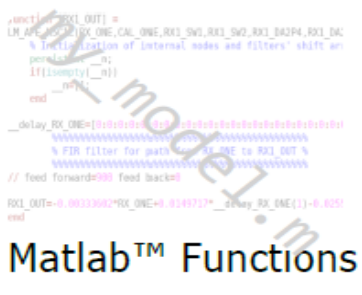


Behavioral Characterization

Test Bench



Matlab™ Functions



## High-Fidelity Surrogate Model


**Selectable model accuracy vs. model creation run-time**

Source: Synopsys, Inc.

# TYPICAL APPROACH TO AMS VERIFICATION

**VCS AMS** UVM Accellera SystemVerilog

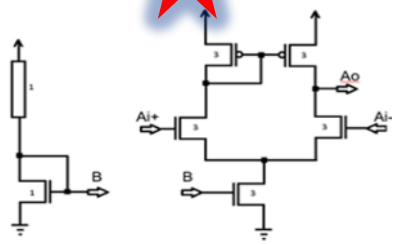
**VCS**
Functional Verification

**CustomSim**
FastSPICE Simulation

**RTL Digital Design**

```
module four_bit_comp (gt_out, A, B);
output       gt_out;
input  [3:0] A, B;

wire   [2:0] carry;
supply0      gnd;

one_bit_comp b0 (carry[0], A[0], B[0], gnd),
             b1 (carry[1], A[1], B[1], carry[0]),
             b2 (carry[2], A[2], B[2], carry[1]),
             b3 ( gt_out, A[3], B[3], carry[2]);

endmodule
```

**SPICE Transistors**



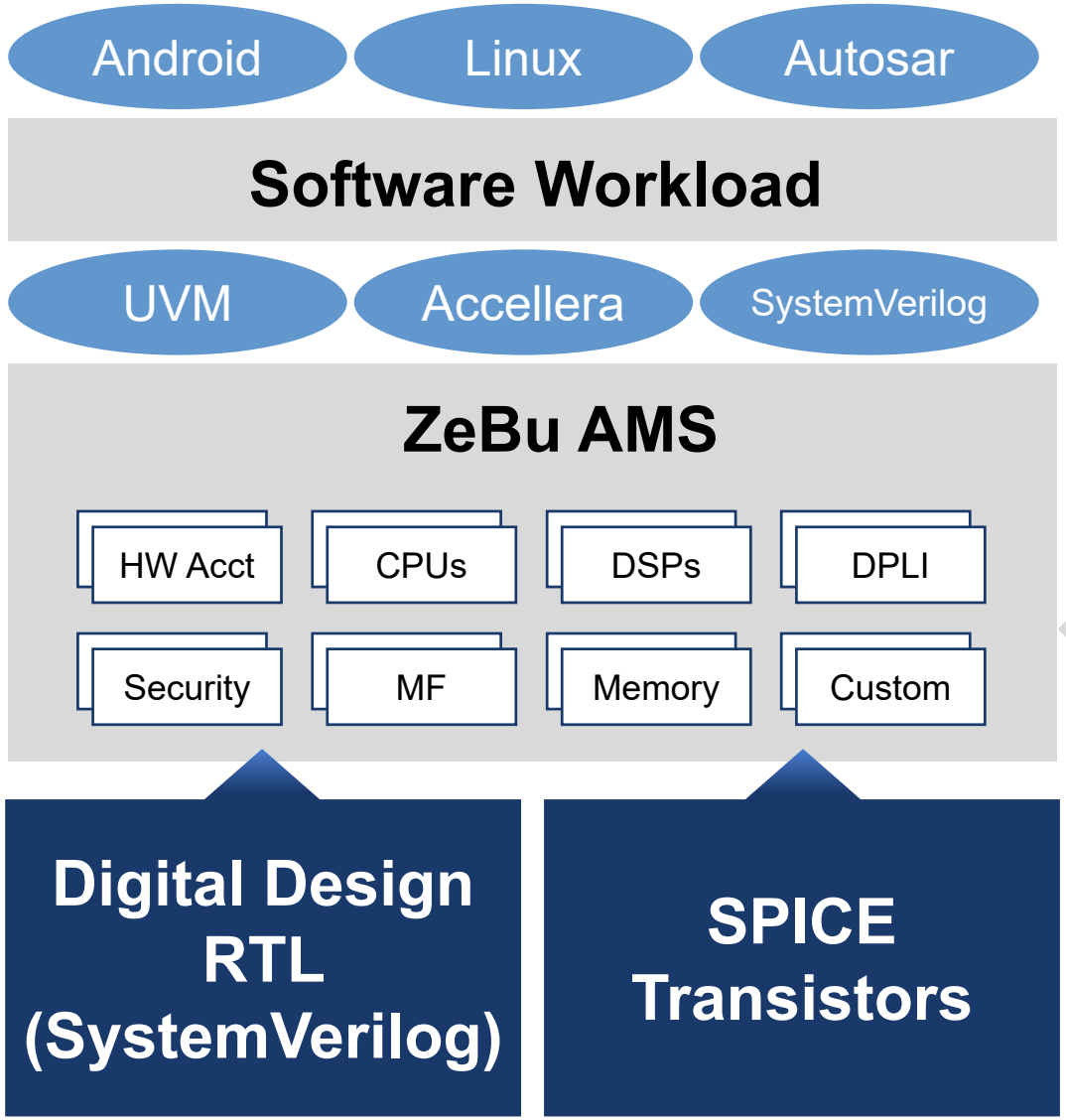

**Software?**

**Compute Farm**

Source: Synopsys, Inc.

# NOVEL APPROACH TO AMS VERIFICATION

**SW bring-up & HW/SW validation including analog circuits**



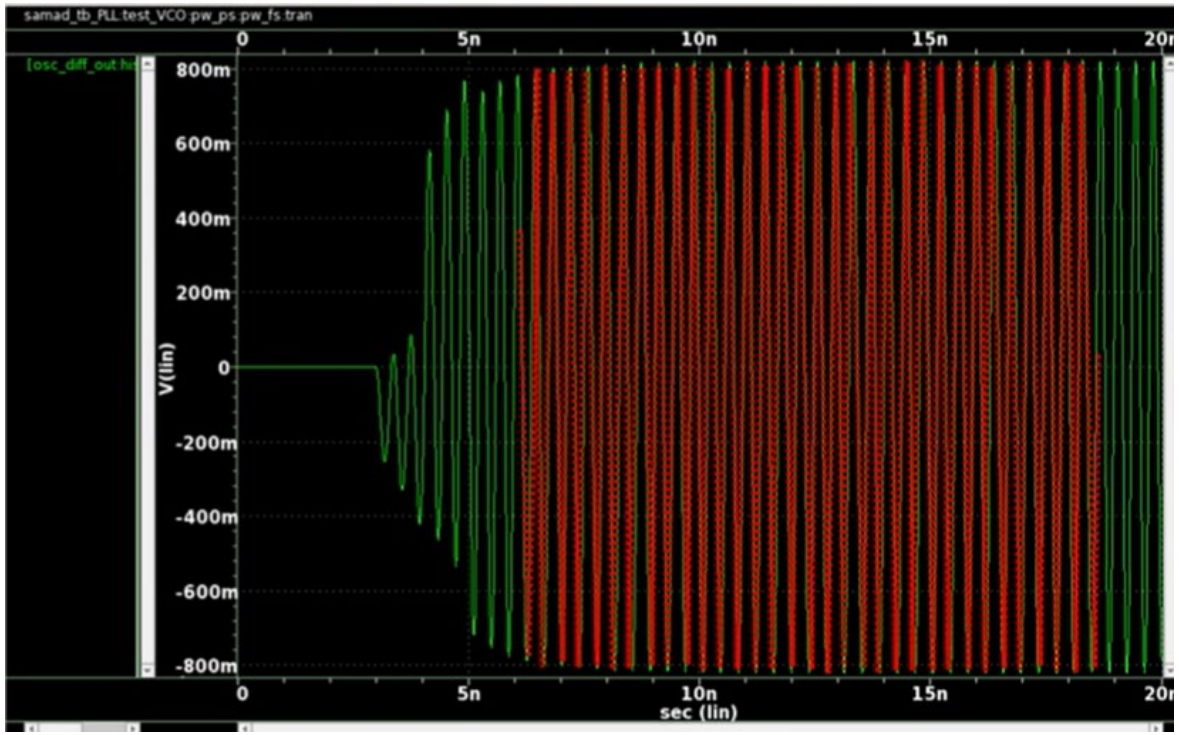

**Support mix of Verilog and analog behavioral models**

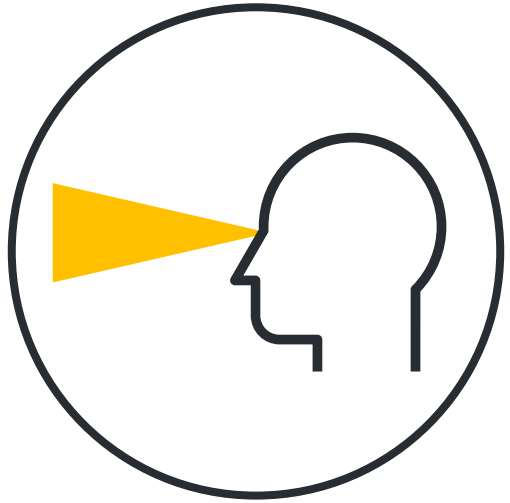
ZeBu Emulator

**Solutions for synthesis, partitioning, timing, and FPGA routing of AMS components**

Source: Synopsys, Inc.

# ANALOG DESIGN DEBUG IS VERY MANUAL



**Stare at Waveforms**

"Waveform debugging remains the primary means the design and verification community uses for investigating simulation failures"

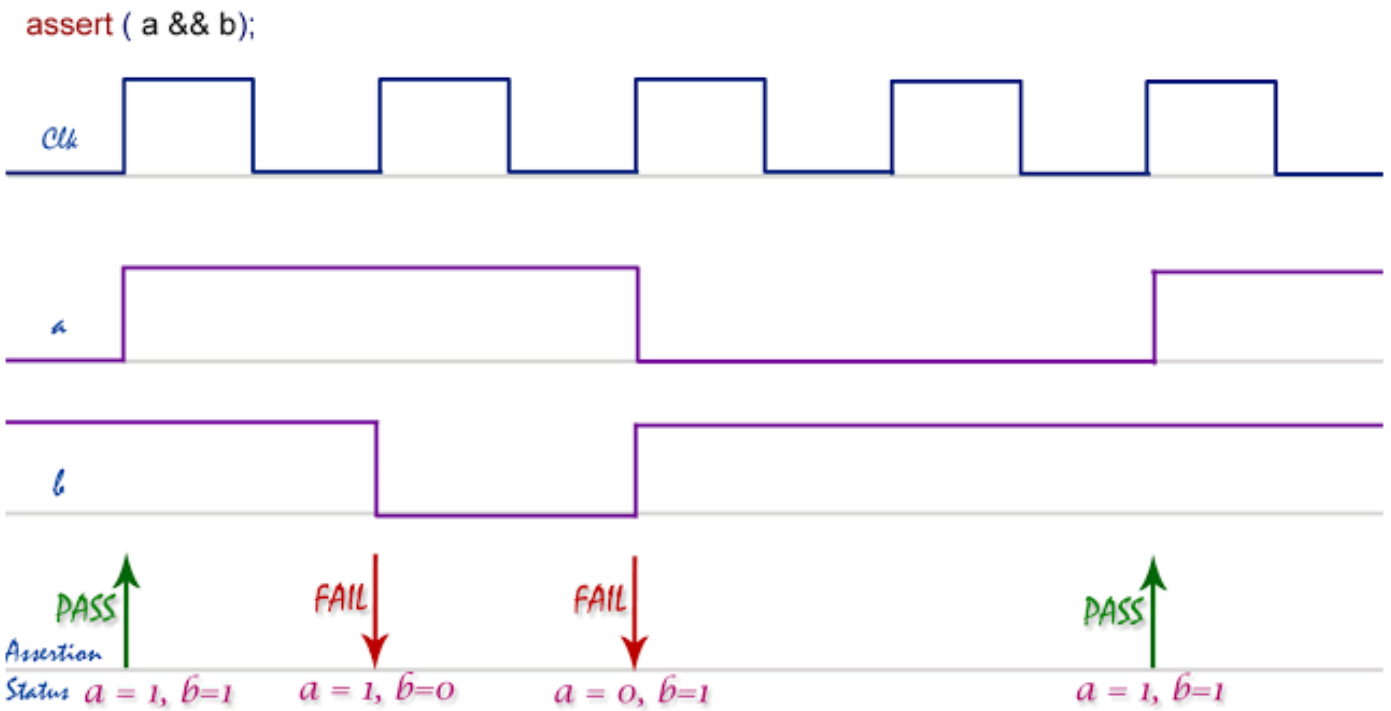
*Elevate Verdi Waveform Debugging with Python*, SNUG 2019

Source: Synopsys, Inc.

# ANALOG ENGINEERS NEED NOT APPLY

```
module asertion_ex;
  bit clk,a,b;

  //clock generation
  always #5 clk = ~clk;

  //generating 'a'
  initial begin
    a=1;
    b=1;
    #15 b=0;
    #10 b=1;
        a=0;
    #20 a=1;
    #10;
    $finish;
  end

  //Immediate assertion
  always @(posedge clk) assert (a && b);

endmodule
```

SystemVerilog



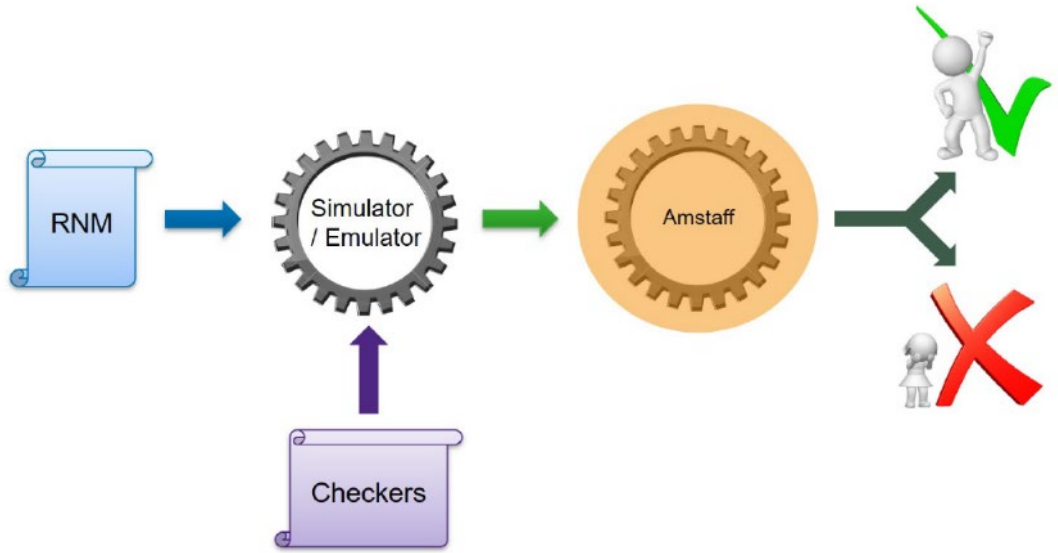

Source: verificationguide.com

# INNOVATION IN AMS DESIGN DEBUG

## Python-based specification language describing the desired circuit behavior in both the time and frequency domains

```
@analog_checker
class MyChecker:

    def __init__(self, sig):
        self.sig = sig
        # ...
        self.mean_val = mean(self.sig)

    @assert_temporal
    def RMS:
        self.rms = std(self.sig - 0.5)
        return self.rms < 0.01

ck = MyChecker(my_signal)
ck.check()
print(f'Average value = {ck.mean_val}, rms = {ck.rms}')
```

## Amstaff performs assertion checks concurrently with simulation/emulation




Source: Synopsys, Inc.

# INNOVATIONS IN AMS VERIFICATION

## Assisted Modeling

- Assisted SV Real-number model creation (DEGEM)
- Takes SPICE Netlist, Waveforms and Specification as input
- Emulation friendly synthesizable models with SV Data types

## Multi-Mhz Fast Emulation

- 100-100X faster than Simulation (ZeBu AMS), suitable for software driven validation
- Floating point support
- Accurate to support system level integration and HW/SW analysis

## Efficient Debug

- AMS assertion definition for AMS SPICE netlist (Amstaff)
- Concurrent and post-simulation analysis
- Graphical debug aids
- Wholistic coverage using unified verification management infrastructure

# PUTTING IT ALL TOGETHER

## Demonstrated 1.7MHz (150X Faster) with ZeBu

- ZeBu emulation for Real Numbers and Verilog transport delays
- Real-time debug with waveforms and assertions
- Proven with project at major US processor semiconductor company

- **Use modeling tool to convert SPICE circuitry to real number models**
- **Rapid hardware-assisted emulation of complete SoC including AMS, pure digital, and software**
- **Programmable, automated checks for proper design operation**


# OPENSOURCE EDA AT ARMY RESEARCH LABORATORY

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

# PETER GADFORT

**SILICON TECHNOLOGIES TEAM LEAD**

DEVCOM ARMY RESEARCH LABORATORY

# ARMY RESEARCH

## SILICON TECHNOLOGIES TEAM

# SMALL TEAM IN BIG EDA ECOSYSTEM

- The issues we face as a small Government team:
  - Lengthy and complex license negotiations
  - Time limited licenses and lengthy and unpredictable contracting actions makes lining up tapeouts and tools difficult
  - Substantial time overhead associated with each of these

- Opensource allows us focus on our research interests and apply resources towards tapeouts.
  - Not all roses, need to get new tools running with varying levels of documentation.
  - Sometimes requires substantial time investment to modify the tools.

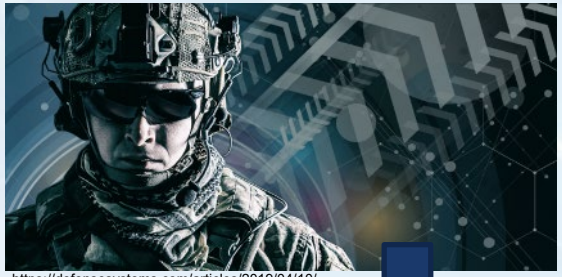
# ARL'S FOCUS AREA

## RECONFIGURABLE COMPUTING

# OPENSOURCE FPGAS FOR ARMY APPLICATIONS

Tune hardware to Army-specific needs

- Domain-specific IP
  - Electronic Warfare (EW)
  - Artificial Intelligence (AI)
  - Security
- FPGA size
  - Fine-grained control
  - Minimal unused FPGA resources
- FPGA Power
  - Extreme SWaP-C → Warfighter-borne implementation



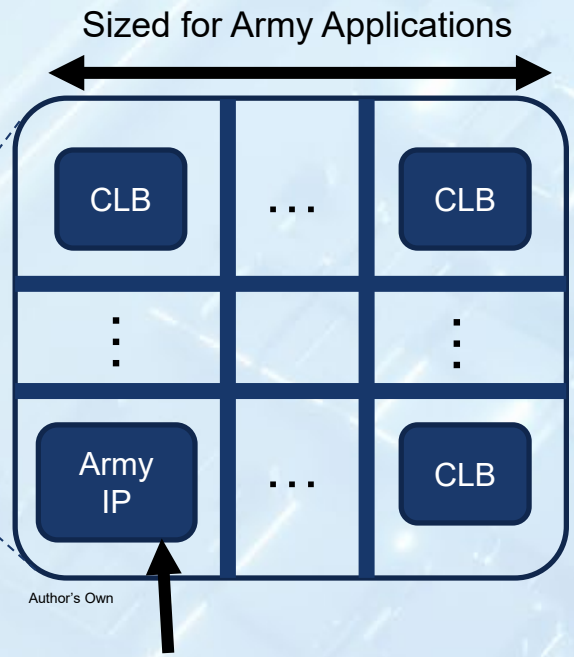
https://defensesystems.com/articles/2019/04/10/-/media/GIG/EDIT_SHARED/Military/militaryAI.png

https://www.army-technology.com/wp-content/uploads/sites/3/2020/08/AdobeStock_297617231_1_650x.jpeg

https://www.army-technology.com/wp-content/uploads/sites/3/2020/08/AdobeStock_210155062_650x.jpeg

Custom-built FPGA for Army Applications

https://www.autodesk.com/products/eagle/blog/wp-content/uploads/2017/05/microchip-on-card.jpg




Army Domain-Specific IP

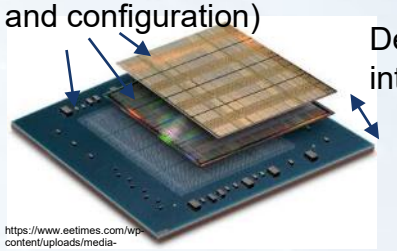
# OPENFPGA – ENABLES CUSTOM FPGA RESEARCH

## Potential Army FPGA Research Areas

### 3D FPGA

Partitioning across tiers (circuits and configuration)

Density of cross-tier interconnect



https://www.eetimes.com/wp-content/uploads/media-1159484-virtex-7-h580t-02a.jpg

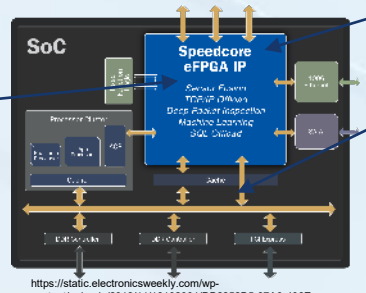
Size (capacity vs. SWaP-C)

### Embedded FPGAs

Amount of FPGA Fabric

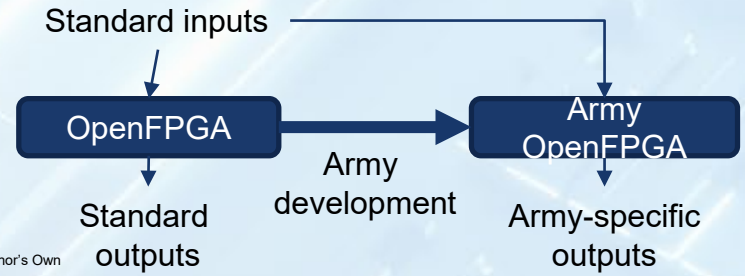
Inclusion of IP/accelerators

Interfaces to eFPGA




https://static.electronicsweekly.com/wp-content/uploads/2018/11/16102901/DB2252B5-67A0-408E-8F75-C68757813 6B1.png

- Proprietary, Army-designed add-ons to OpenFPGA for <u>overmatch</u> in design capability
  - Additional trust considerations (new hardware IP, proprietary bitstream generation, etc.)

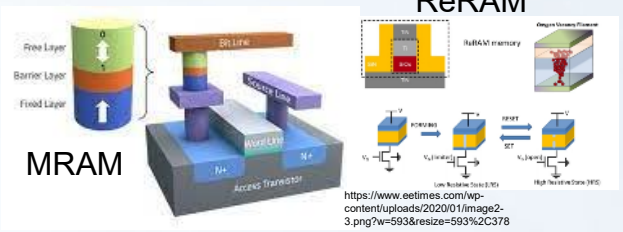



Author's Own

### New non-volatile configuration memory

ReRAM

MRAM



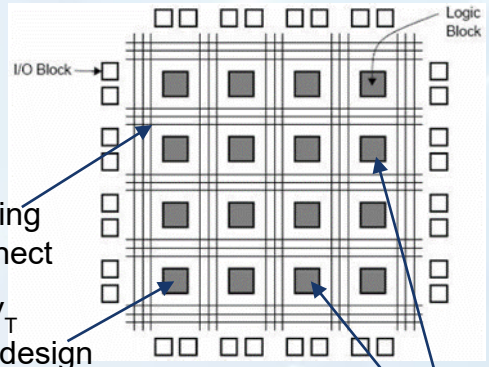
https://i0.wp.com/semiengineering.com/wp-content/uploads/2019/05/sttmram1.jpg?w=950&ssl=1

https://www.eetimes.com/wp-content/uploads/2020/01/image2-3.png?w=593&resize=593%2C378

### Sub-$V_T$ FPGA

Low-swing interconnect

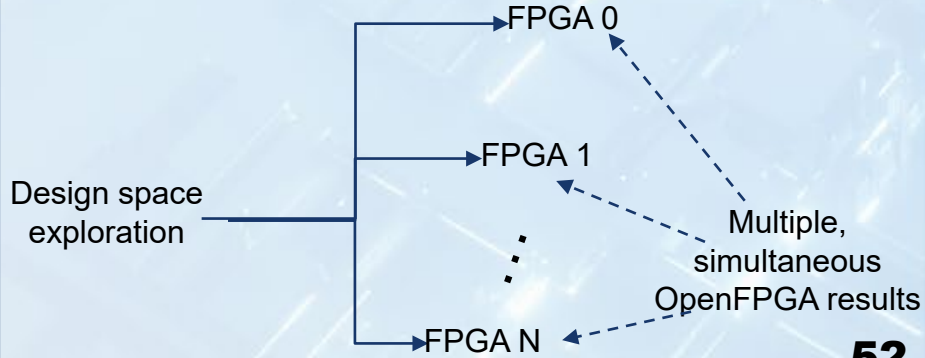
Sub-$V_T$ Sub-circuit design




https://www.tutorialspoint.com/vlsi_design/images/fpga_introduction.jpg

Variation Compensation

### "Unlimited" licenses – enablement for research in small teams

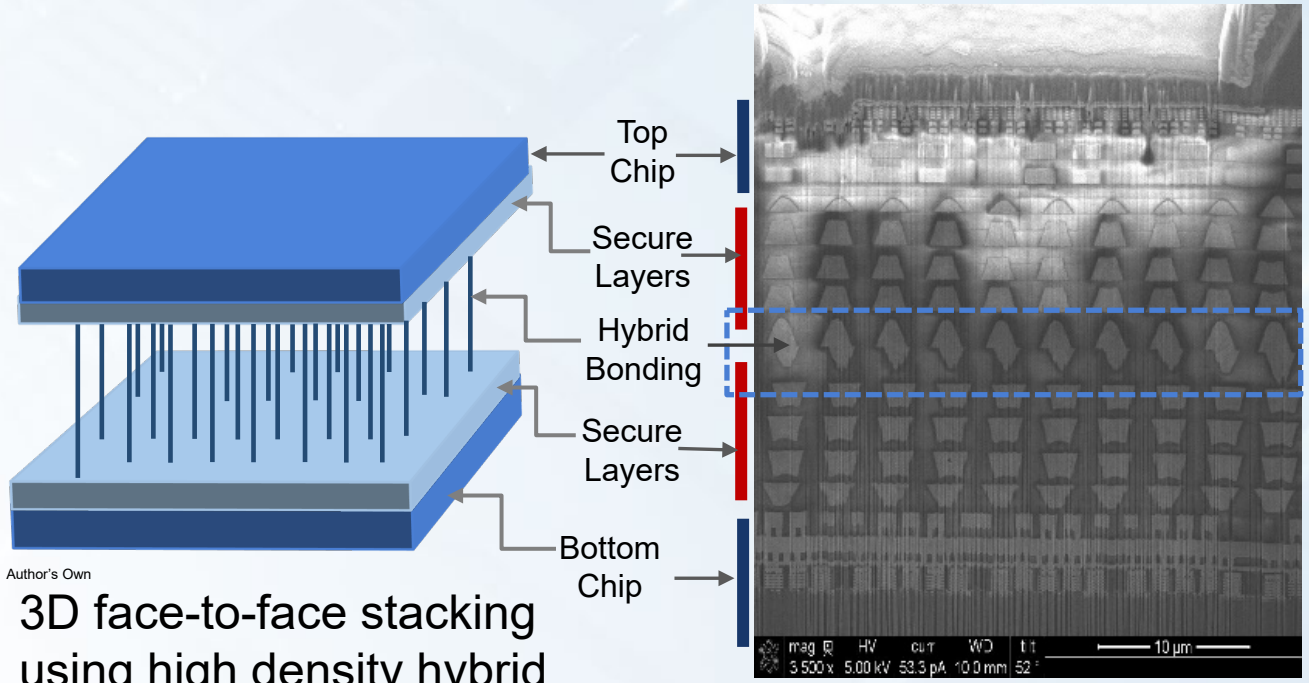


# ARL'S FOCUS AREA

## 3DICS AND TRUST

# OPENSOURCE TOOL FOR 3DIC DESIGN ENABLEMENT

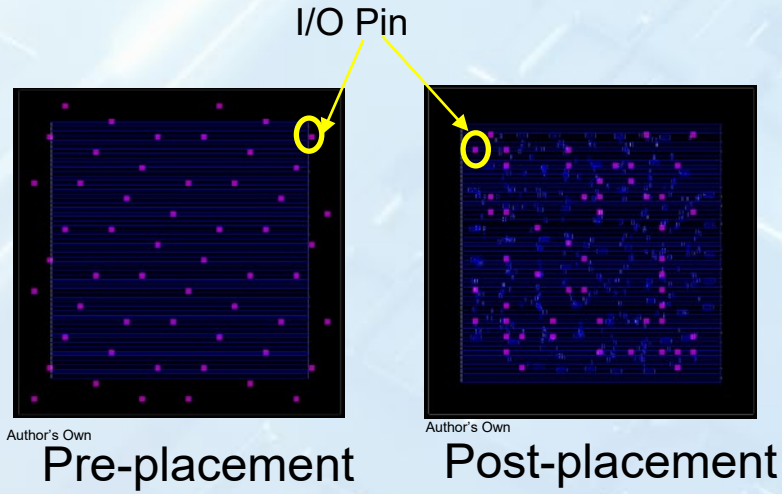
- Need a 3DIC tool to study design obfuscation techniques for trust related Army/DoD application
  - Split manufacturing using high density hybrid bonding technology to maximize obfuscation
  - Obfuscation achieved by hiding the connection points of the design splits in the secure layers




3D face-to-face stacking using high density hybrid bonding technology

SEM X-section for the 3D stack

- Leverage opensource tool for adding 3DIC design capability
- Collaborated with UCSD team to integrate 3DIC design flow in OpenROAD
  - Circuit partitioning
  - I/O pin placement for 3D integration



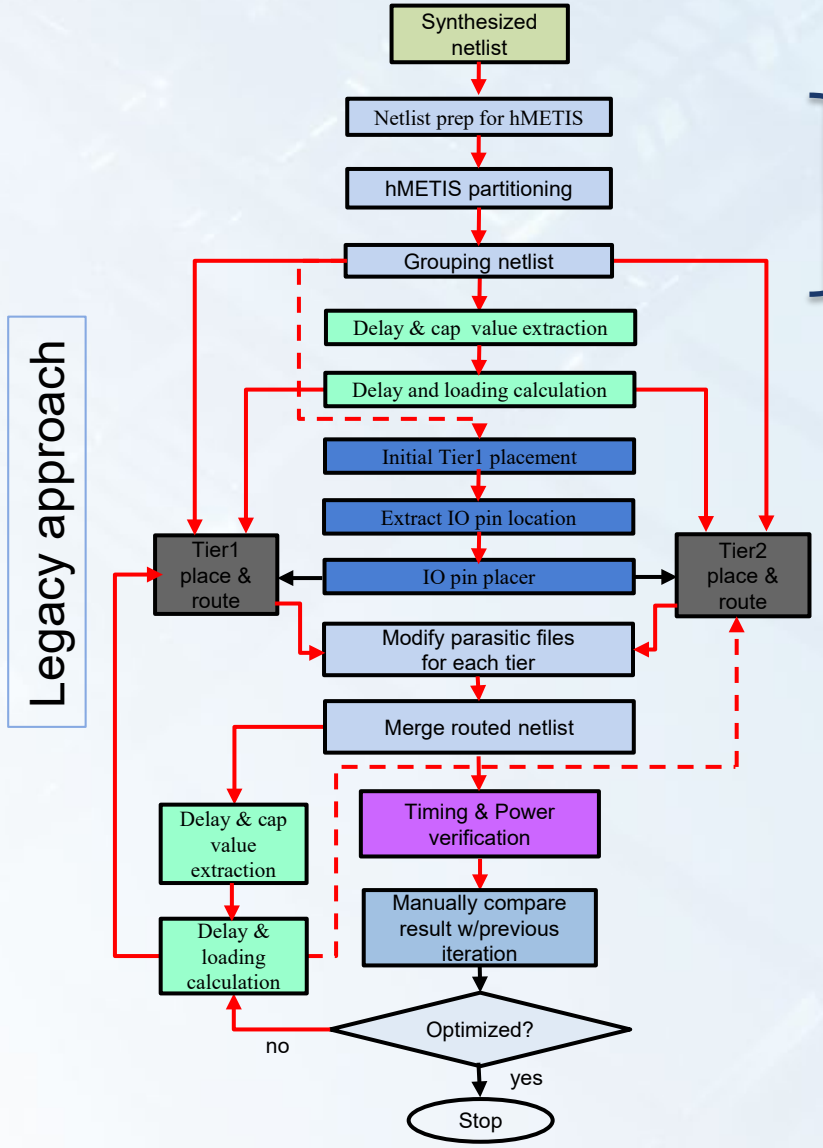

Pre-placement

Post-placement

Automatic 3D I/O pins in OpenROAD

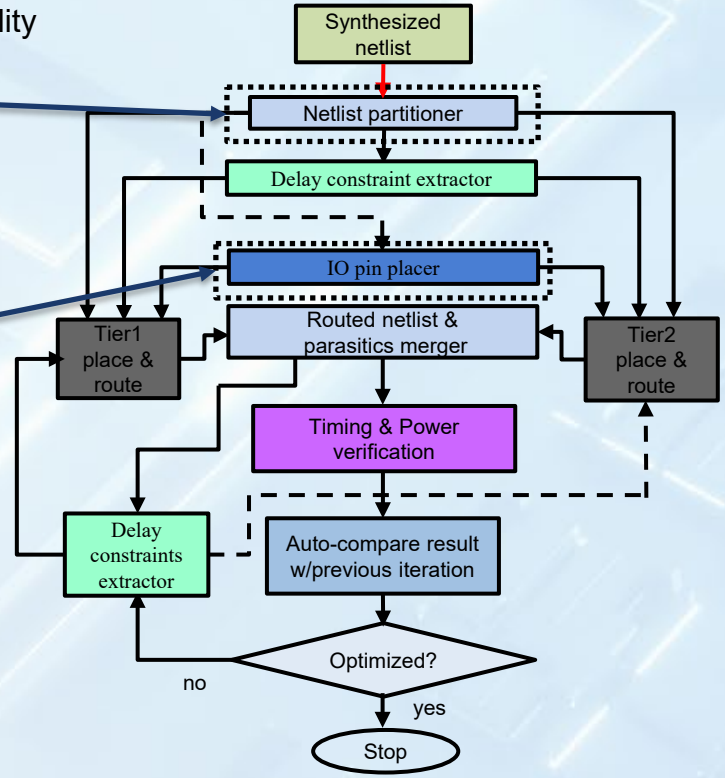
Franzon, Paul, GOMACTECH 21 Conference - Obfuscation, Presentation Slides titled Design Obfuscation through Smart Partitioning and 3D Integration - Experimental Results, NCSU, March 2021

# OPENROAD 3DIC DESIGN FLOW




Fewer tools and custom scripts → reducing errors and increases quality of results

Automated 3D pin placement → increases quality of placement and handling of large numbers of pins




Author's Own

Desired approach

Legend:

- Transition to a different tool
- Transition within same tool
- Included through collaboration with OpenROAD

Nigussie, Theodros, Design Obfuscation through Smart Partitioning and 3D Integration, PhD Dissertation at NCSU , Dec. 2020

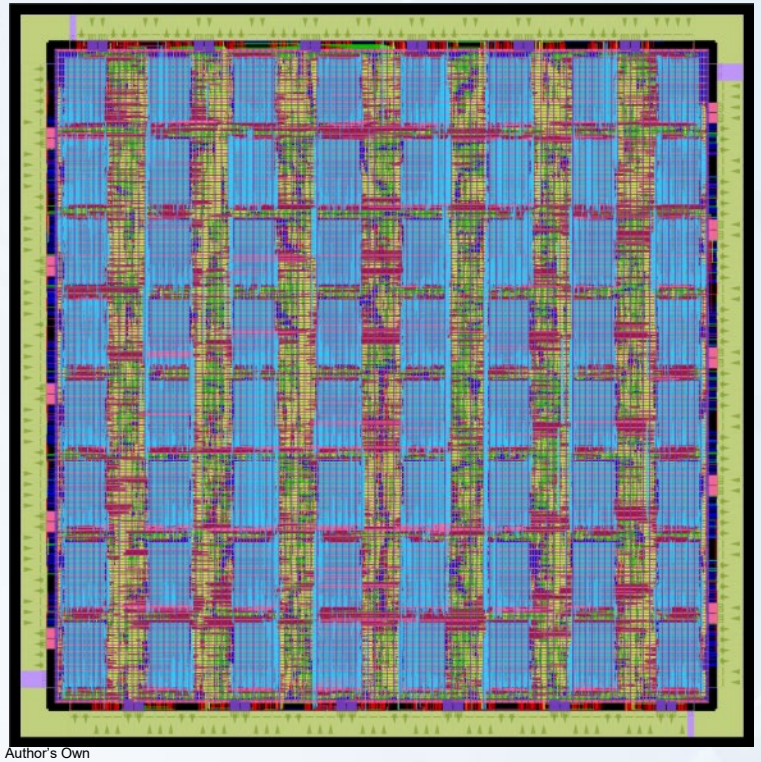
# STATUS OF 3DIC ENABLEMENT IN OPENROAD

| Activity | | Status | |
|---|---|---|---|
| | | Tool | Integration |
| Partitioning | Min-cut | ■ | |
| | Obfuscation | | |
| I/O pin placement | | ■ | ■ |
| Parasitics & routed netlist merger | | ■ | |
| Extracting delay constraints | | | |
| Power grid setup | | | |

Legend: ■ Complete ☐ Future need

# RECONFIGURABLE AI PLATFORM ON OPENROAD

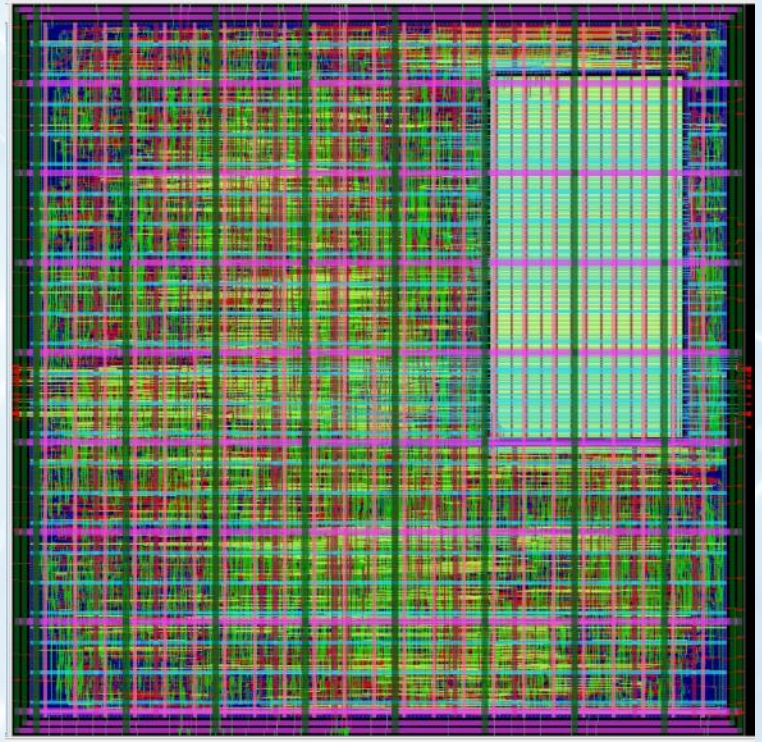
## GF55



Author's Own

800k instances, ~8.5 hours run time

## GF12



Author's Own

~30k instances, ~30 minutes run time

# GOING FORWARD

# GOING FORWARD

- Grow the user base of Opensource EDA tools
  - Demonstrate benefits for research
  - Silicon validation where possible
  - Improved quality of documentation and user interfaces

- Expand Army and DoD involvement
  - Participate in increasing the quality of the tools
  - Focus on building Government only add-ons

- Gaps I still see in the EDA tools (i.e. wish list):
  - Digital simulation
  - Synthesis
  - Signoff

ERI ELECTRONICS RESURGENCE INITIATIVE

SUMMIT

& MTO Symposium

DARPA