ERI ELECTRONICS RESURGENCE INITIATIVE SUMMIT & MTO Symposium

WORKSHOP:
The Future of Open-Source Chip Design Tools
Advancements in Open-Source Electronic Design Automation

PROGRAM MANAGER: Serge Leef	
DATE: Wednesday, October 20, 2021	**TIME:** 3:15pm – 5:30pm
ROOM NAME: Julian Warchall	

DESCRIPTION

This workshop will review ongoing research and transition opportunities under the Intelligent Design of Electronic Assets (IDEA) and Posh Open Source Hardware (POSH) programs, including presentations on open-source transition, the role of commercial consortiums, ASIC engineering in a no-human-in-the-loop software environment, and government user perspectives on design automation. Following the presentations, a moderated panel discussion will encourage audience Q&A.

AGENDA

3:15pm-3:30pm	***Kickoff Presentation - The Future of Open-Source Chip Design Tools*** Serge Leef, DARPA
3:30pm-3:45pm	***Academic Presentation - OpenFPGA: From POSH/IDEA to the Open-Source FPGA Foundation*** Professor Pierre-Emmanuel Gaillardon, University of Utah
3:45pm-4:00pm	***Academic Presentation - An Open-Source ASIC Flow for Asynchronous Logic*** Professor Rajit Manohar, Yale University
4:00pm-4:15pm	***Industry Presentation - Making Pre-Silicon Complex AMS System Validation Feasible*** Dale Donchin, Synopsys
Afternoon Break: 4:15pm-4:30pm	
4:30pm-4:45pm	***Government Presentation - Open-Source EDA at Army Research Laboratory*** Peter Gadfort, Army Research Laboratory
4:45pm-5:30pm	***Panel Discussion - The Future of Open-Source Chip Design Tools*** All presenters with audience participation
Workshops Conclude at 5:30pm	

QUESTIONS

Please contact Julian Warchall for more information following this workshop at julian.warchall.ctr@darpa.mil.