ELECTRONICS
RESURGENCE INITIATIVE

ERI SUMMIT

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MTO
MICROSYSTEMS TECHNOLOGY OFFICE

DARPA

ELECTRONICS RESURGENCE INITIATIVE
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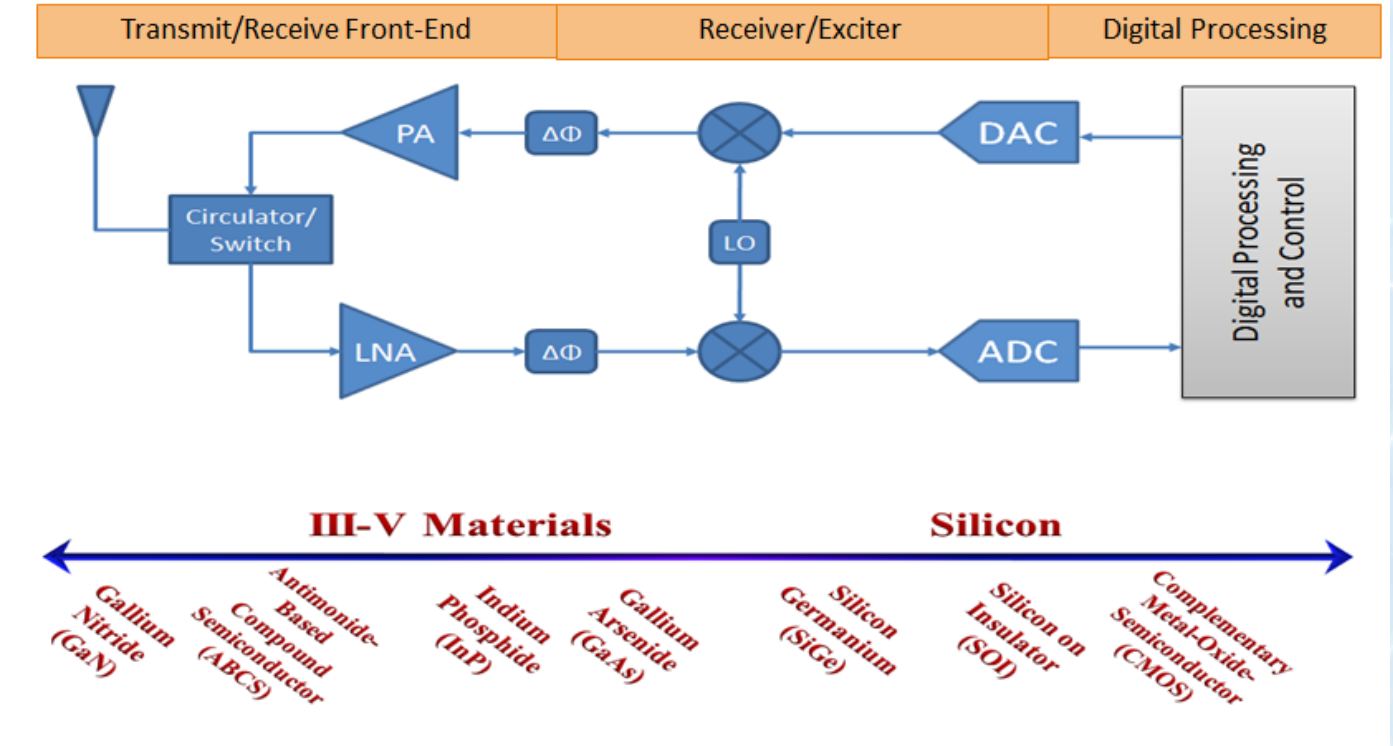
MIXED-MODE GOVERNMENT APPLICATIONS AND NEEDS

TONY QUACH
CHRIS BOZADA

AIR FORCE RESEARCH LABORATORY
SENSORS DIRECTORATE

HIGHLY INTEGRATED MICROSYSTEMS

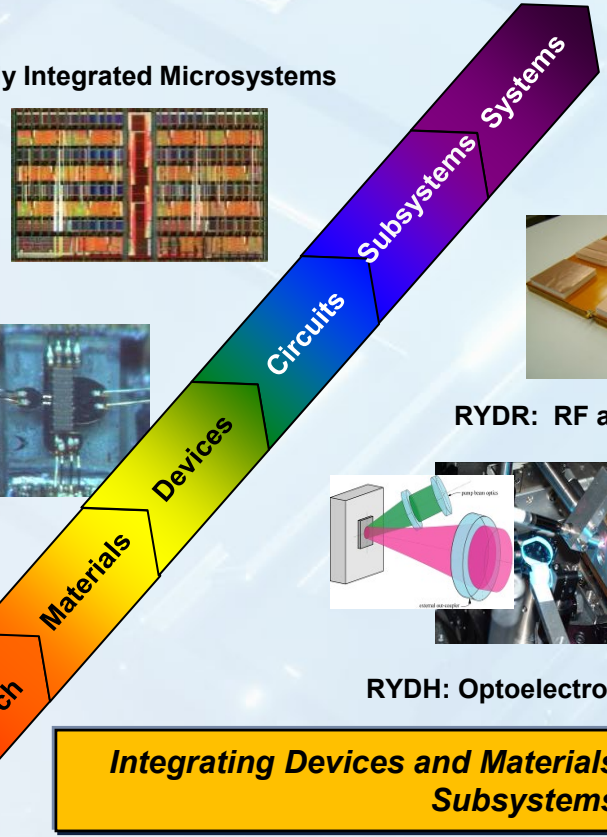
Mission: To discover, mature, and demonstrate emerging semiconductor and integration technologies that dramatically reduce the cost, size, weight, and power consumption of EO & RF sensor components to enable Air, Space, & Cyber Dominance!



AEROSPACE SUBSYSTEMS & COMPONENTS DIVISION (AFRL/RYD)

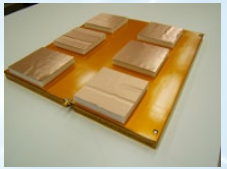
Derived Enabling Sensor Devices and Component Needs

- Low Cost, Size, Weight, Power
- Wideband / Multifunction
- High Power/Efficiency
- High Spectral Purity
- Low Latency
- Agile and Reconfigurable
- Integrated
- Digitization/Processing in Sensor
- Reliable
- Trusted

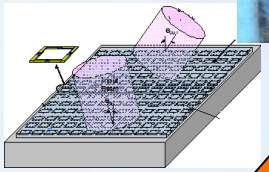


RYDI: Highly Integrated Microsystems

RYDT: Trusted Electronics



RYDR: RF and EO Subsystems



RYDD: Devices for Sensing

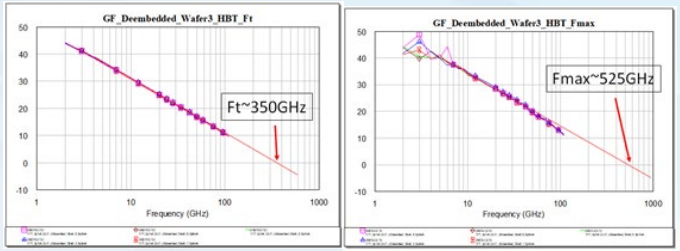
RYDH: Optoelectronics Technology

Integrating Devices and Materials to Make Circuits and Subsystems

DARPA T-MUSIC BENEFITS TO AF APPLICATIONS

Global Persistent Awareness

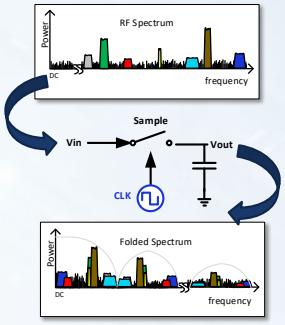
Ultra-high frequency transistor delivers Gain beyond W-band of operation



Phase 1 Measured Data

DARPA T-MUSIC BENEFITS TO AF APPLICATIONS

Nyquist Folding Receiver



- All-Domain Staring Capability for High Probability-of-Intercept
- >15 GHz of instantaneous BW (2-18 GHz)
- Directional Finding: Near real-time line of bearing (LOB) estimation at <1° accuracy

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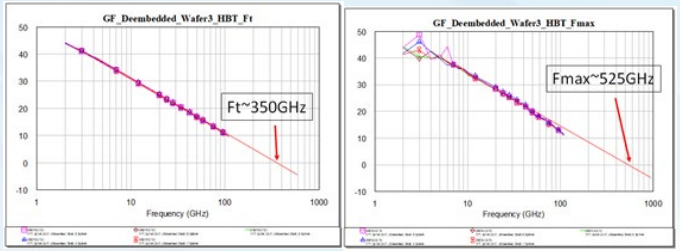

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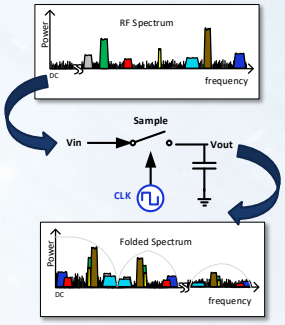

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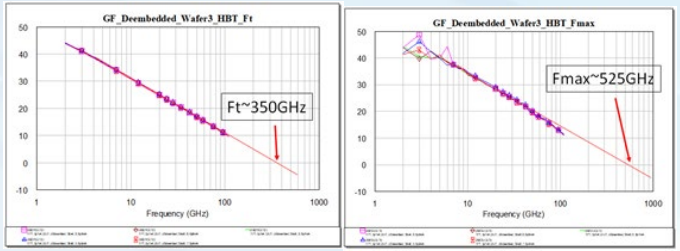
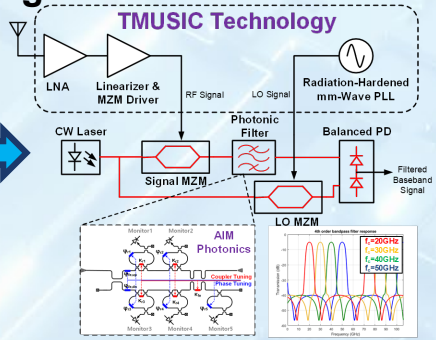


Phase 1 Measured Data

Integrated Photonic Receiver



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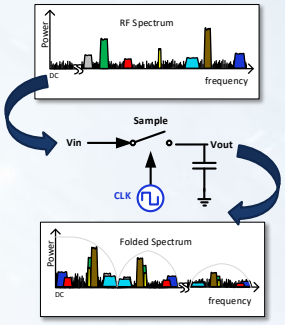

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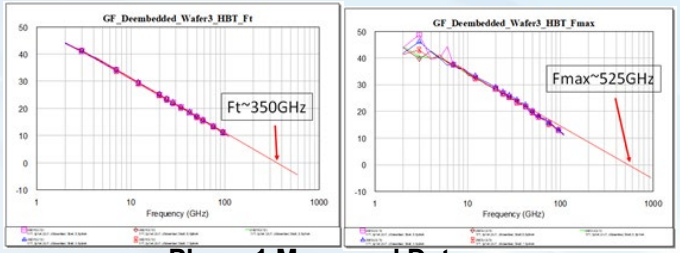

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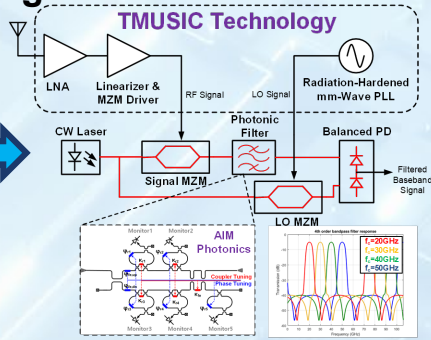
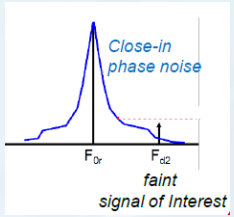


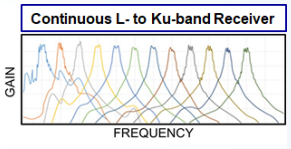
REMAR

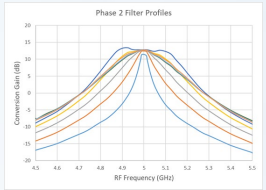
- Multi-band, multifunction frequency coverage & waveform diversity
- Ability to sense and respond to any signal/threat and eliminate "blind spots" in our control of the EMS

Rapid Effective Decision-Making

Low Noise Clock Source







- Fast transistors enable high frequency clocks
- Low close-in and broadband noises ensure capturing faint signal

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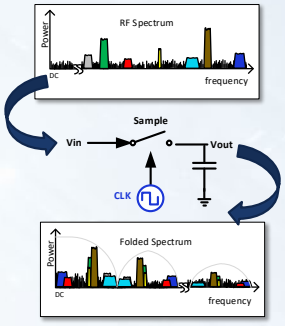
Nyquist Folding Receiver



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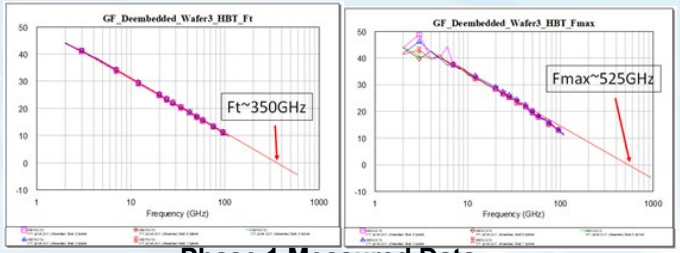

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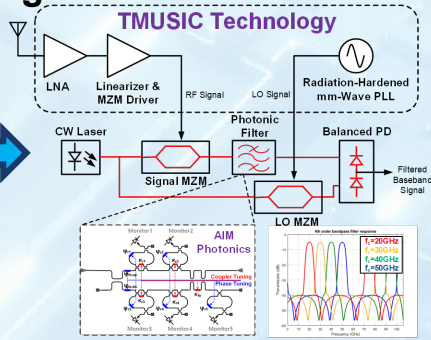

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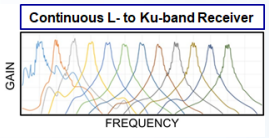

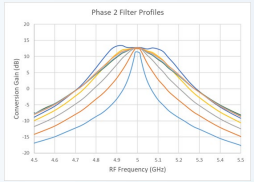

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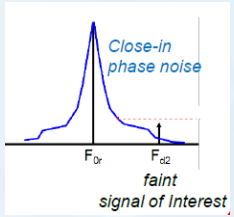

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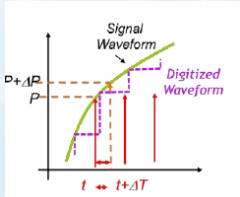
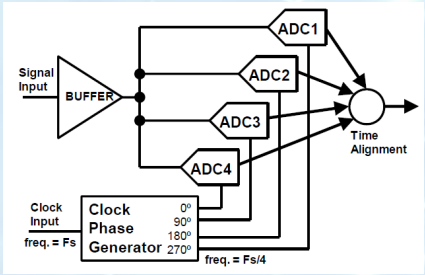
High Resolution Converters



- High speed transistors needed to capture fast signals
- Low transistor noise enables precision sampling resolution

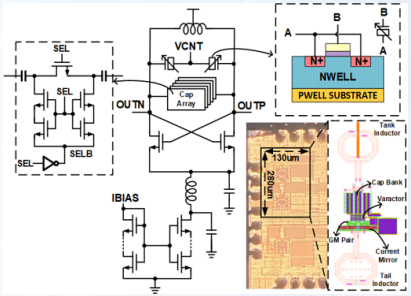
Direct Sampling Tech

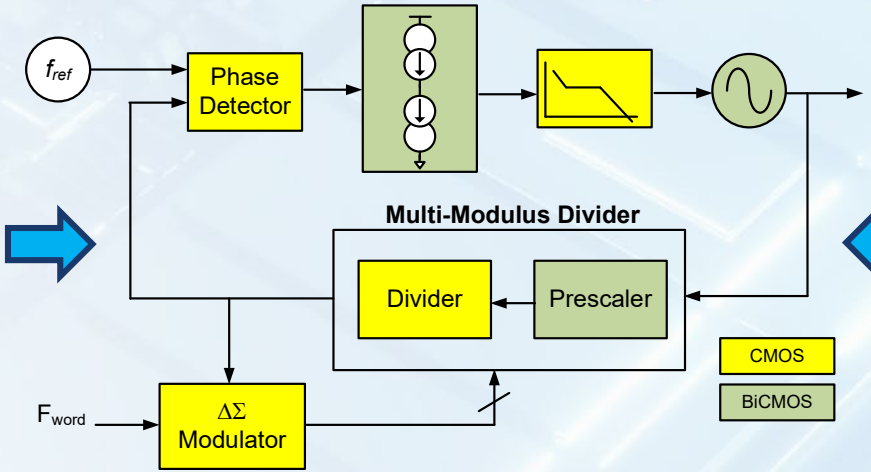


Element Level Digital Beam Former

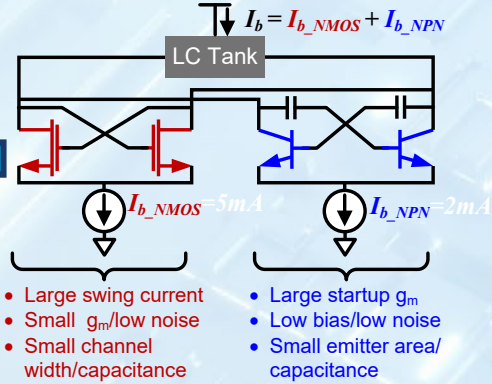
T-MUSIC TECHNOLOGY ENABLEMENT: RADIATION HARDEN, WIDE TUNING RANGE, MMW PLL

Rad-Hard Design Techniques (TAMU)





Ultra-Wide Tuning Design Techniques (OSU)



- Fast-switching CMOS and low 1/f noise BJT offer superior close-in noise performance in reference path
- BiCMOS VCO architecture exploits BJT's high g_m and low 1/f noise and CMOS's low thermal noise for wide TR and low phase noise at mm-Wave
- RHBD methodology employed for critical VCO components to provide rad tolerance while still meeting stringent performance specs

ACKNOWLEDGEMENT

- DARPA T-MUSIC: Dr. James Wilson & Dr. Y.K. Chen
- Team Members: William Gouty, Steve Hary, Aji Mattamana, Dr. Samantha McDonnell, Lauren Pelan, & Dr. Paul Watson
- Collaborators:
  - Dr. Waleed Khalil (Ohio State University)
  - Dr. Samuel Palermo (Texas A&M University)

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HYBRID MIXED-MODE ELECTRONIC CIRCUITS

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

T-MUSIC UCLA TEAM

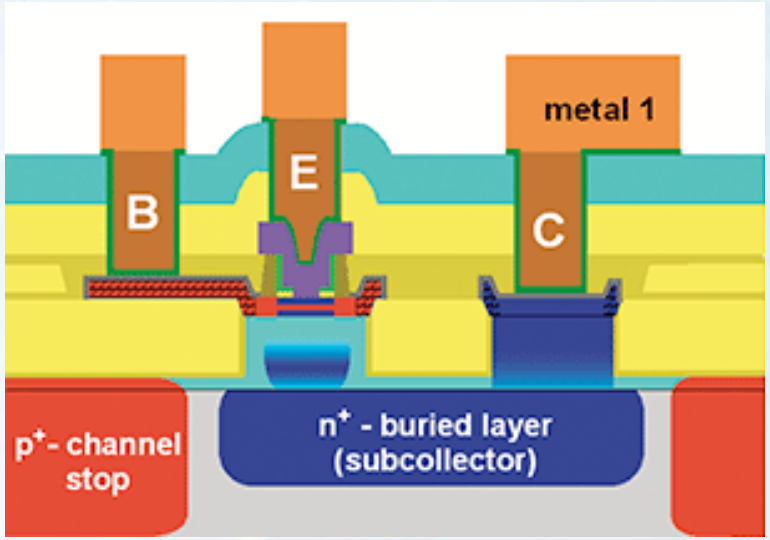
C.K. Ken Yang

M.C. Frank Chang

Sudhakar Pamarti

- *Graduate and Post-Doctoral Students:*
  - *Chris Chen*
  - *Allen Chien*
  - *Avantika Singh*
  - *Jiazhang Song*

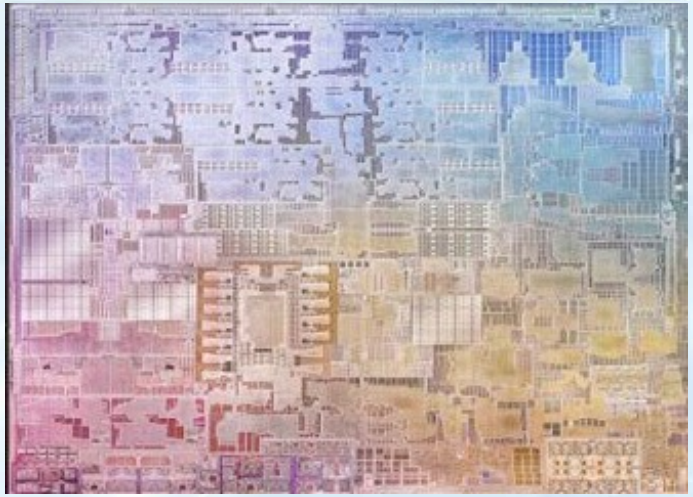
T-MUSIC GOALS



- Benefits of SiGe HBT
  - f_T (f_{MAX})
  - 1/f corner
  -
  - g_m/I_c
  - Dynamic range

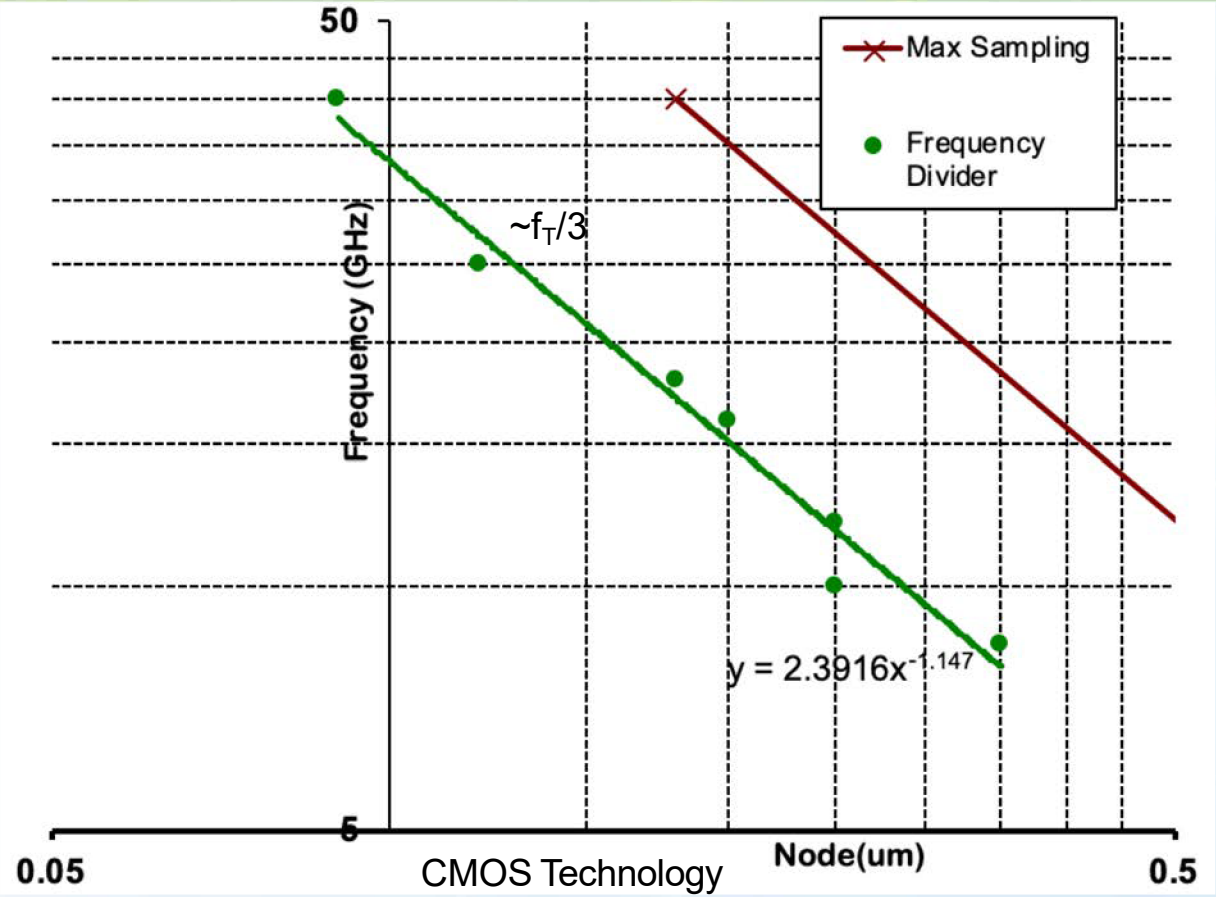
- Program Goals
  - Demonstration vehicles for ultra-high performance through hybrid design

	Divider	***PLL***	***ADC***
Phase 1	100GHz	-106dBc @1MHz	16b, 1GS/s, 500MHz
Phase 2	200 GHz	-120dBc	8b, 100GS/s, 50GHz



- Benefits of CMOS
  - Integration
  - Fast switching
  - Power

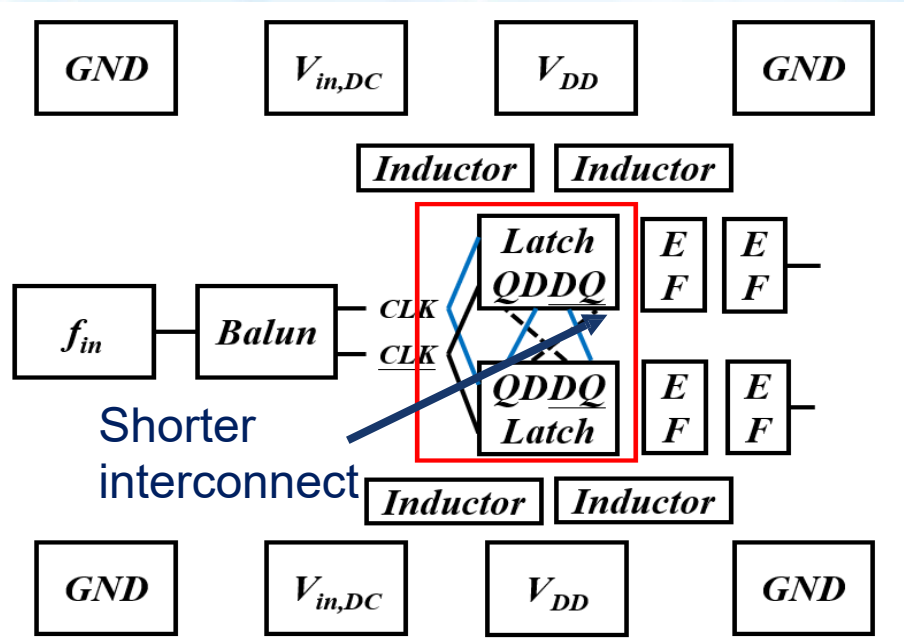
FREQUENCY DIVIDER – LEVERAGE F_T

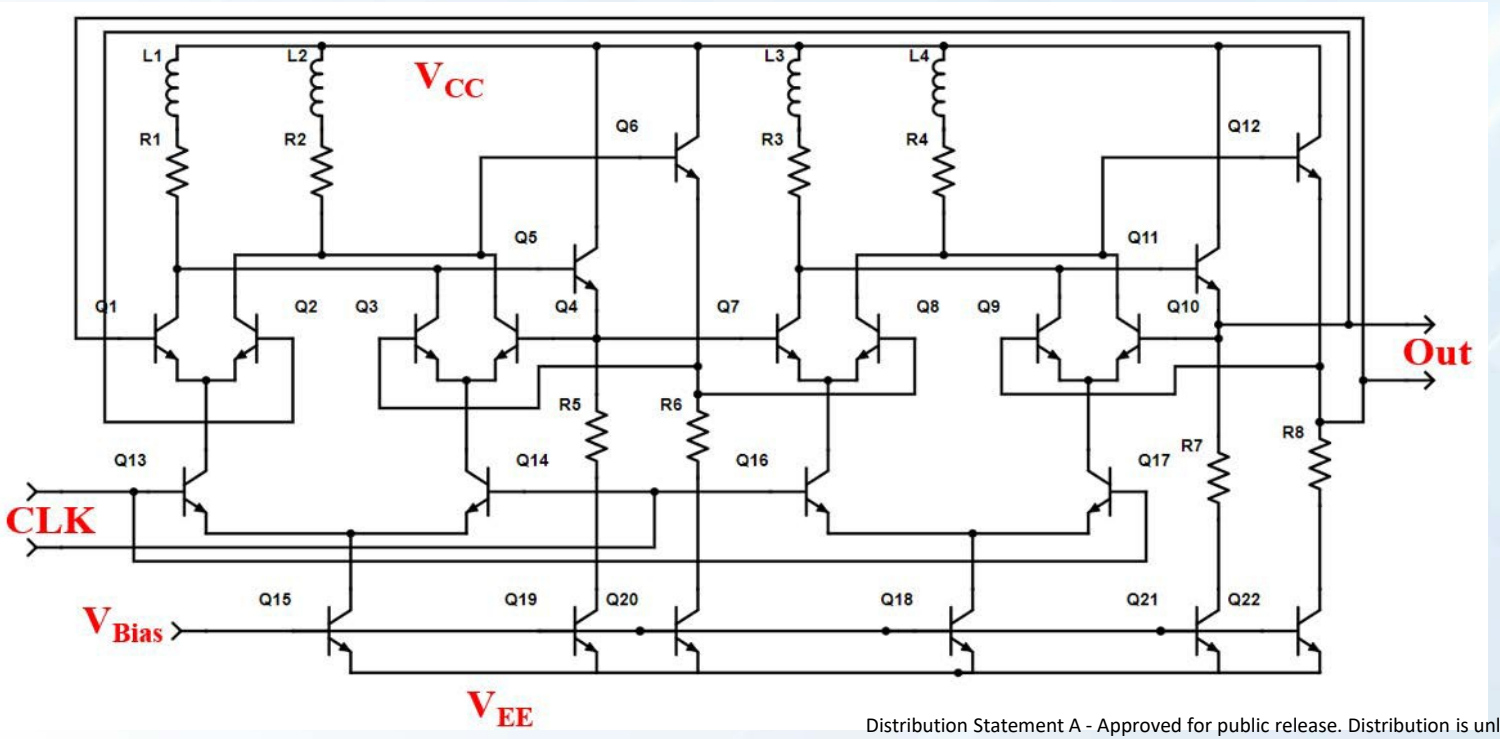


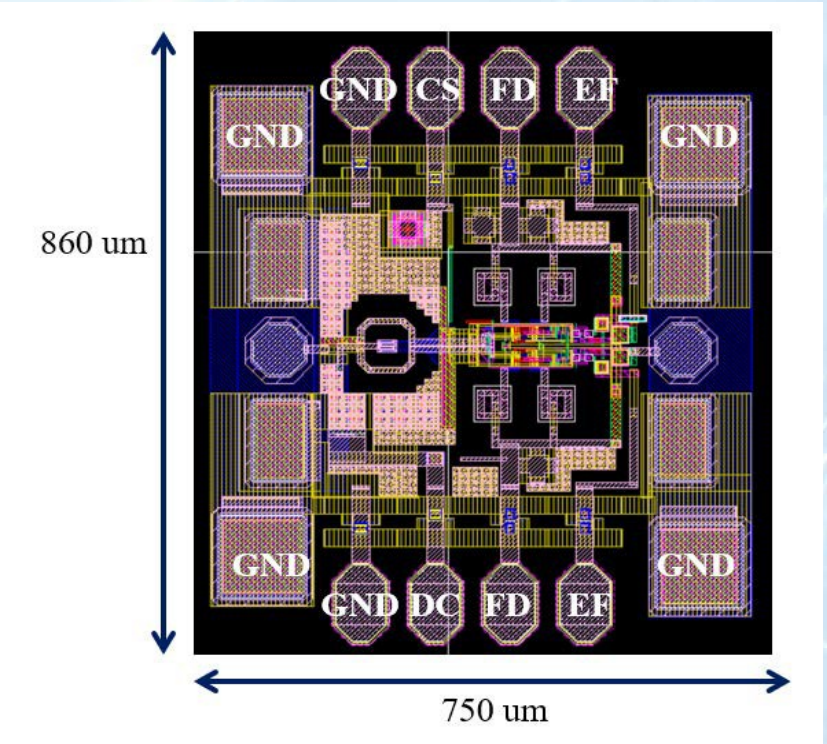
- Maximum static divider frequency as a fraction of f_T (f_{MAX}) is ~f_T/3.
  - Similar between HBT and CMOS
  - Example: 200GHz on InP HBT (600GHz f_T) [D'Amore]
  - CMOS becomes very power hungry

STATIC DIVIDER DESIGN

- Design targets
  - Broad frequency range
  - Low input power, <-10dBm
  - Low total power, 66mW for main divider
- Inductive peaking with EF buffering
- Symmetric placement
  - Reduced wiring capacitors and more balanced delay.

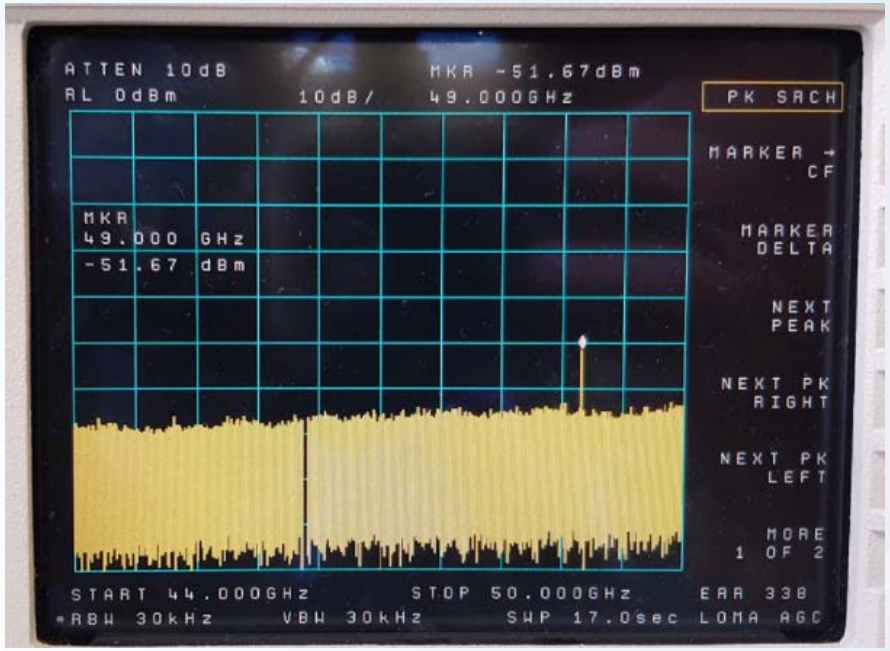


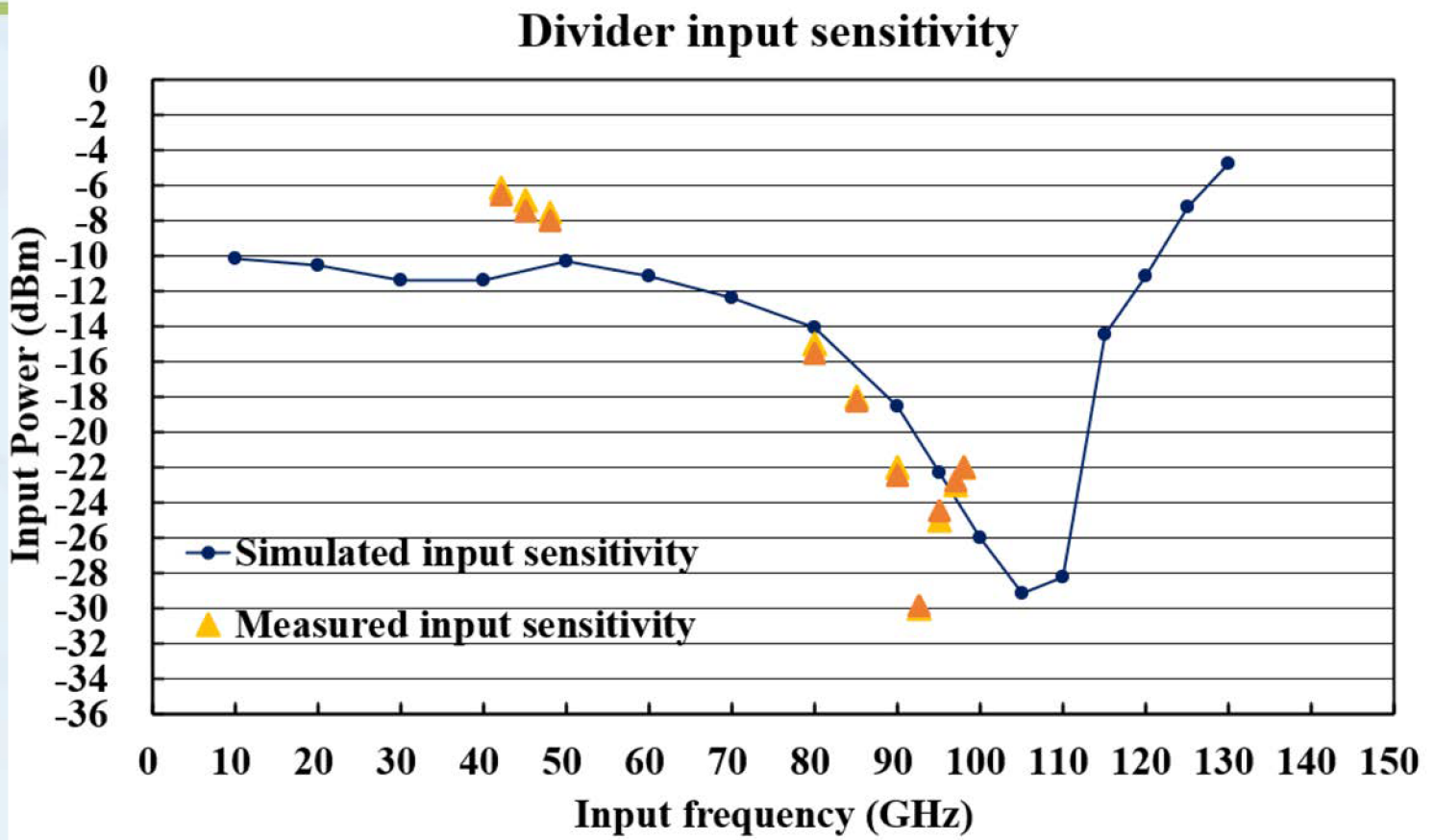


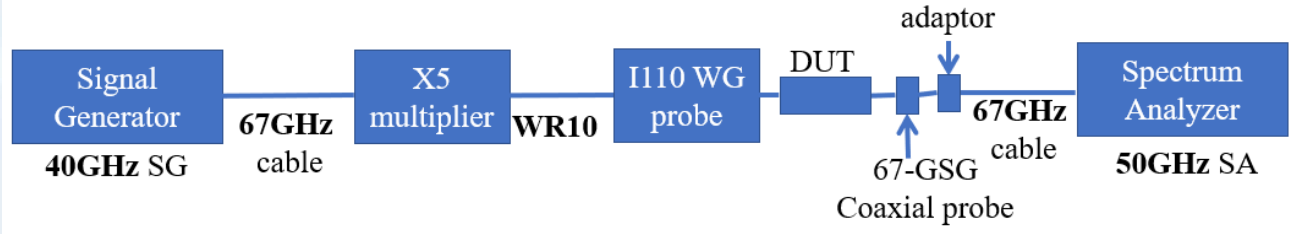


MEASUREMENT RESULTS

- Sweeping input sensitivity
- The self resonant frequency is designed around 105-110 GHz, Measured at 100GHz
- The DC current is designed around 23 mA per stage – measured ~35mA
- Multiple test chips & repeatable yield.







DIVIDER PERFORMANCE COMPARISON

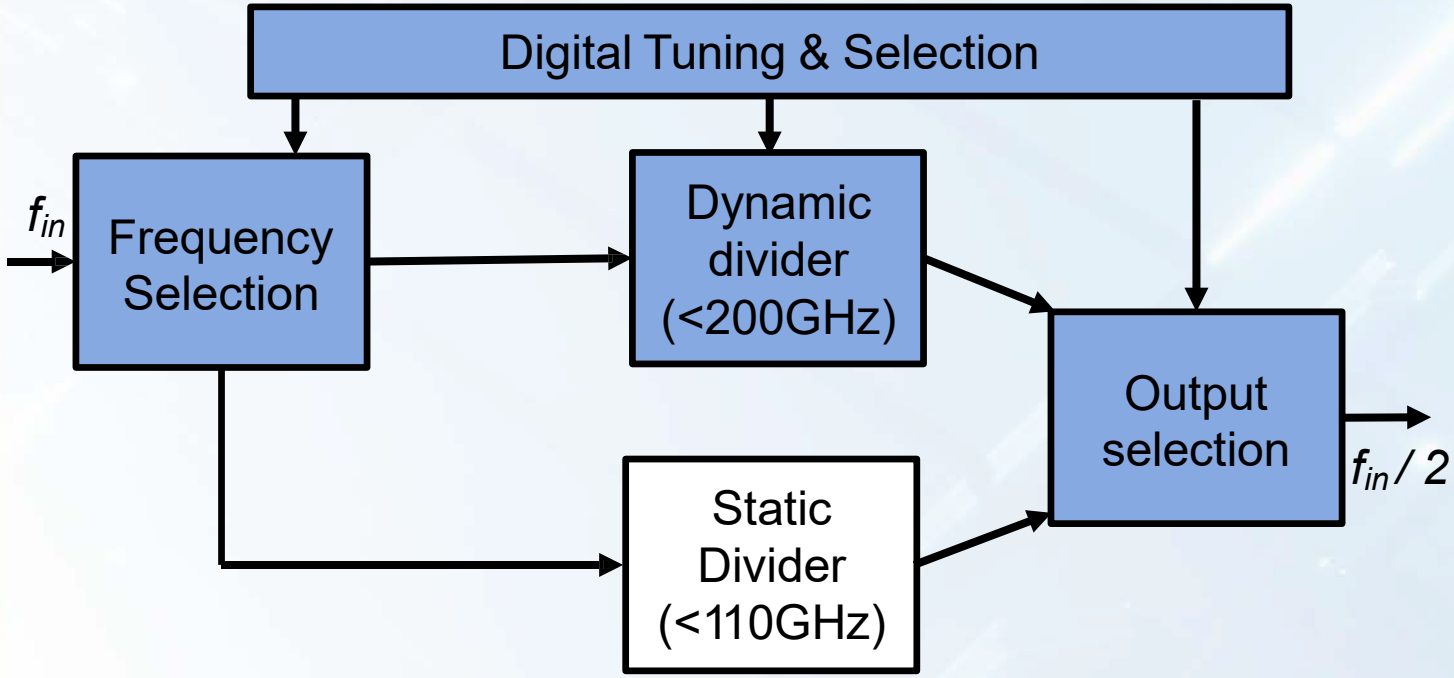
Technology (Lg, f_t/f_{max})	Self-oscillating frequency (GHz)	Max operating frequency (GHz)	Minimum input power (dBm)	DC power (mW)	FoM (GHz/mW) FoM = SRF/DC
130nm, 240/330	70.34	>80	-49	141	0.5
130nm, 250/330	64	92.5	-42	56	1.14
180nm, 200/-	80	113	-30	115	0.69
130nm, 300/500	111.6	128.7	-20	196	0.57
130nm, 200/250	75	90	-38	61.6	1.22
160nm, 280/300+	**92.5/89**	**100/95**	**-39**	**75.6/69.3**	**1.22/1.28**

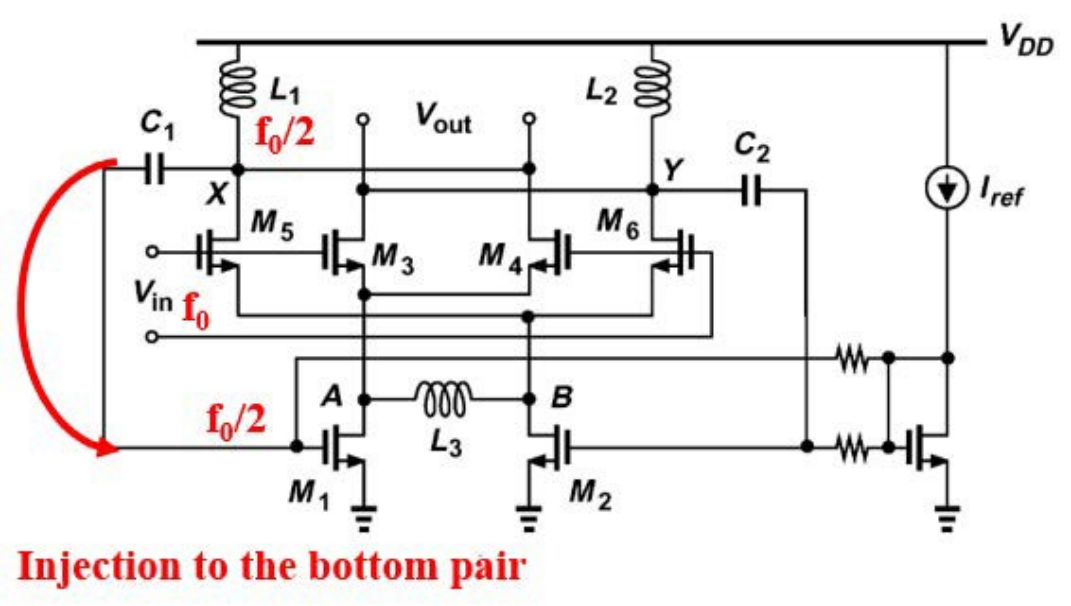
A. Awny, et al., "Design and Measurement Techniques for an 80 Gb/s 1-Tap Decision Feedback Equalizer," *IEEE JSSC*, vol. 49, no. 2, pp. 452-470, Feb. 2014.
V. Issakov, et al., "Low-voltage flip-flop-based frequency divider up to 92-GHz in 130-nm SiGe BiCMOS technology," *2017 INMMiC Workshop*, Graz, 2017, pp. 1-3.
S. Trotta, et al., "A tunable flipflop-based frequency divider up to 113 GHz and a fully differential 77GHz push-push VCO in SiGe BiCMOS technology," *2009 IEEE RFIC Symposium*, Boston, MA, 2009, pp. 47-50.
U. Ali, et al., "High speed static frequency divider design with 111.6 GHz self-oscillation frequency (SOF) in 0.13 µm SiGe BiCMOS technology," *2015 German Microwave Conference*, Nuremberg, 2015, pp. 241-243.
P. Zhou, et al., "A low power, high sensitivity SiGe HBT static frequency divider up to 90 GHz for millimeter-wave application," in *China Communications*, vol. 16, no. 2, pp. 85-94, Feb. 2019.

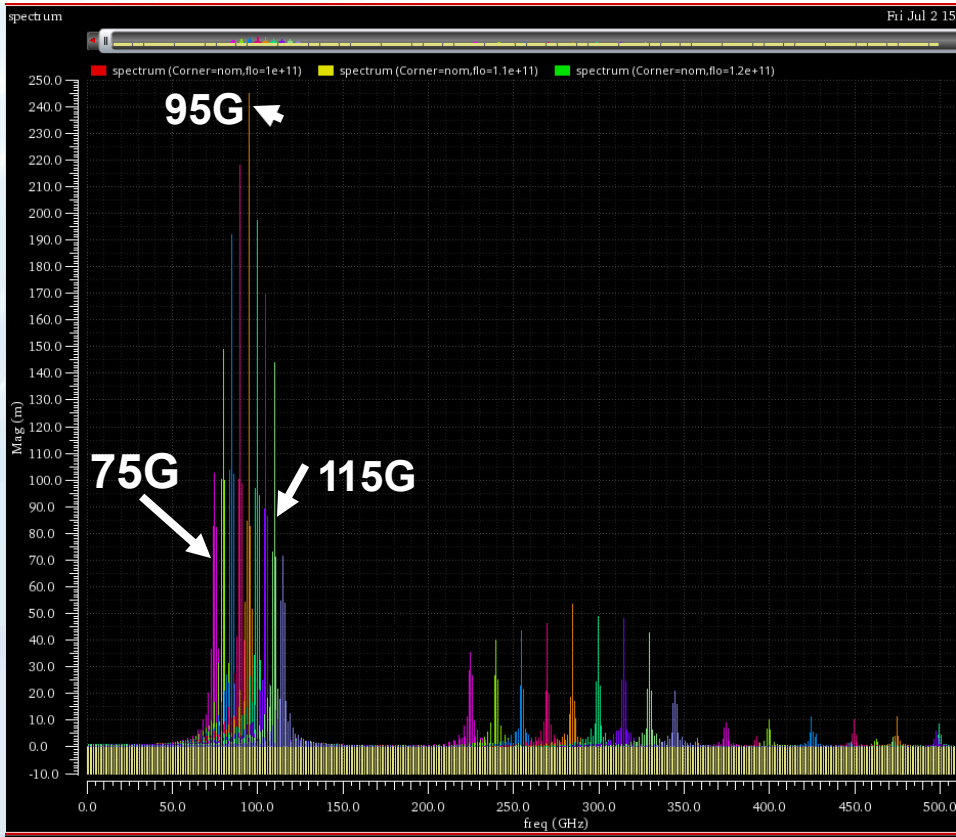
Up to 120GHz is achievable in this technology!

EXTENDING BEYOND $F_T/3$

- Tuned divider performance can exceed $f_{MAX}/2$.
  - Challenge #1 – design a wide-range tuned-divider.
- Combining the two designs to improve range.
  - Challenge #2 - selection and detection of frequency setting

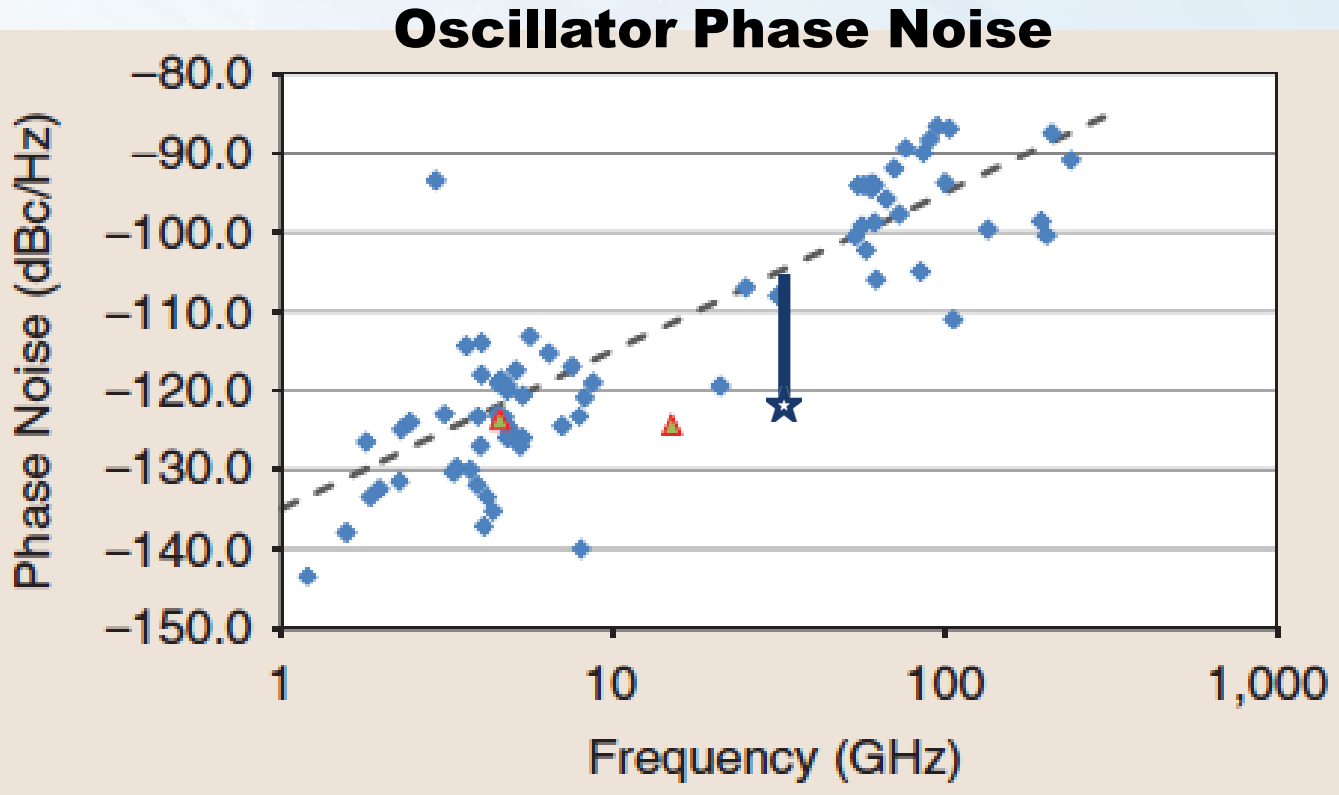


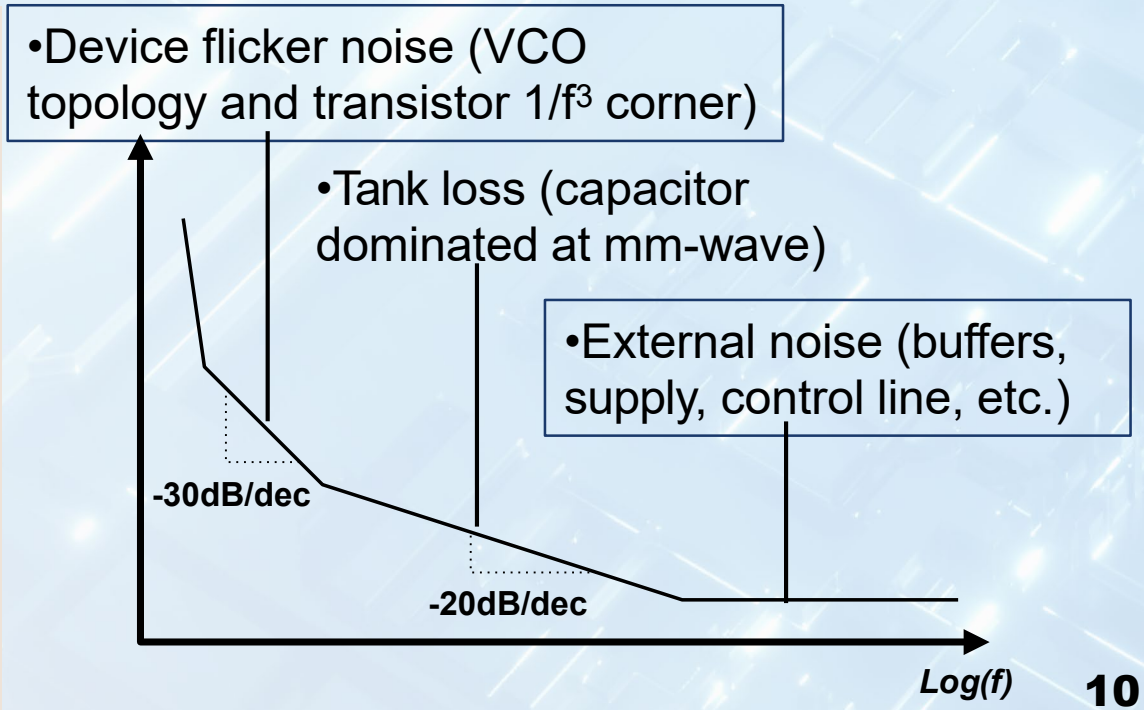




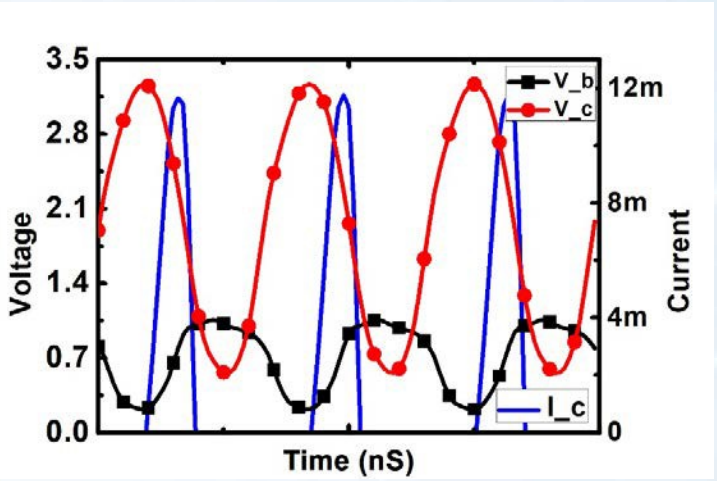
MM-WAVE PLL – LEVERAGE 1/F, BUFFERING, AND CMOS SAMPLING

- PLL noise is largely from reference input and VCO.
  - 100MHz crystal has sufficiently low phase noise – 1MHz phase noise of -175dBc/Hz
  - State of the art VCO equivalent noise at 30GHz is >-110dBc/Hz

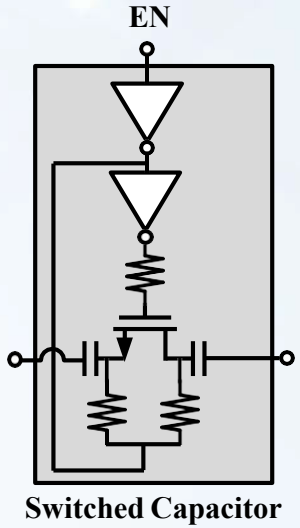




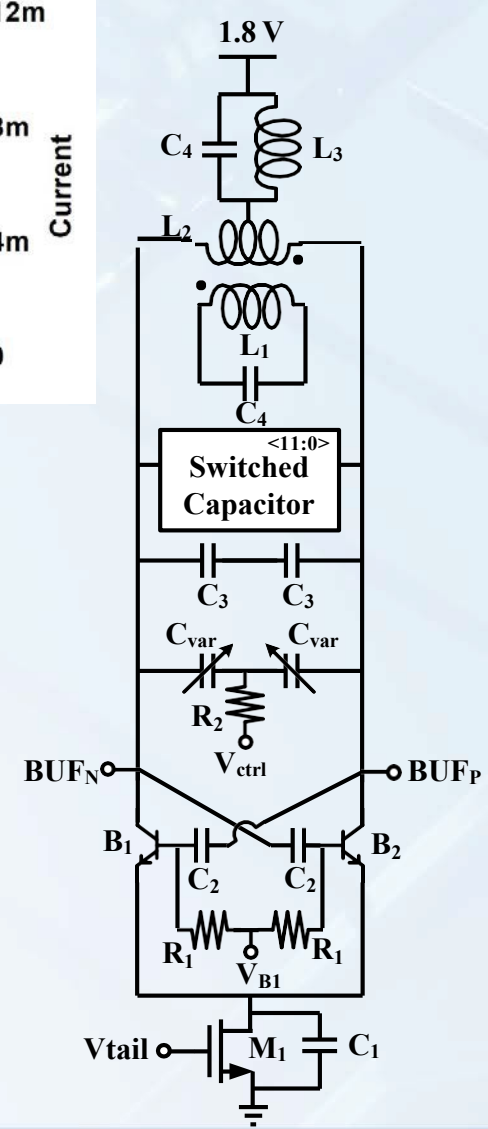
CLASS-C MULTI-HARMONIC RESONANCE VCO



Waveforms of B_1 device



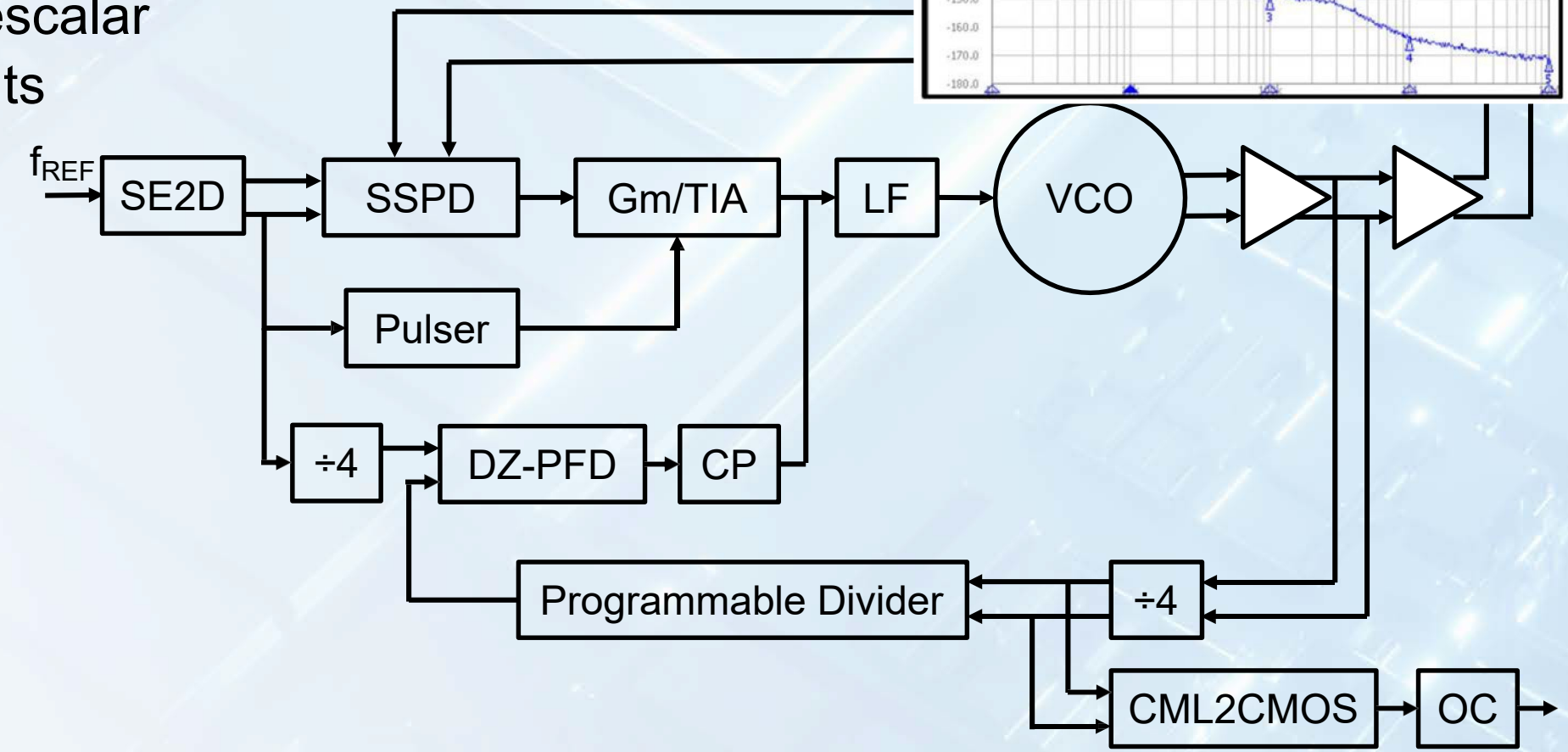
Switched Capacitor



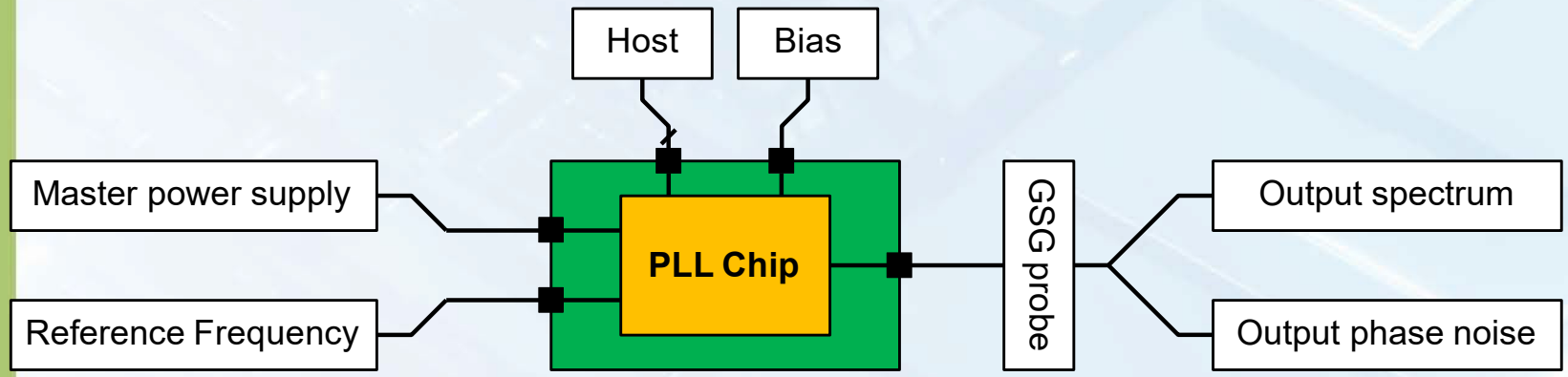
- SiGe
  - High dynamic range
  - Leverage high-f_T device to achieve sufficient loop gain with minimum parasitic
  - 1/f corner
  - Drive capability for buffering
- CMOS
  - Switched-C tuning
- Class-C operation
  - Shrinks flicker noise region of operation by reducing zero-crossing time of the waveforms
  - Saves DC power consumption
  - Maintains high-Q tank by avoiding operating BJT in sat. region
- Multi-harmonic resonance
  - Reduces up-converted flicker noise
    - 2nd harmonic side-transformer
  - 3rd harmonic waveform shaping improves jitter and lowers P_{DC}

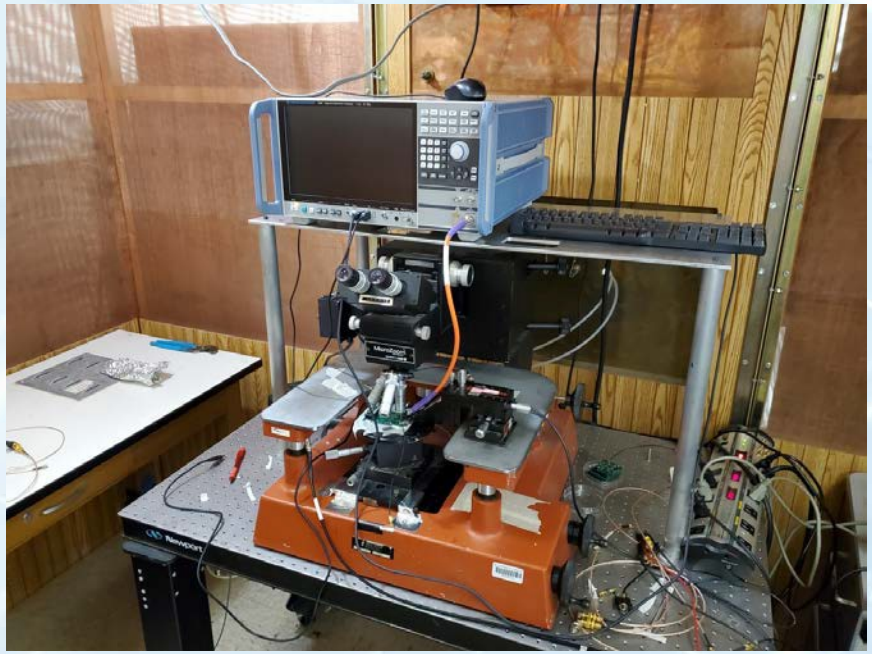
PLL ARCHITECTURE

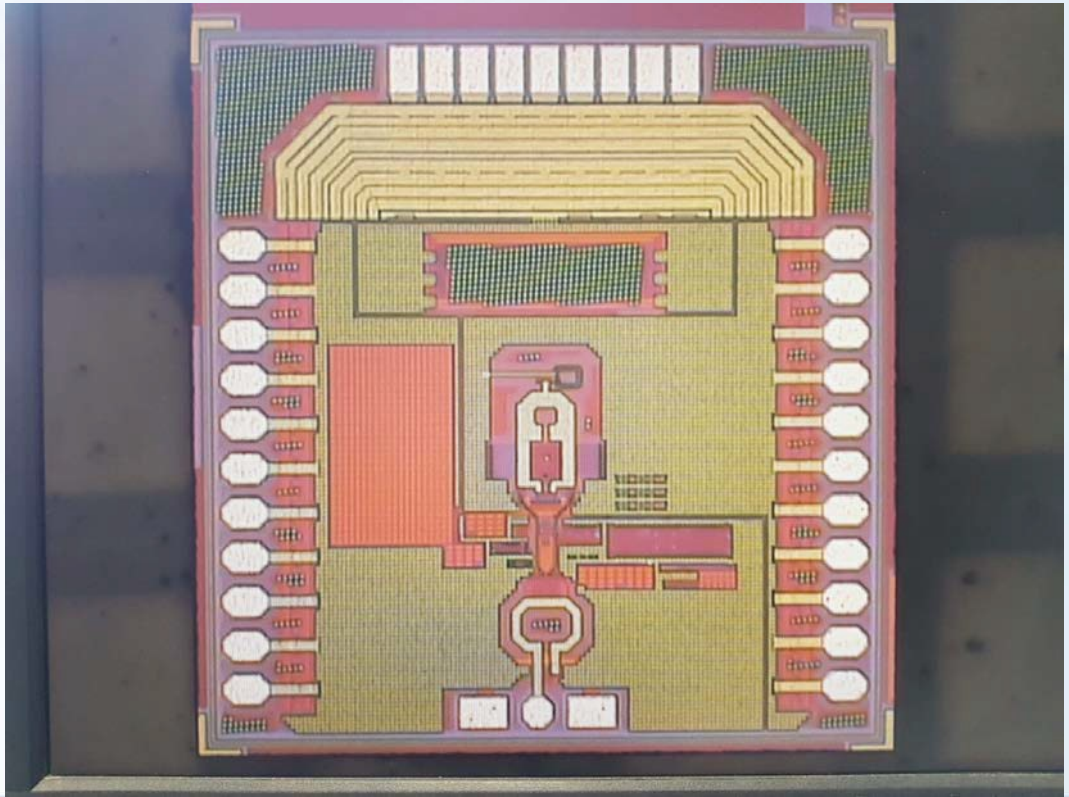
- Direct sub-sampling + PFD-based FLL
- CMOS benefits
  - Sub-sampling
  - Low-power prescalar
  - FLL components



TEST CHIP IMPLEMENTATION



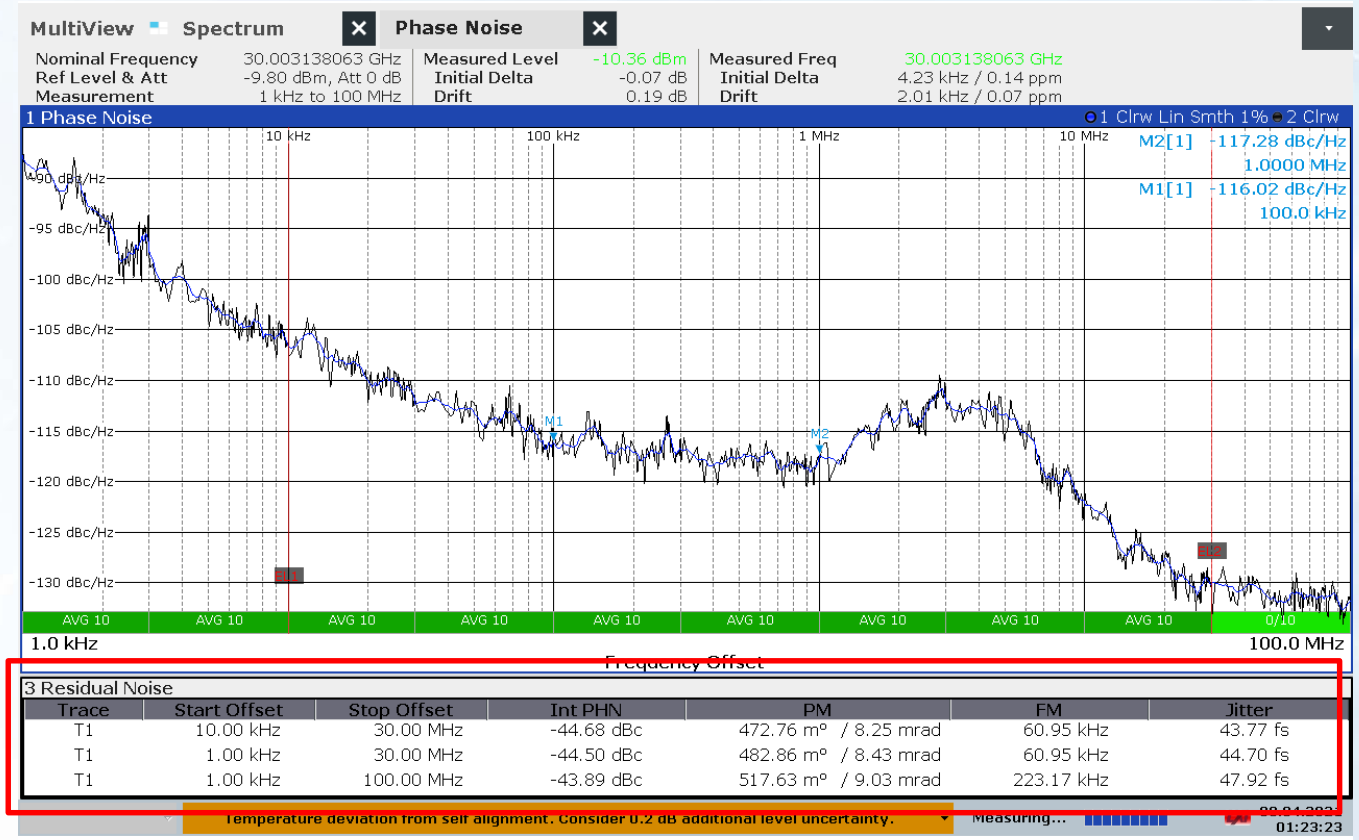




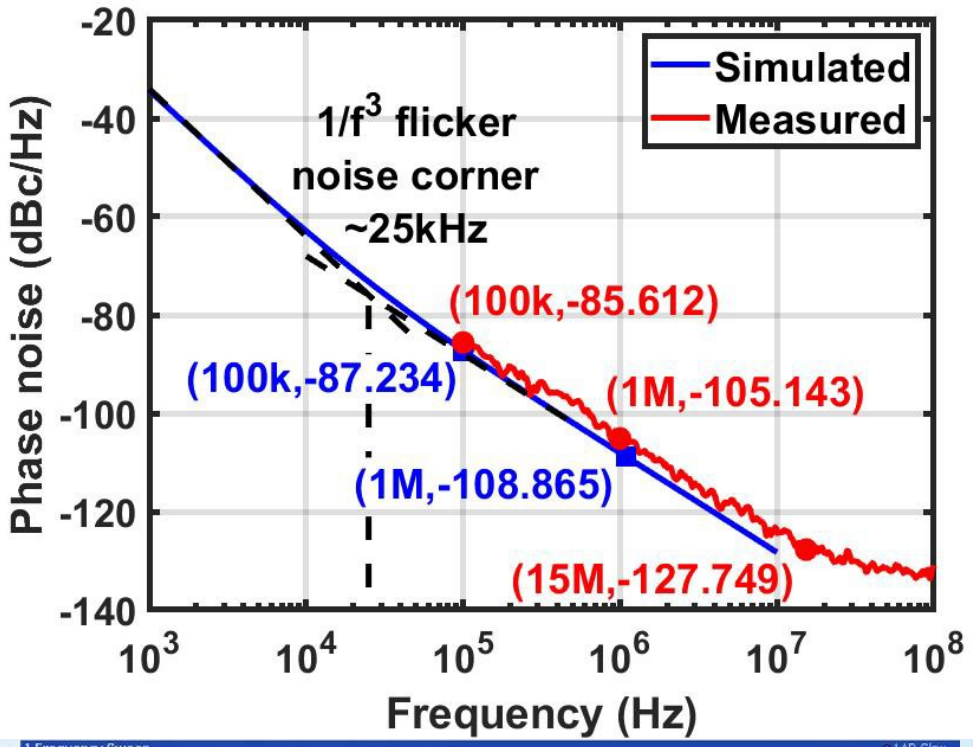
Host	PC + Arduino Nano
Master Power Supply	3 AA batteries in series
Reference Frequency	Wenzel Associates OCXO VHF (100MHz) or VHF Citrine (160MHz)
Output Probe (GSG100 or 150)	FormFactor Cascade Infinity
Output Spectrum	R&S FSW67 SA
Output Phase Noise	R&S FSWP50 Phase Noise Analyzer

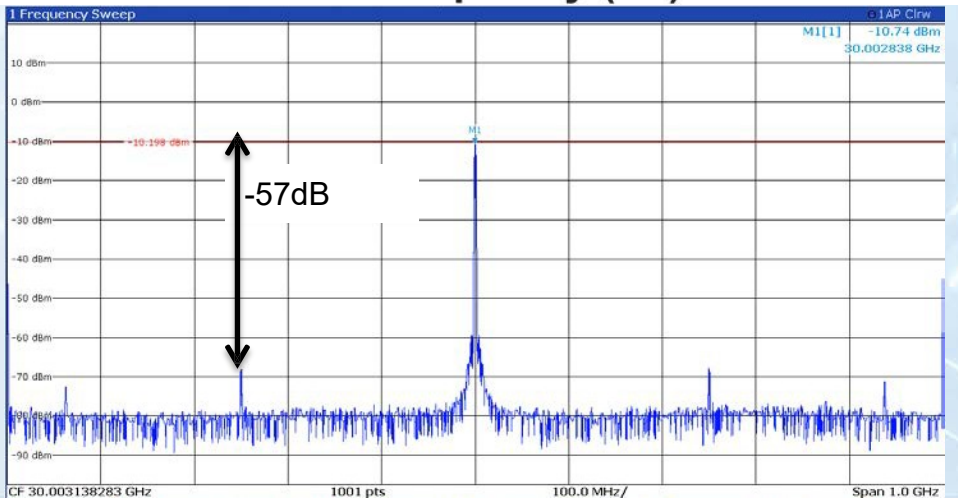
VCO AND PLL PERFORMANCE

- PLL at 30GHz
  - <50fs jitter
  - -117dBc/Hz @1MHz
  - Reference spur level = -57dBc



VCO Phase Noise





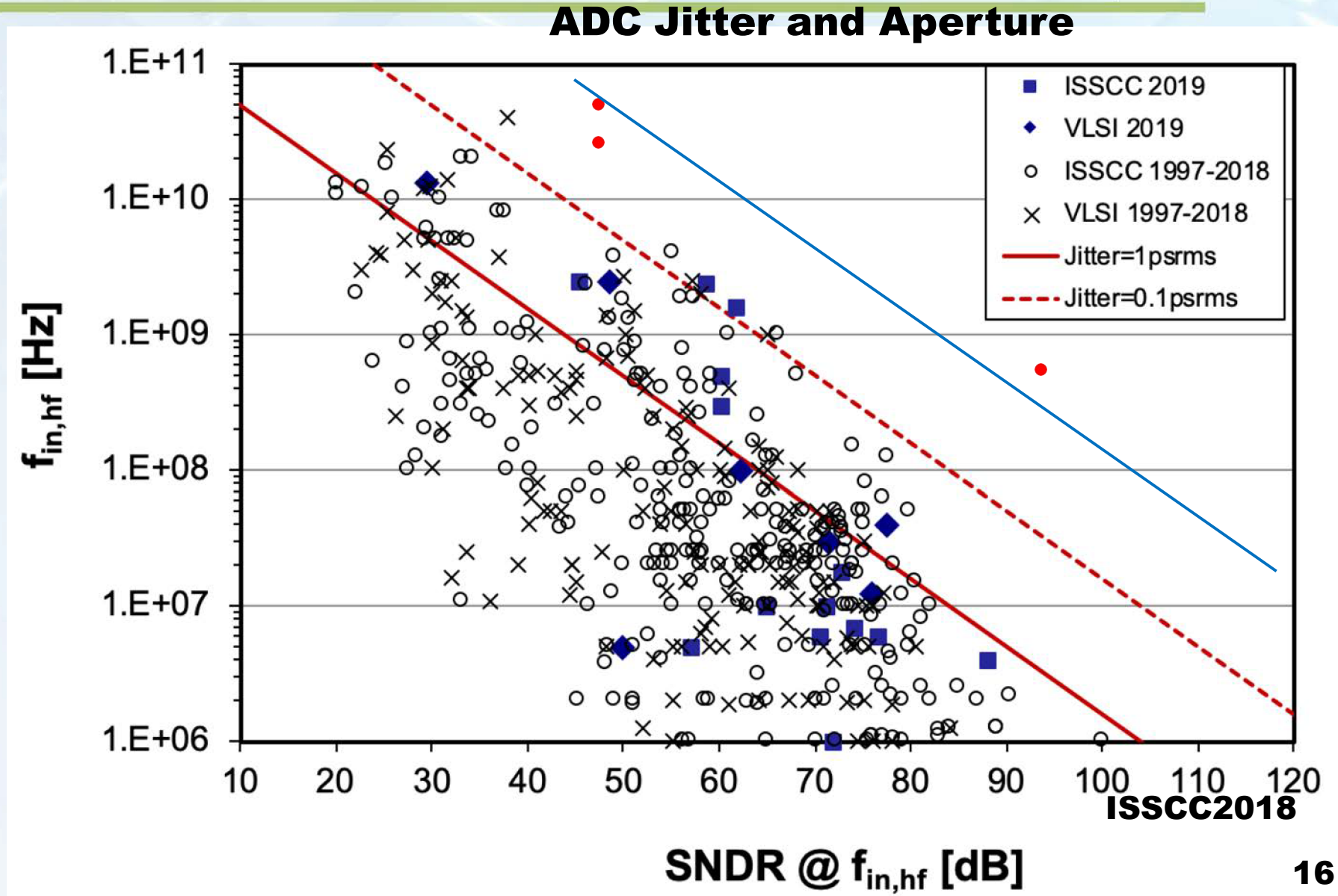
PERFORMANCE SUMMARY

- PLL Performance Comparison
  - Compared with other integer-N PLL at similar center frequency

	UCLA T-MUSIC	ISSCC20 17.6	ISSCC19 16.8	ISSCC19 16.2
Technology	0.18um SiGe BiCMOS	28nm CMOS	65nm CMOS	65nm CMOS
Technique	Sub-sampling PLL	Charge-Sharing Locking	Sub-sampling PLL	Sub-sampling PLL + ILFM
Ref. Freq (MHz)	250	250	103	100
Output Freq (GHz)	27-30	21.71-26.49	25.4-29.5	28-31
SPN 100kHz (dBc/Hz)	-112.23	-103.8	-112.5	-101.55
SPN 1MHz (dBc/Hz)	-114.85	-110.4	-112.8	-105.81
Jitter (fs) (Integration range, Hz)	43.77 (10k to 30M)	75.89 (10k to 30M)	71 (1k to 100M)	76.4 (1k to 30M)
	44.70 (1k to 30M)			
	47.92 (1k to 100M)			

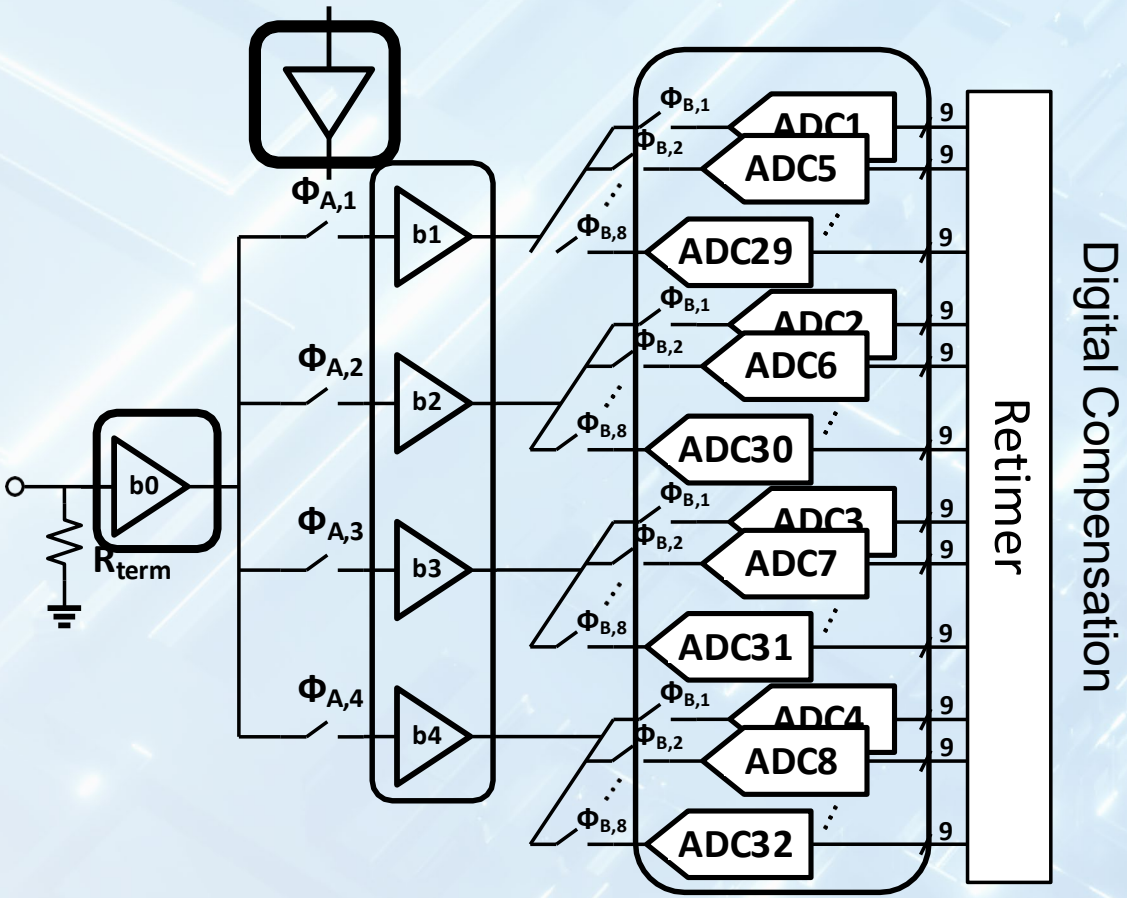
HIGH-PERFORMANCE ADC

- Benefit of SiGe
  - Low jitter
  - Buffering (power/noise)
- Benefit of CMOS
  - T/H and sampling
  - Digital linearization

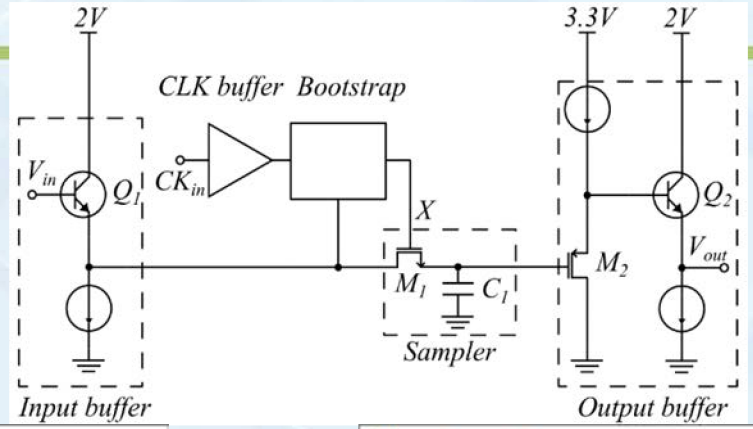


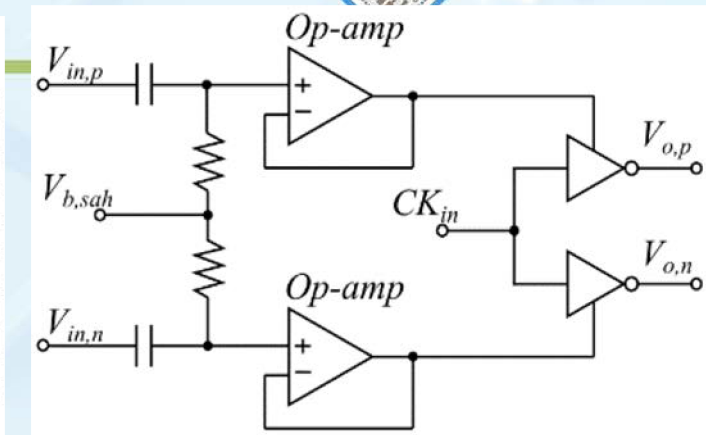
INTERLEAVE-SAMPLING AND LINEARIZATION

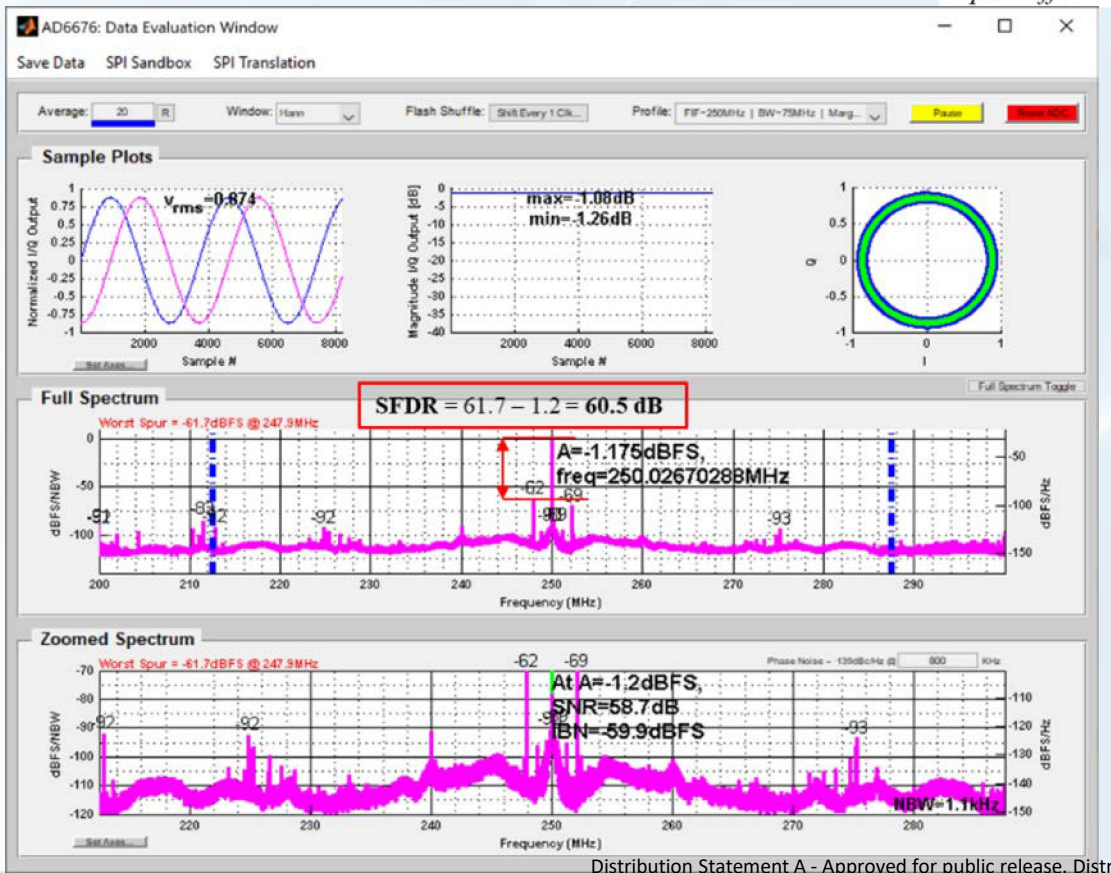
- Phase noise
  - Leverage PLL performance
  - Low noise buffering
  - Digital compensation
  - Accurate tuning of interleave paths makes design more challenging.
- Linearity
  - Leverage high inherent linearity of buffers
  - Digital compensation.

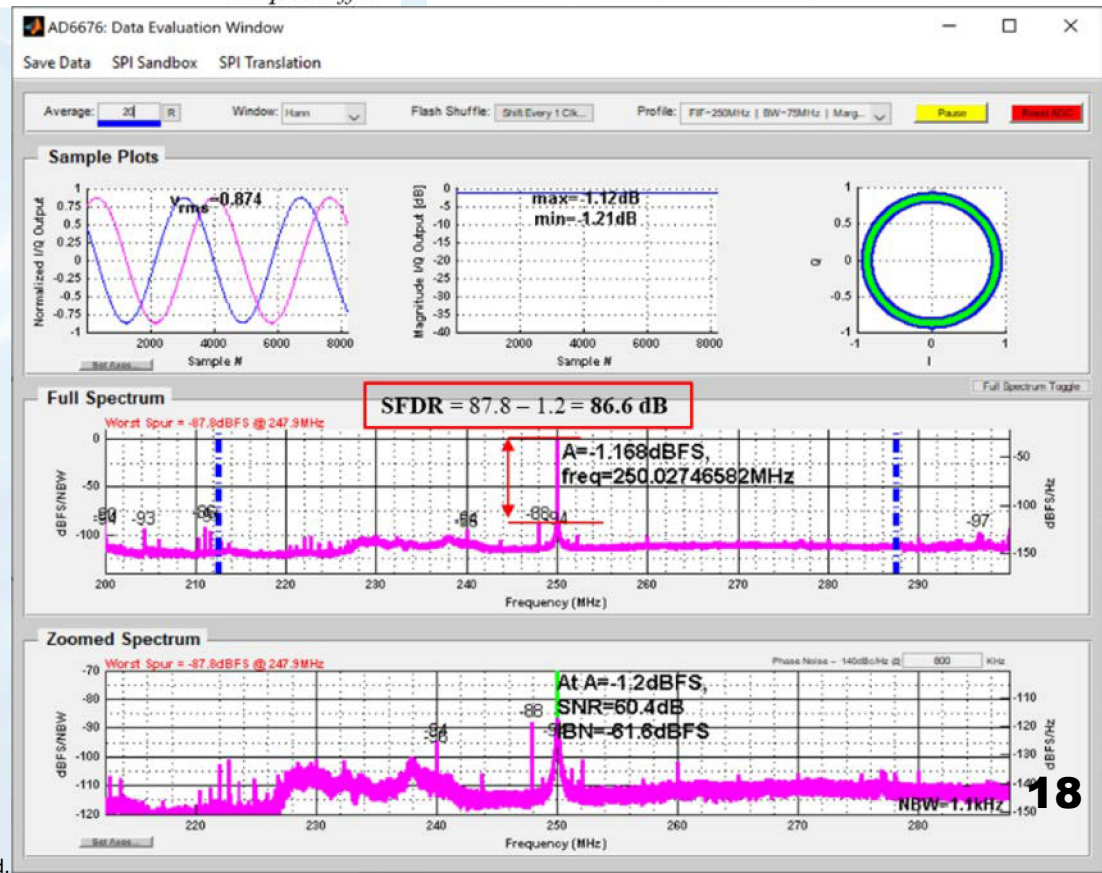


EXAMPLE: BOOST-STRAP TAH

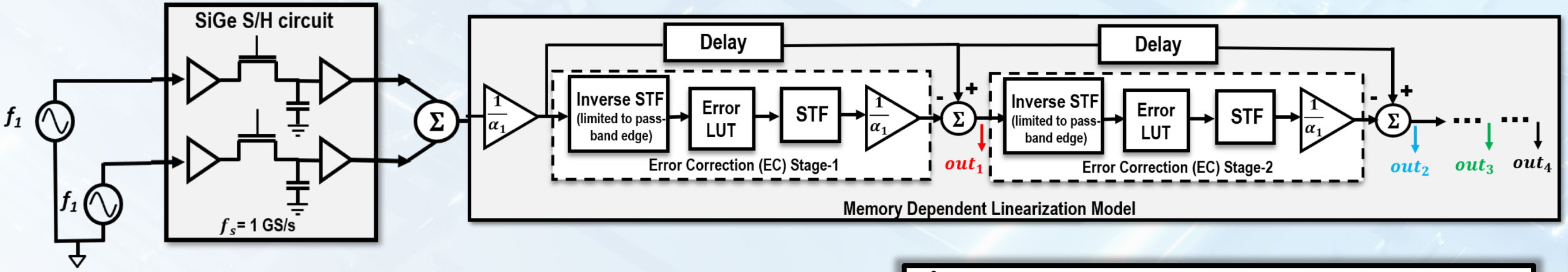




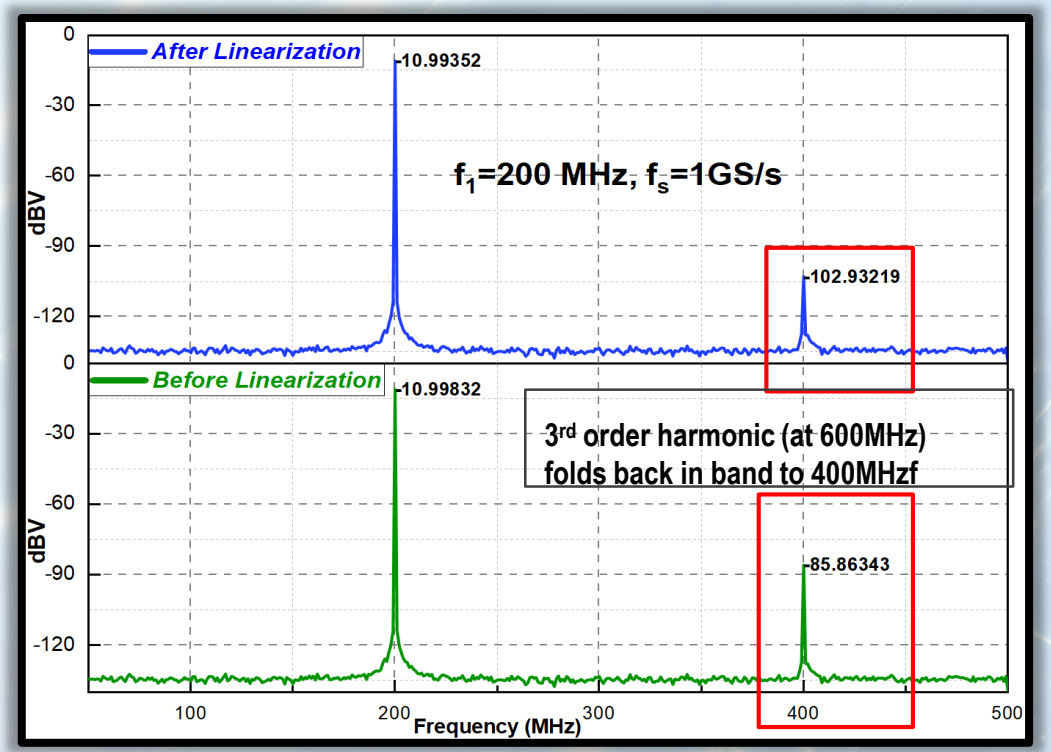




EXAMPLE: DIGITAL LINEARIZATION



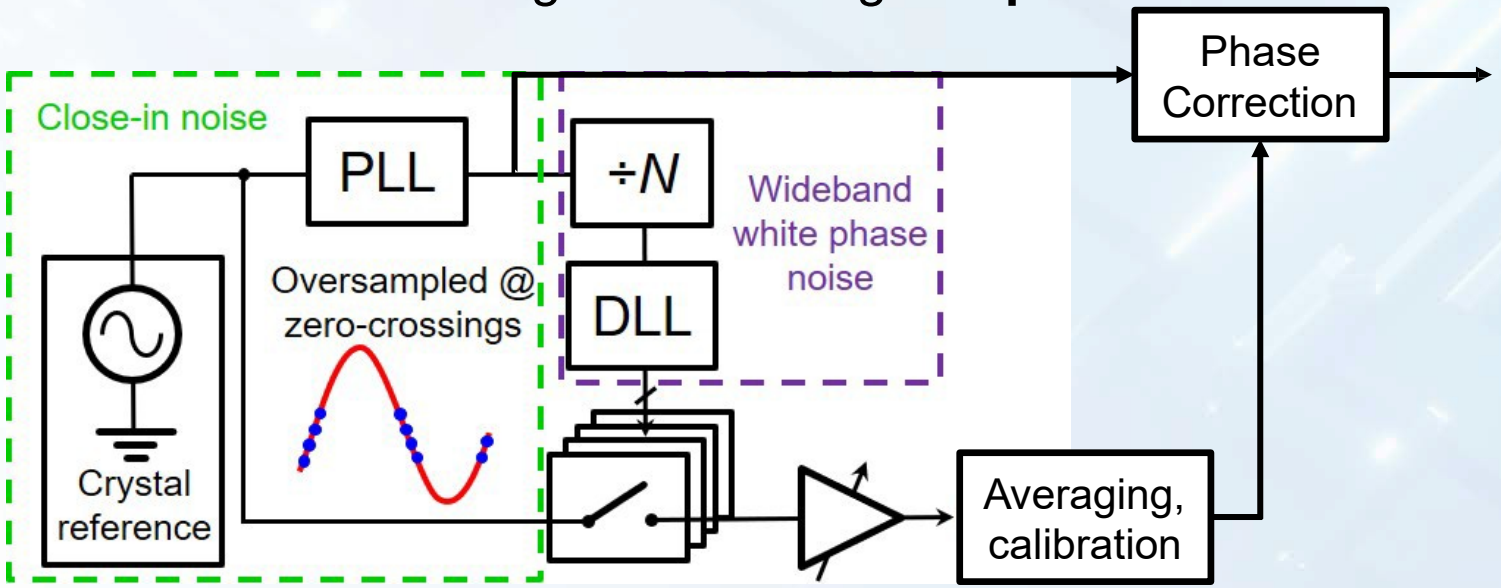
Input Frequency (MHz)	Before Linearization Relative HD3 (dBc)	After Linearization Relative HD3 (dBc)	Linearization (dB)
! " "	-74.82	-92.85	18.03
# " "	-74.87	-91.94	17.07
$ " "	-75.93	-82.96	7.03

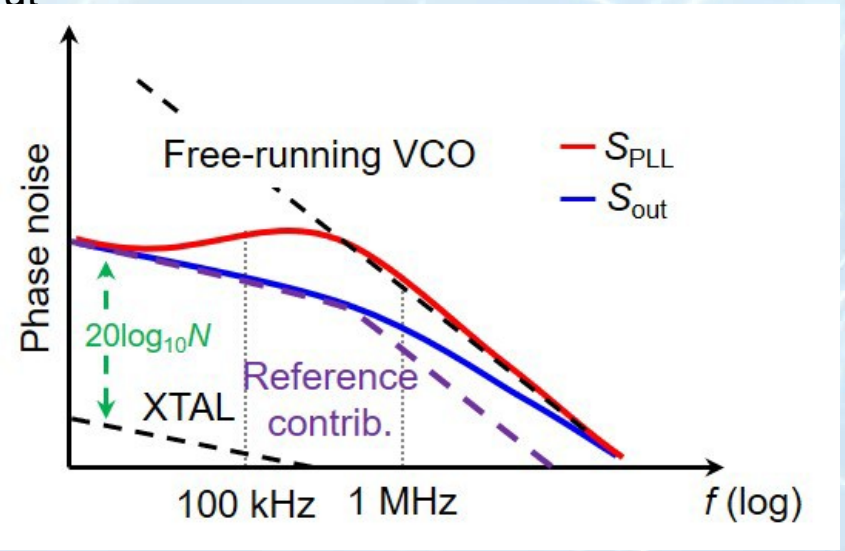


- Compensation of nonlinearity **saves power**
  - Can be memoryless or memory dependent
  - Fully CMOS digital backend

EXAMPLE: SAMPLING JITTER COMPENSATION

- Reduce PLL jitter through feedforward phase noise cancellation
  - Oversample clock jitter during rising/falling edges and correct using phase interpolators
  - Enables wide bandwidth cancellation - limiting factor in prior art
- Anticipated key building block performance
  - ~200ps rise/fall times, ~10ps DLL resolution, 20 sampling points - target 10fs rms
- Combine **SiGe DLL** to reduce wideband noise with **CMOS calibration**
  - Same building blocks for digital **Spur Cancellation**





With the possibility of >500GHz f_T and finFET CMOS!

The future of Hybrid Mixed-Signal Electronics is bright!

It opens up applications needing *extreme performance*.

ERI ELECTRONICS RESURGENCE INITIATIVE
SUMMIT
& MTO Symposium

QUESTIONS

Negative Capacitance Enabled Scaling to Achieve 1 THz Cut-off Frequency Transistors on a CMOS Platform

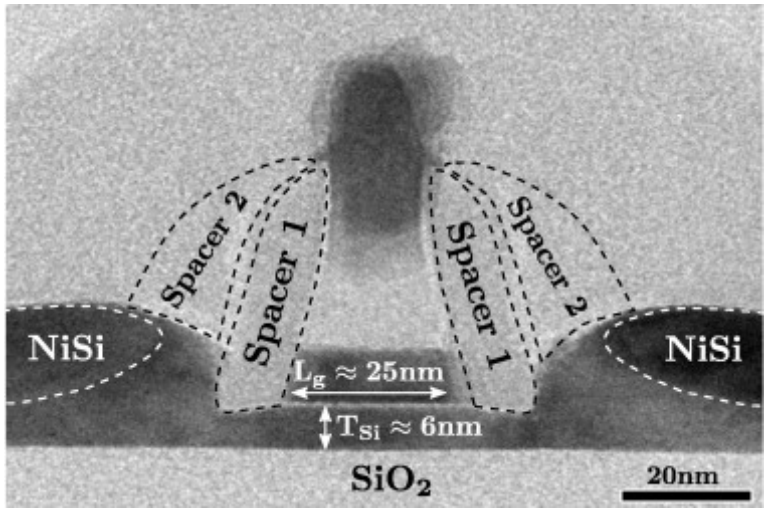
S. Salahuddin, UC Berkeley

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).

The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

Negative Capacitance Enabled Scaling to Achieve 1 THz Cut-off Frequency Transistors on a CMOS Platform

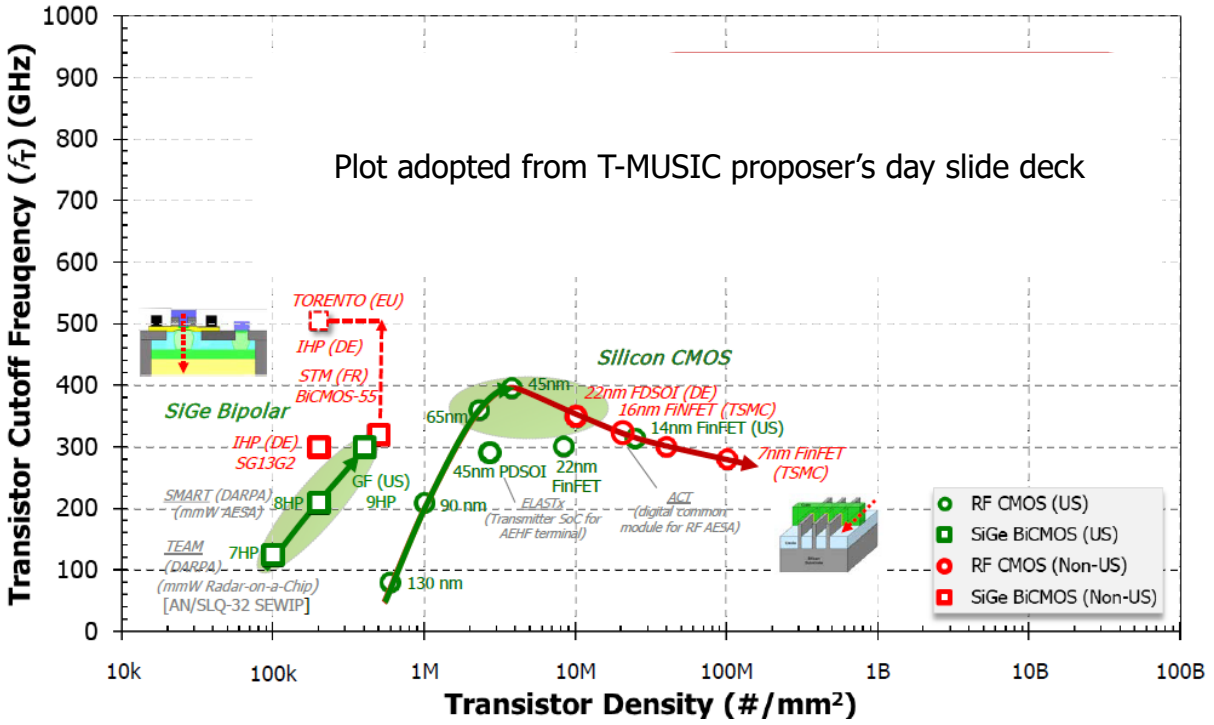
S. Salahuddin, A. Niknejad, TJK Liu: UC Berkeley, S. Datta : Univ Notre Dame



A typical FDSOI transistor

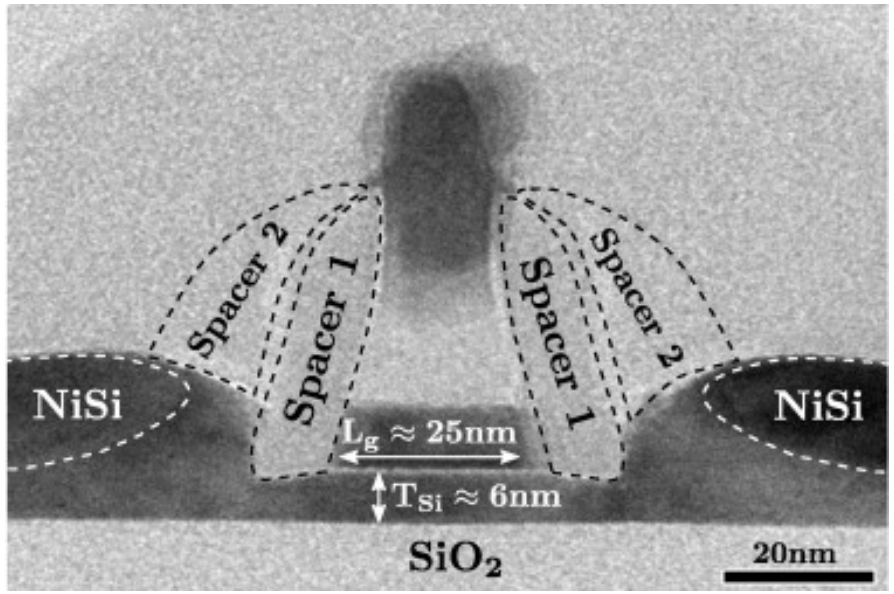
Proposed Solution

- Increase Cox without giving up mobility
  - i. to aid further scaling well below 20 nm
  - ii. to reduce the effect of parasitic capacitance
- Reoptimize transistor structure for high frequency operation, e.g., by air gap spacers

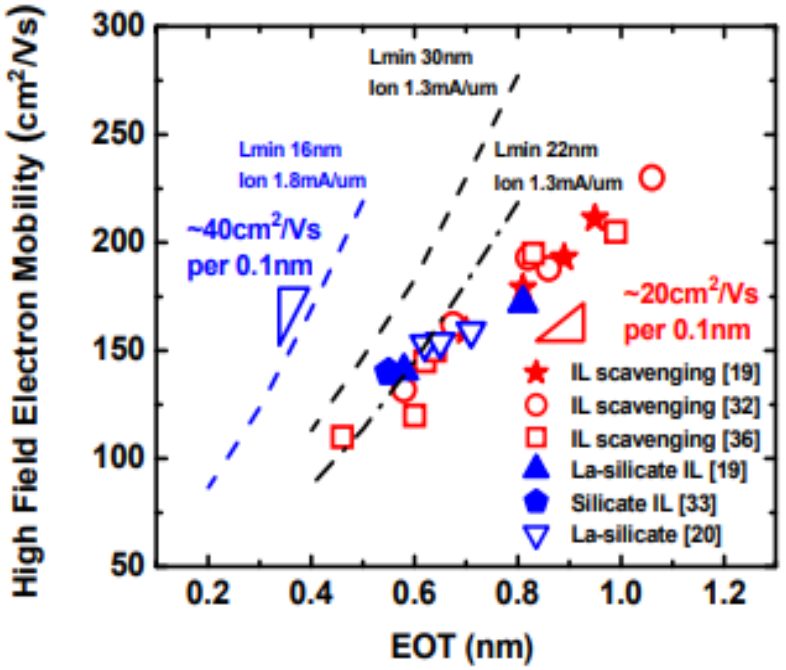


- Scaling is driven by the need to maximize the number of transistors achievable per unit area
- 3D structures bring in additional parasitic capacitance

Overview: Fundamental Premise

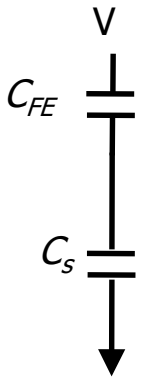


$$L_{critical} = \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}(t_{ox})(t_{SOI}) + \frac{t_{SOI}^2}{2}}$$

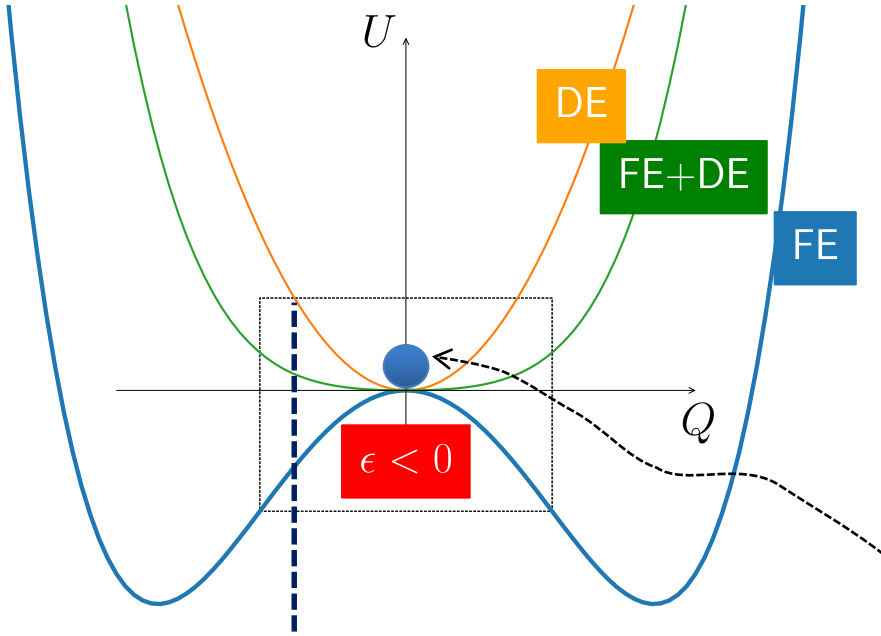


Conventionally lowering EOT using scavenging lowers mobility

Negative Capacitance



$$C = \frac{|C_{FE}||Cs|}{|C_{FE}| - Cs}$$

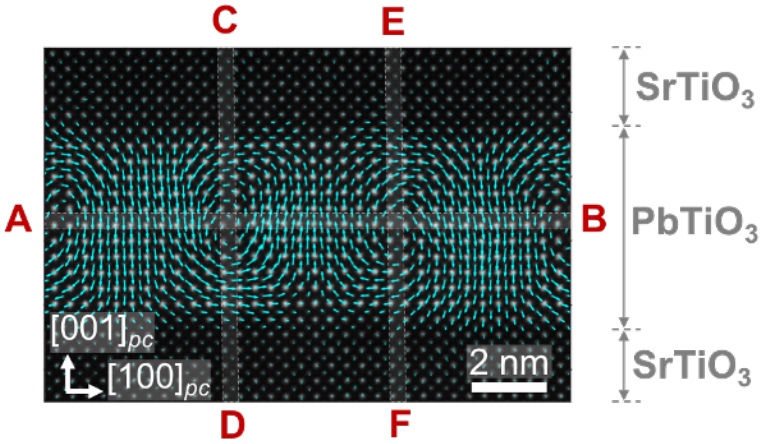


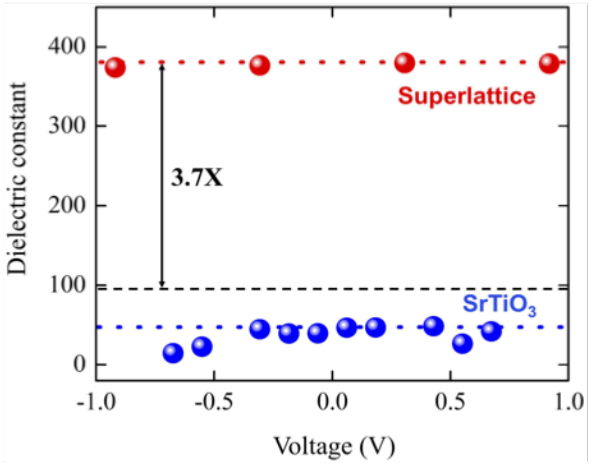
Total energy is minimized, where, locally, FE is at a local maxima

Less Energy for the same Q for FE+DE

$$U = \frac{Q^2}{2C}$$

Exploiting Negative Capacitance





[Yadav et al Nature, 565, 7740, 468–471, 2019]

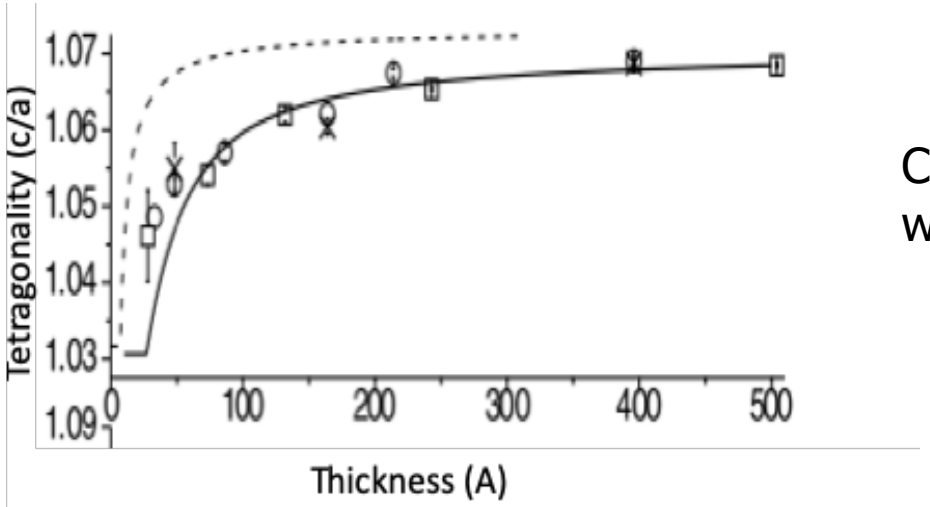
HfO_2

ZrO2

HfO_2

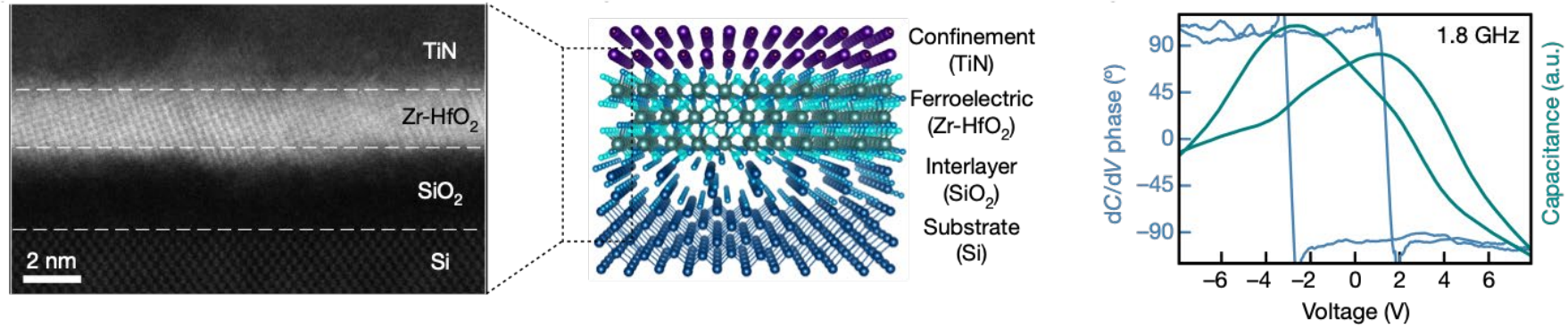
Superlattice Design

Material development: World's thinnest FE on Si



Conventional FE weakens with thickness

[Lichtensteiger et al, Phys Rev. Lett, 94, 047603, 2005]



[S. Cheema et.al, *Nature* 580 (7804), 478-482, (2020)]

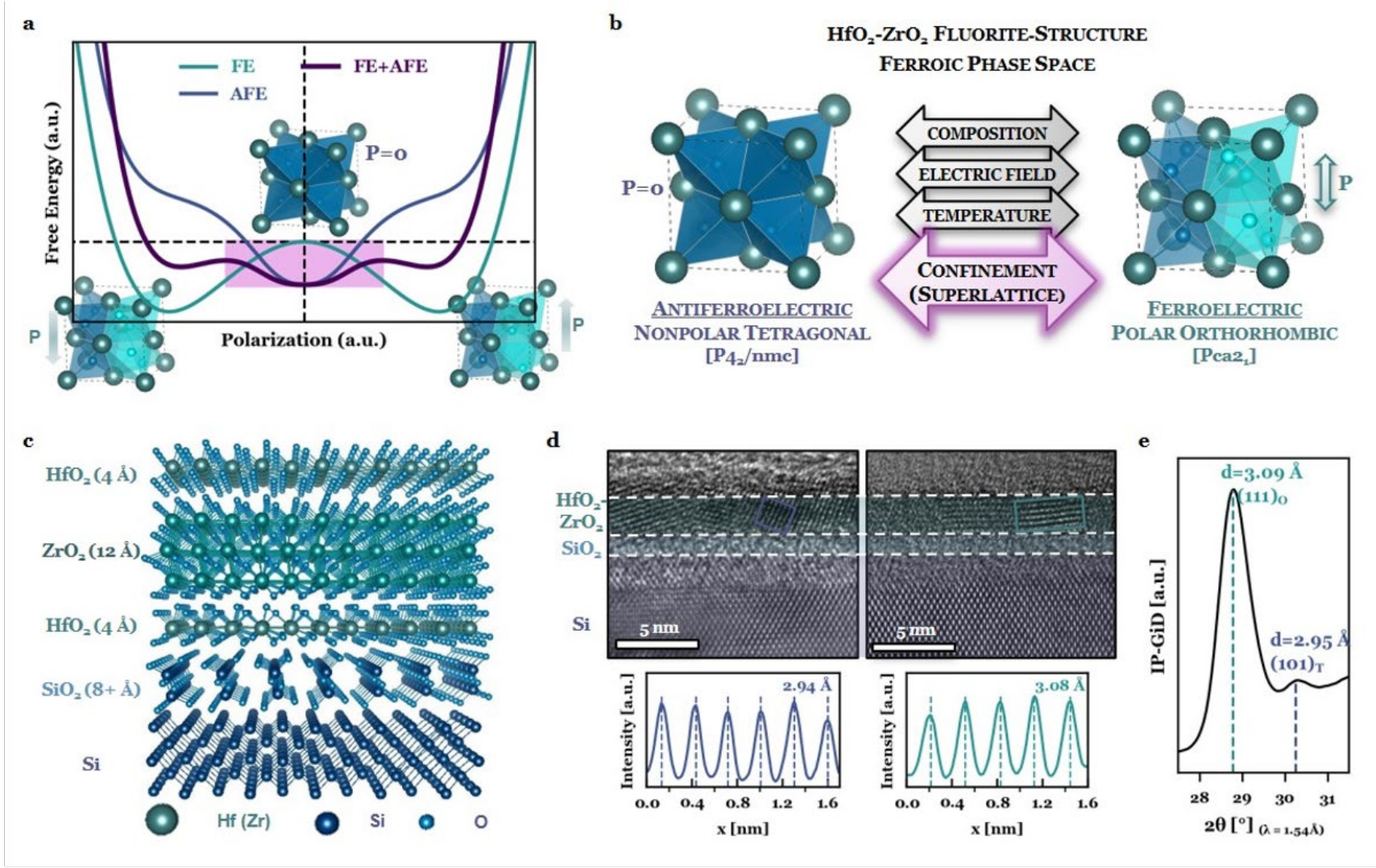
Superlattice Design

HfO_2

ZrO2

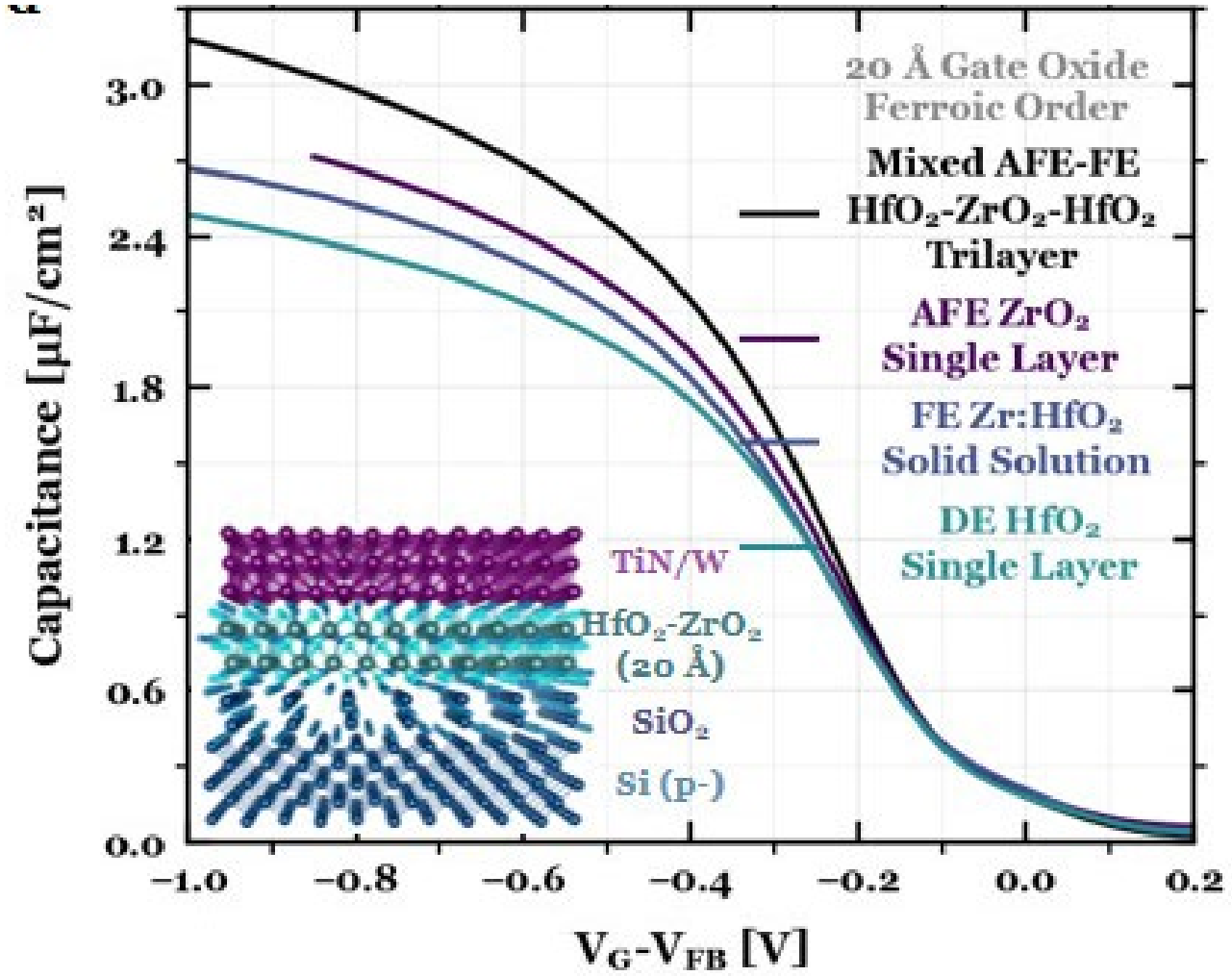
HfO_2

Superlattice Design

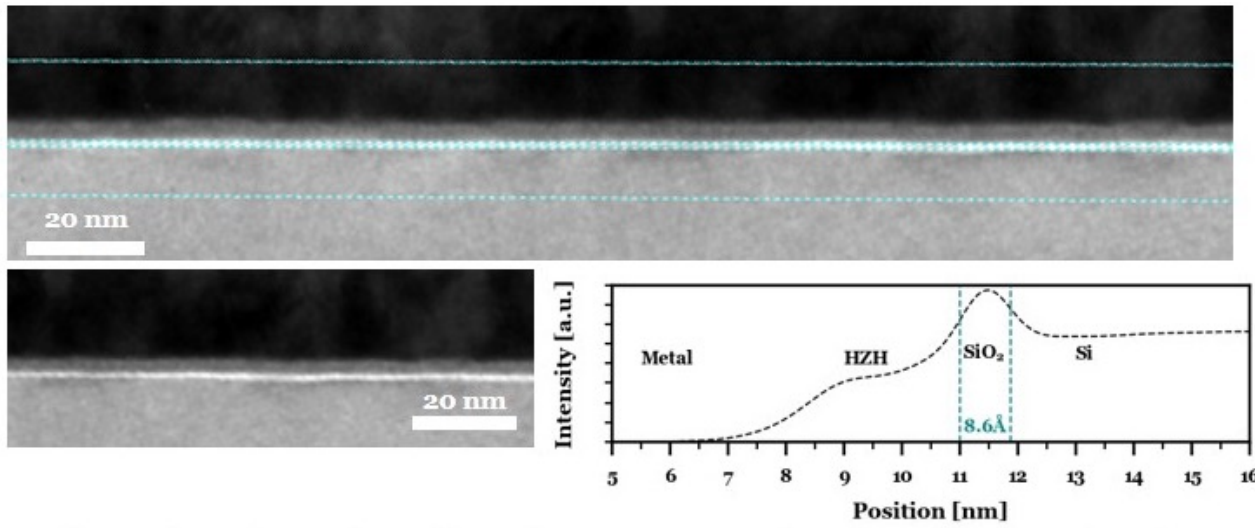


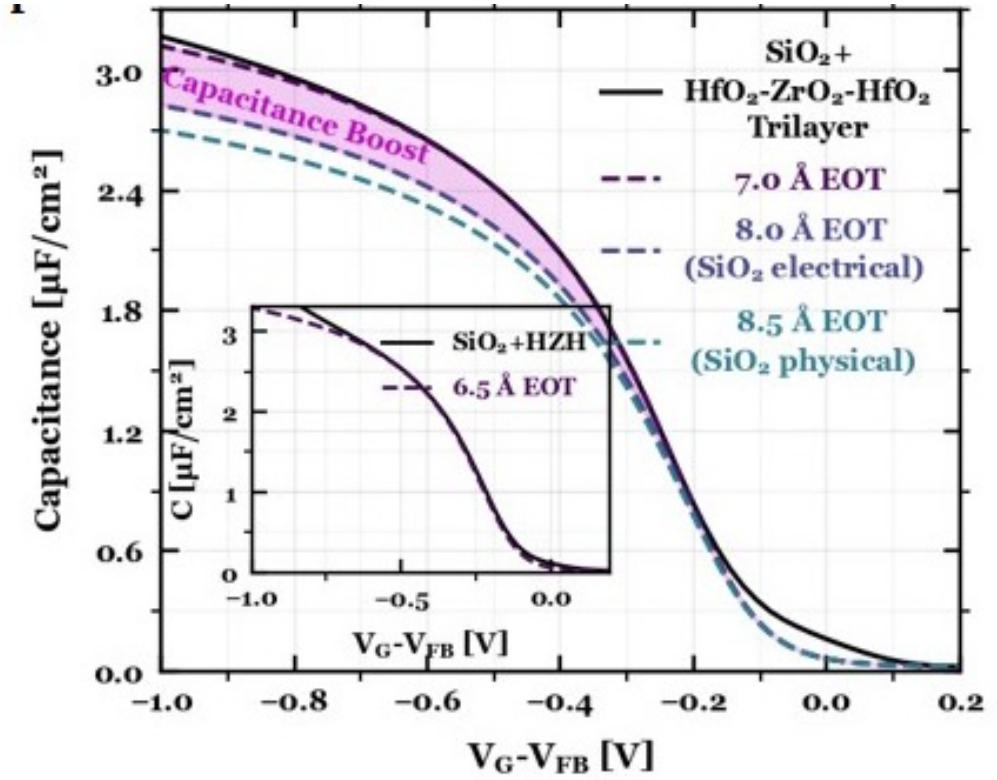
A mixed phase FE-AFE within just 1.8 nm

Capacitance Results



Negative Capacitance Gate Stack

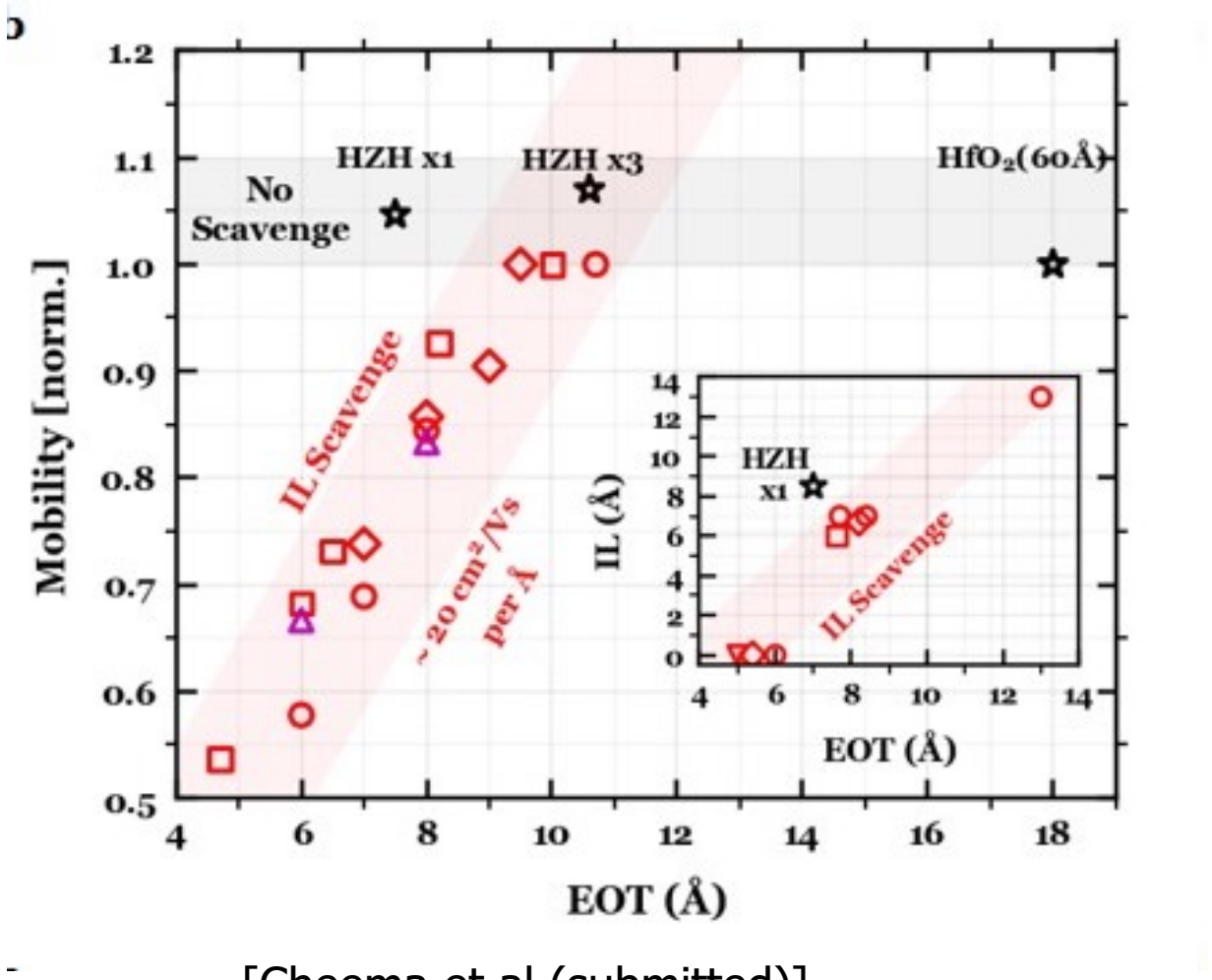




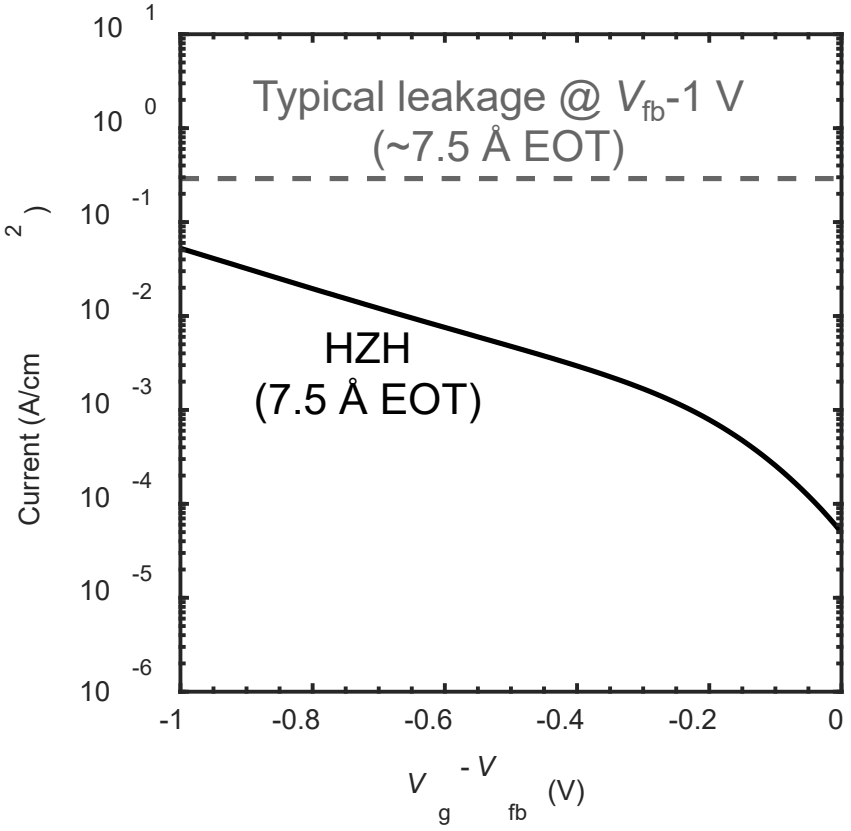
- Reaching EOT ranges that was not possible before without IL scavenging
- Mobility degradation is not present because IL has not been scavenged

Negative Capacitance Gate Stack: No mobility Degradation is observed

No mobility degradation

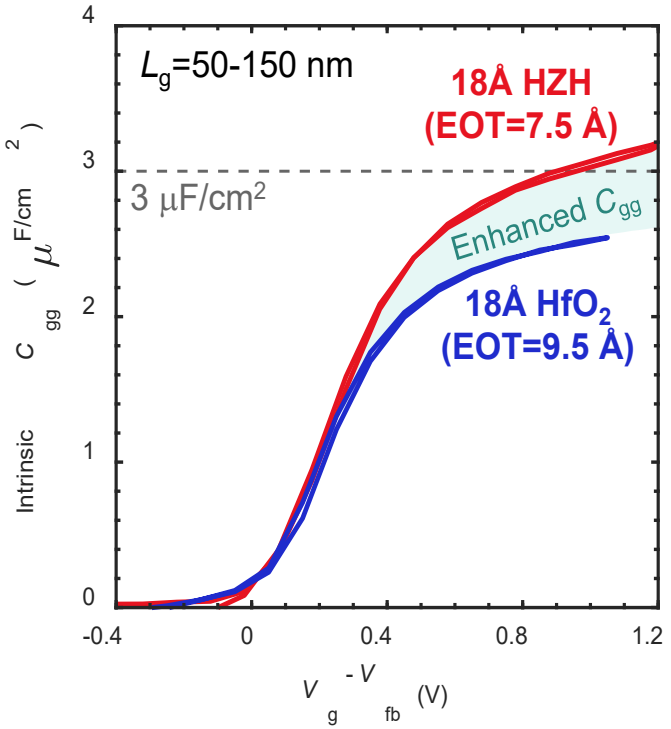


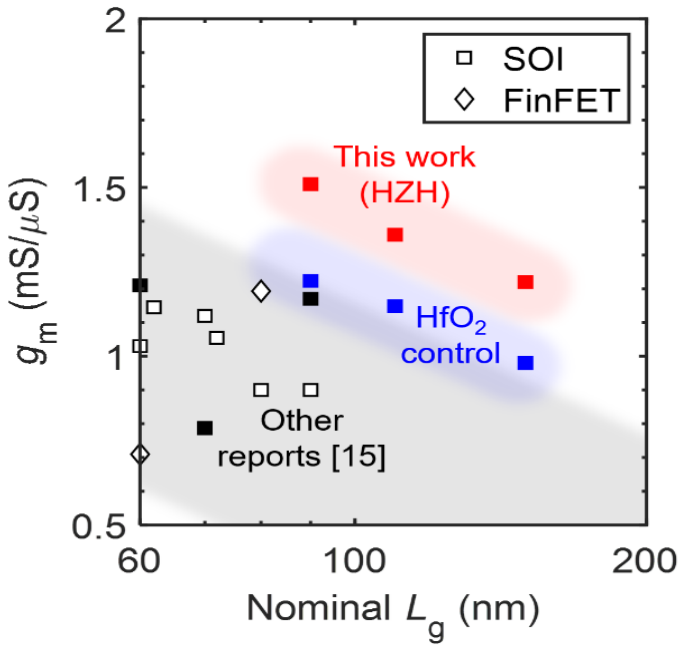
[Cheema et al (submitted)]



RF Transistors at Lg=90 nm

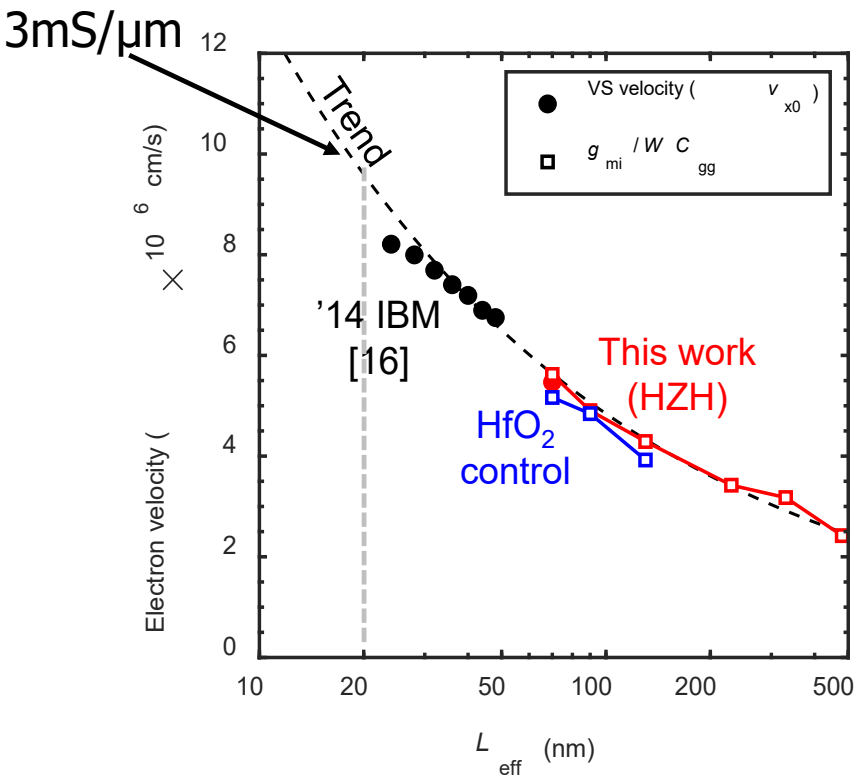
Extracted from 25 GHz measurements

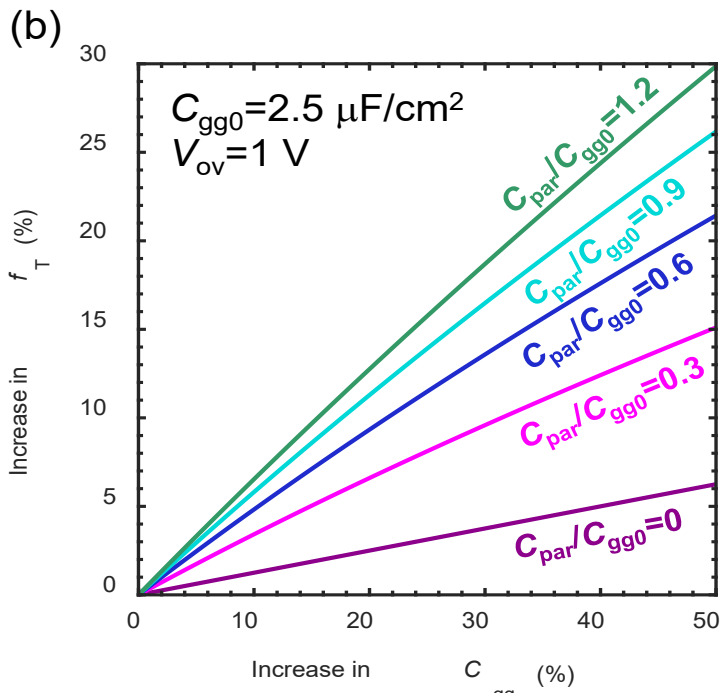




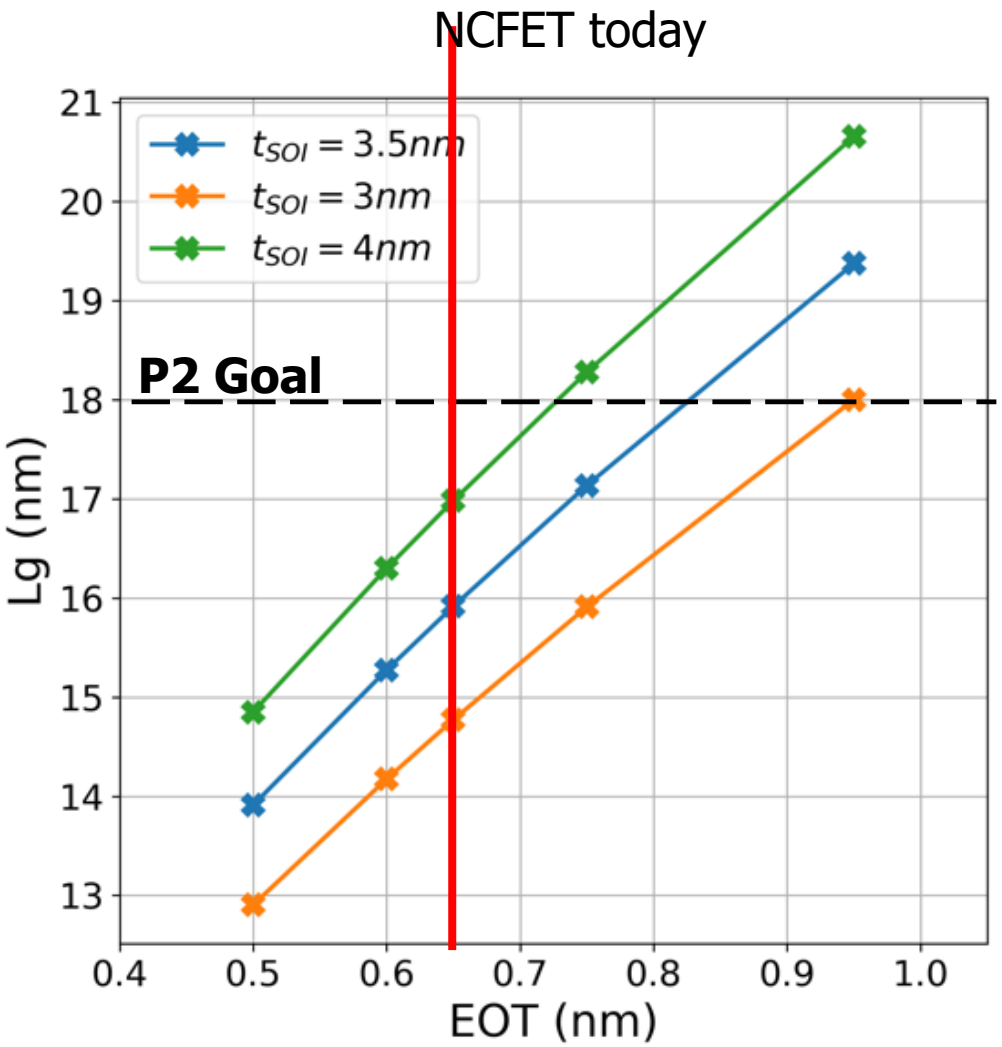
Trends In Velocity

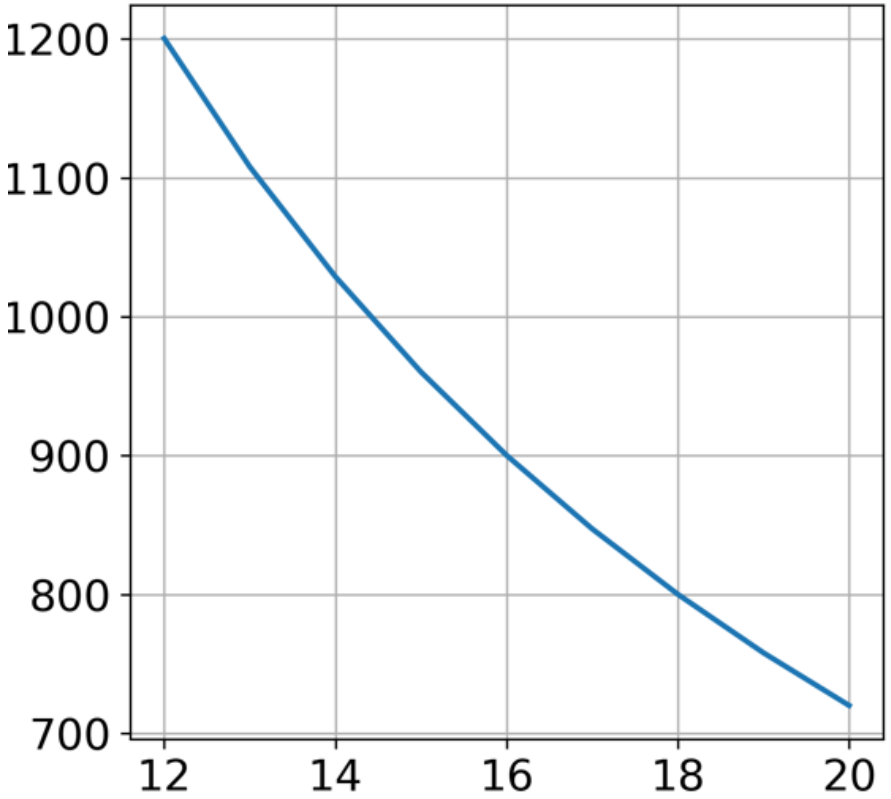
No change in velocity, the increase in gm comes from increased Cox





Towards 1 THz Cut-off Frequency





Assumes the same Rs, Rd and Rg as 22 nm FDX and air-gap spacer

Conclusion

- Negative Capacitance allows to overcome the traditional barrier of losing mobility while trying to access EOT below 8A
- 6.5 A EOT without any degradation on velocity has been demonstrated
- Fabricated devices at Lg=90 nm shows record transconductance
- Further reduction to EOT=6A and an air-gap spacer (already in production research for digital MOSFETs) shows promise for planar FDSOI to reach 1 THz cut-off frequency

www.darpa.mil

2021 DARPA ERI Summit and MTO Symposium, online event, October 19-21,
WORKSHOP: Next Generation Mixed-Mode Microelectronics, Wednesday, October 20, 3:15pm – 5:30pm
presentation 5:00-5:15PM EDT
https://eri-summit.darpa.mil/

Looking to the Future Through a High-Speed InP Lens

Mark Rodwell

University of California, Santa Barbara

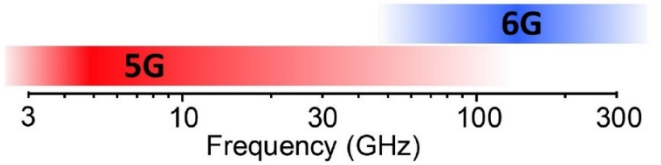
The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

50-300GHz Wireless: Terabit Aggregate Capacities

Wireless networks: rapidly increasing demand.

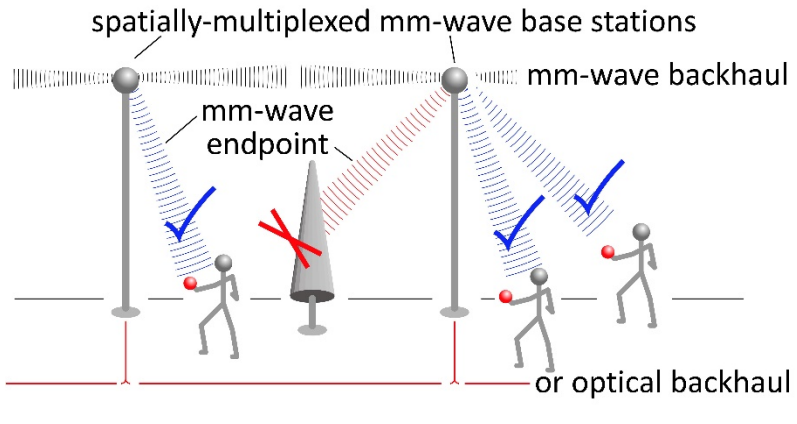
High frequencies→ plentiful spectrum→ high capacity

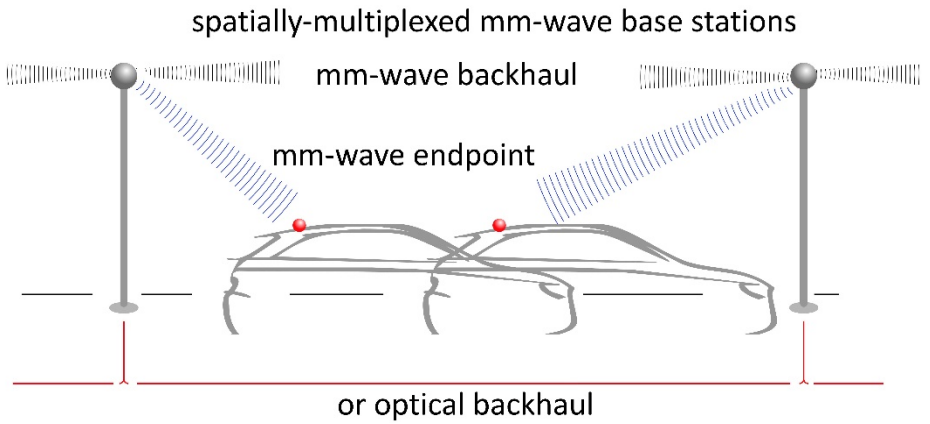
Short wavelengths→ many beams→ massive capacity

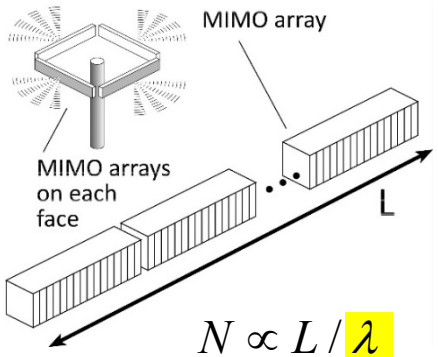


50-300GHz carriers, massive spatial multiplexing

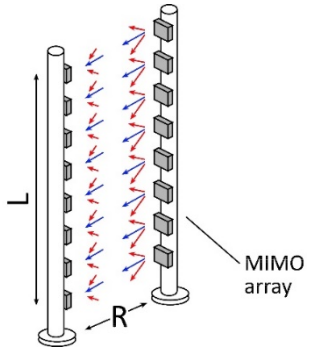
→ Terabit hubs and backhaul links, near-video-resolution short-range radar





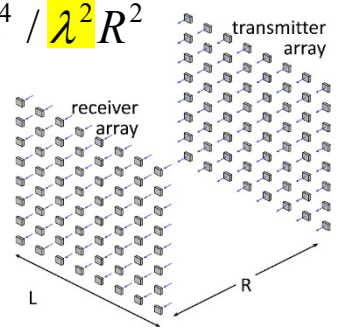


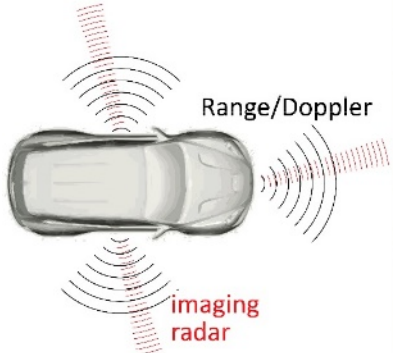
$N \propto L / \lambda$



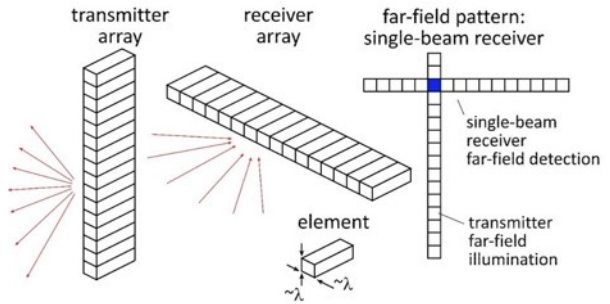
$N \propto L^2 / \lambda R$

$N \propto L^4 / \lambda^2 R^2$





$\Delta\theta \propto \lambda / L$



CMOS alone won't do it.

Wireless needs: low noise, high power & efficiency.

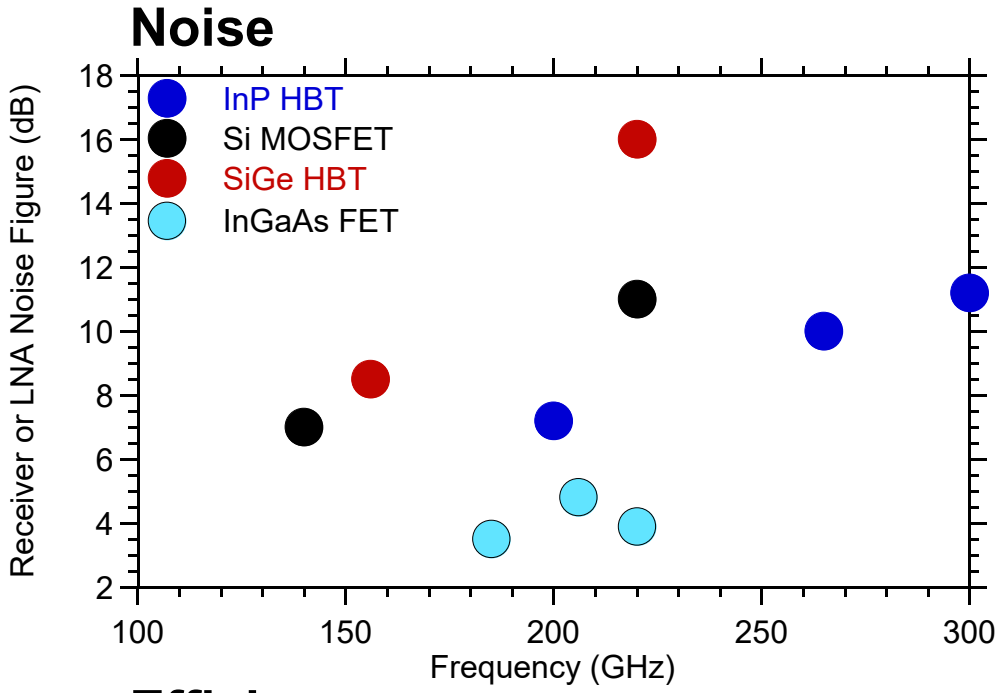
CMOS: good to ~150GHz. Not much beyond.

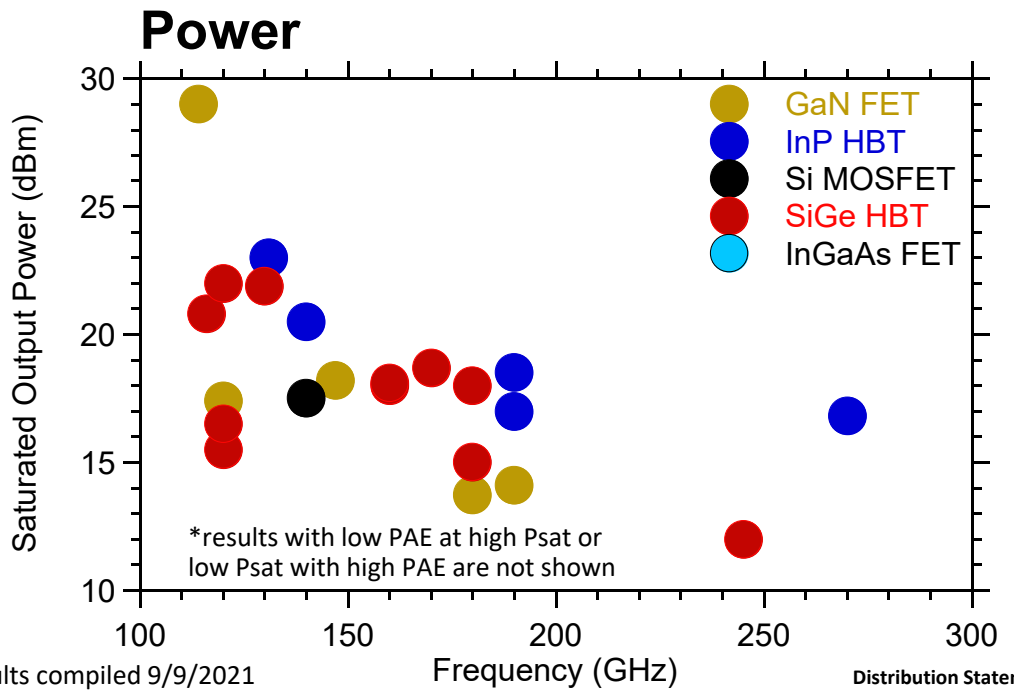
InP HBT: record-efficiency 100-300GHz PAs

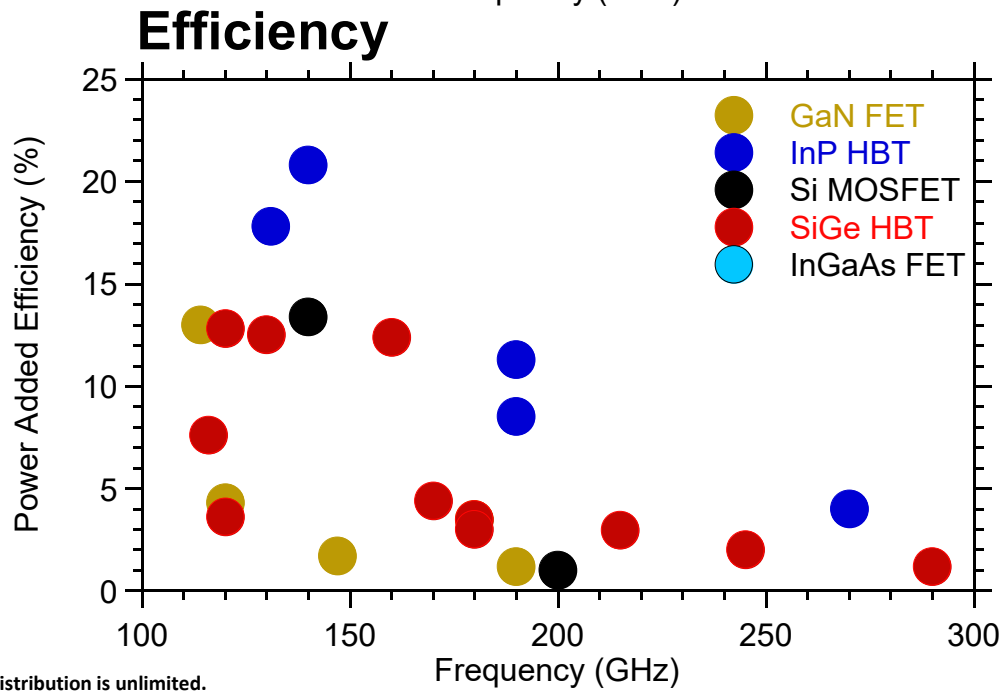
SiGe HBT: power better than CMOS, lower PAE than InP HBT

GaN HEMT: record power below 100GHz. Bandwidth improving

InGaAs-channel HEMT: world's best low-noise amplifiers







Results compiled 9/9/2021

Why InP Bipolar Transistors ?

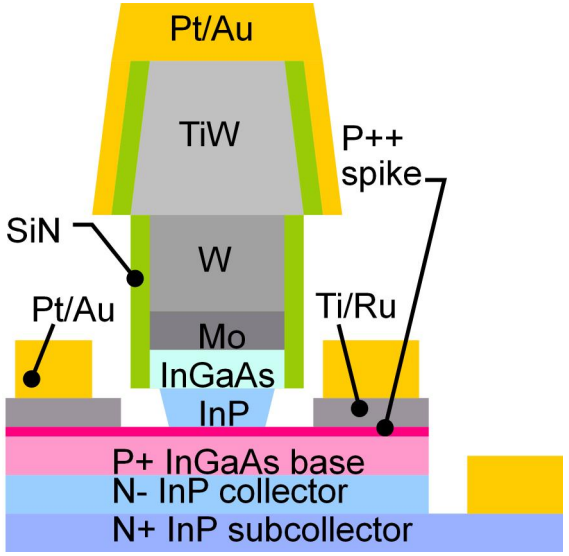
InP: excellent high-field transport
high (peak) electron velocity: 3.5×10^7 cm/s (Si: 1.0×10^7 cm/s)
wide bandgap→ high breakdown field

InGaAs base, base-emitter heterojunction:
very low base sheet resistance

Implications:
Higher (f_τ, f_{max}) at a given scaling node
Higher operating voltage* at a given (f_τ, f_{max})

*Transistor voltage limits are too complex to summarize with BVCEO.
BVCBO vs. BVCEO vs. safe operating area ?
Bottom line: look at ($V_{ce,max}$, $J_{e,max}$) used in published IC data for a given IC technology.

Bipolar Transistor Scaling Laws



to double the bandwidth:	change
emitter & collector junction widths	decrease 4:1
current density (mA/μm^2)	increase 4:1
current density (mA/μm)	constant
collector depletion thickness	decrease 2:1
base thickness	decrease 1.4:1
emitter & base contact resistivities	decrease 4:1

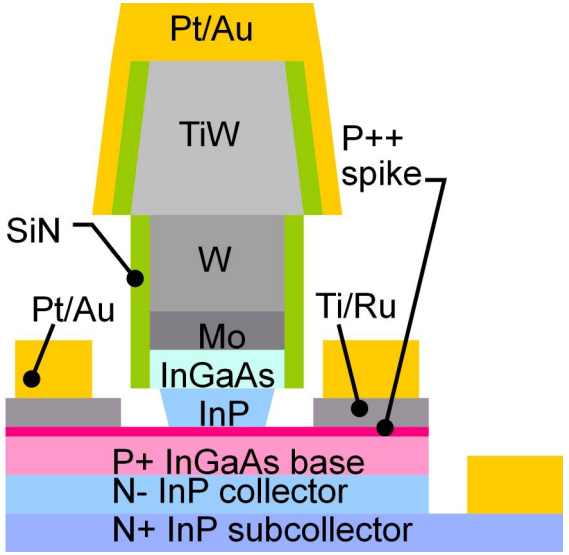
Narrow junctions.

Thin layers

High current density

Ultra low resistivity contacts

InP Bipolar Scaling Roadmap



emitter				
junction width	256✓	128✓	64 (?)	nm
access resistivity	8	4	2	Ω–μm²
base				
thickness	2.5	2.5	2.0	nm
contact width	256	128	64	nm
contact resistivity	10	5	2.5	Ω–μm²
collector				
thickness	150	100	70	nm
current density	2.8	3.5	3.5	mA/μm
breakdown (ceo)	4.6$_{meas}$	3.5$_{meas}$	3.1$_{meas}$	V
f_τ	416$_{meas}$	520$_{meas}$	900$_{calc.}$	GHz
f_{max}	755$_{meas}$	1150$_{meas}$	1600$_{calc}$	GHz

Narrow junctions.

Thin layers

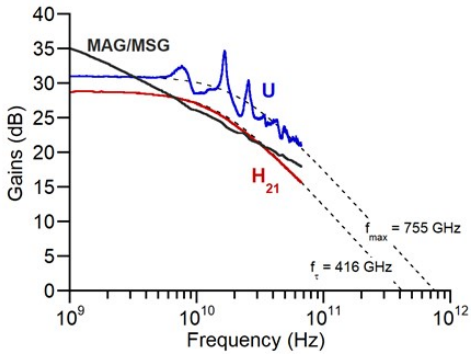
High current density

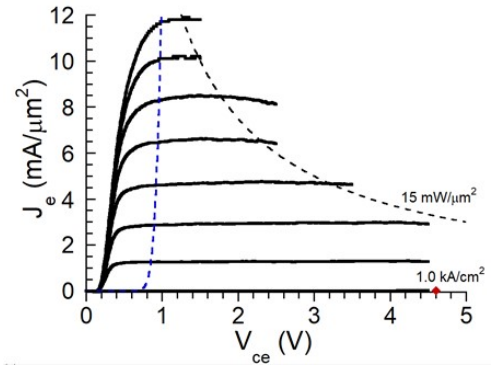
Ultra low resistivity contacts

250nm / 700GHz InP HBT Technology

750GHz / 4.5 V transistor

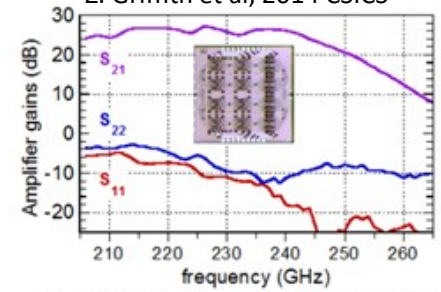
Z. Griffith et al 2007 IPRM

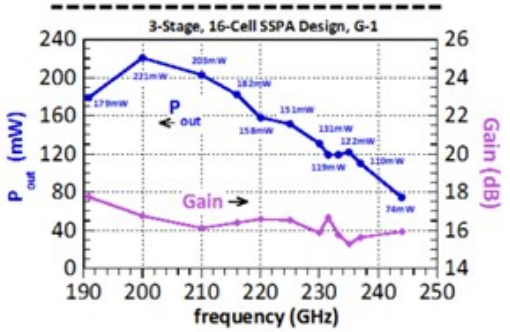




200GHz power amplifier: 23dBm

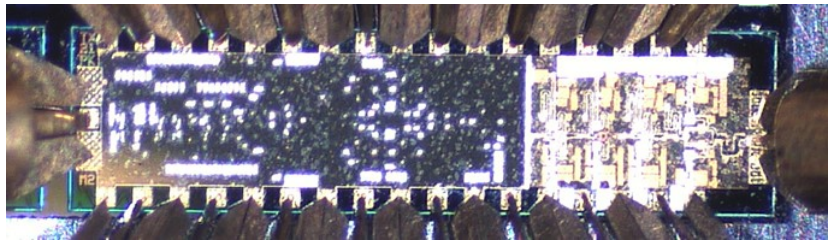
Z. Griffith et al, 2014 CSICS





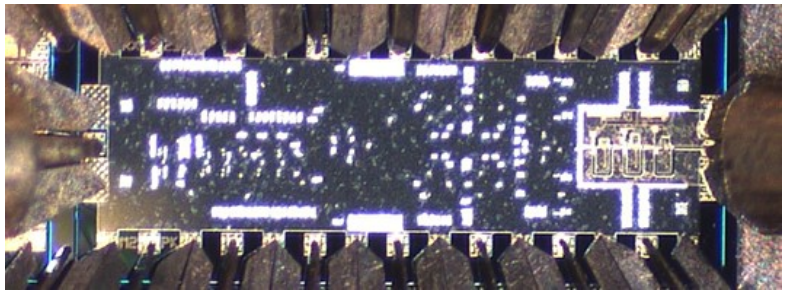
190GHz transmitter: 16.5dBm power

M. Seo et al, 2021 IMS



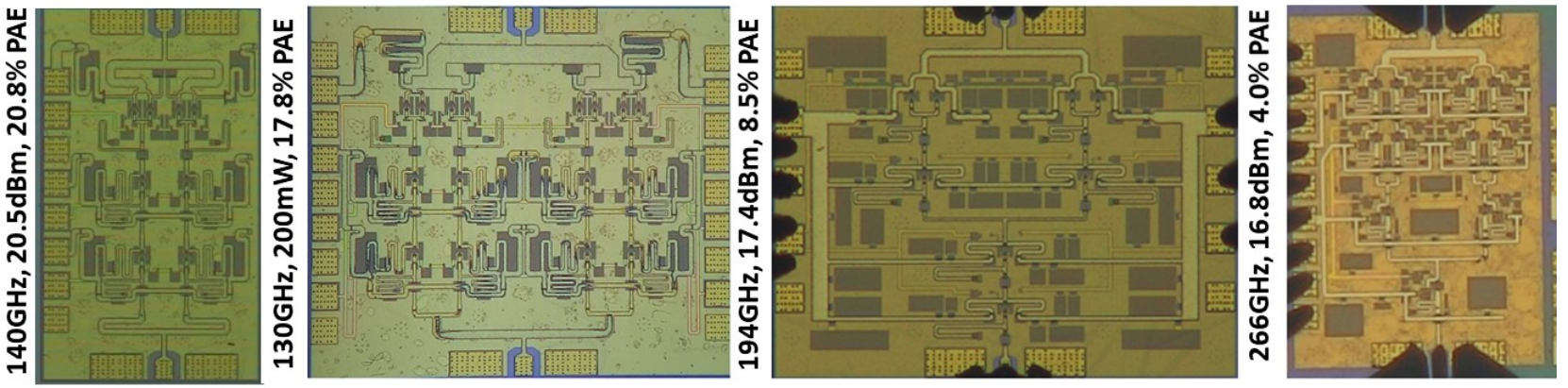
200GHz receiver: 8.0dB noise figure

M. Seo et al, 2021 IMS



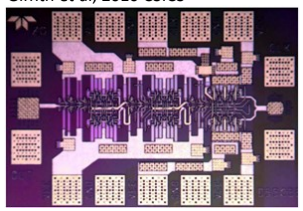
130-270GHz power amplifiers: record efficiencies

Ahmed et al, 2020 IMS, 2020 EuMIC, 2021 IMS, 2021 RFIC



204.9GHz static divider (M/S latch)

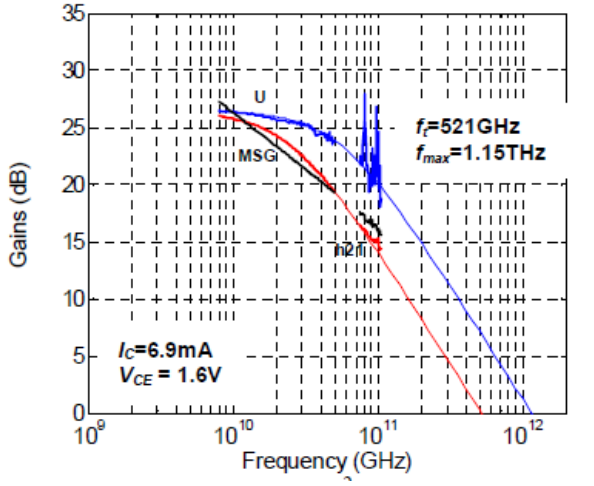
Giffith et al, 2010 CSICS

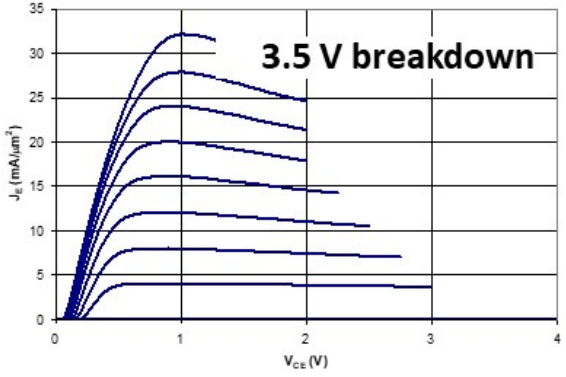


130nm / 1.1THz InP HBT Technology

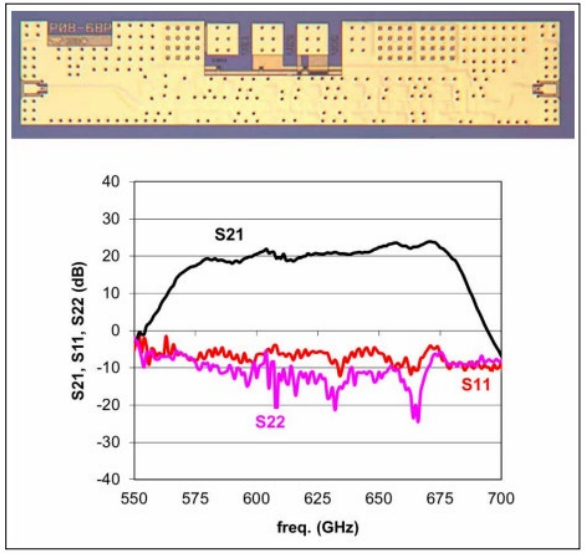
Teledyne: M. Urteaga *et al*: 2017 IEEE Proceedings

1.1THz / 3.5 V transistor

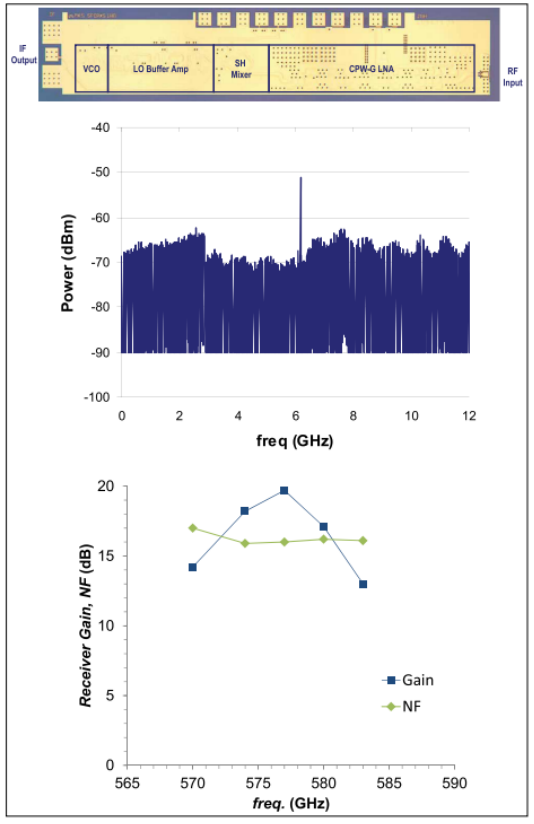




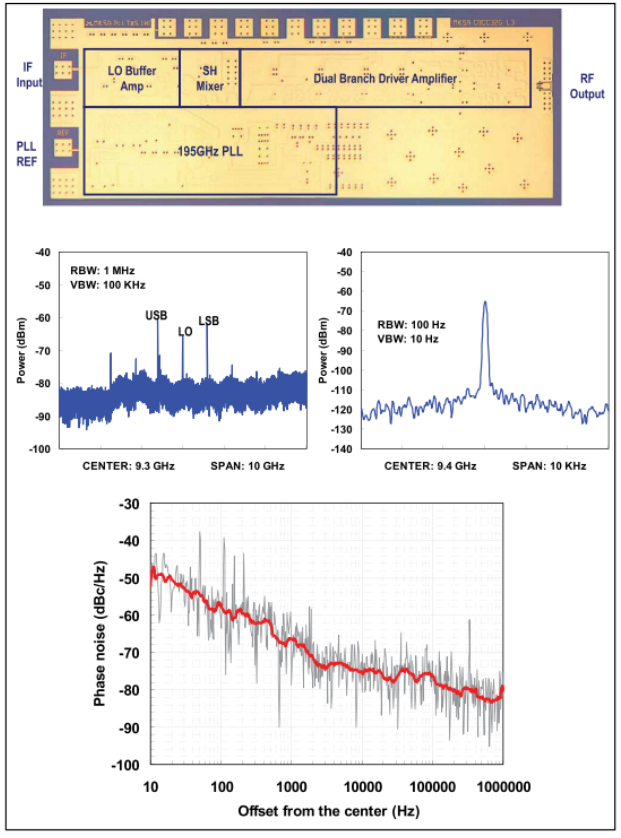
670GHz amplifier



570GHz receiver

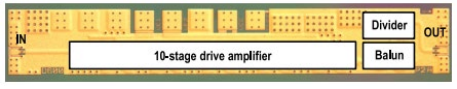


590GHz transmitter



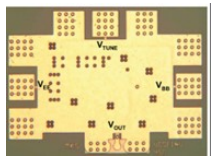
529GHz dynamic divider

Seo et al, 2015 IEICE Electronics Express



688GHz fundamental oscillator

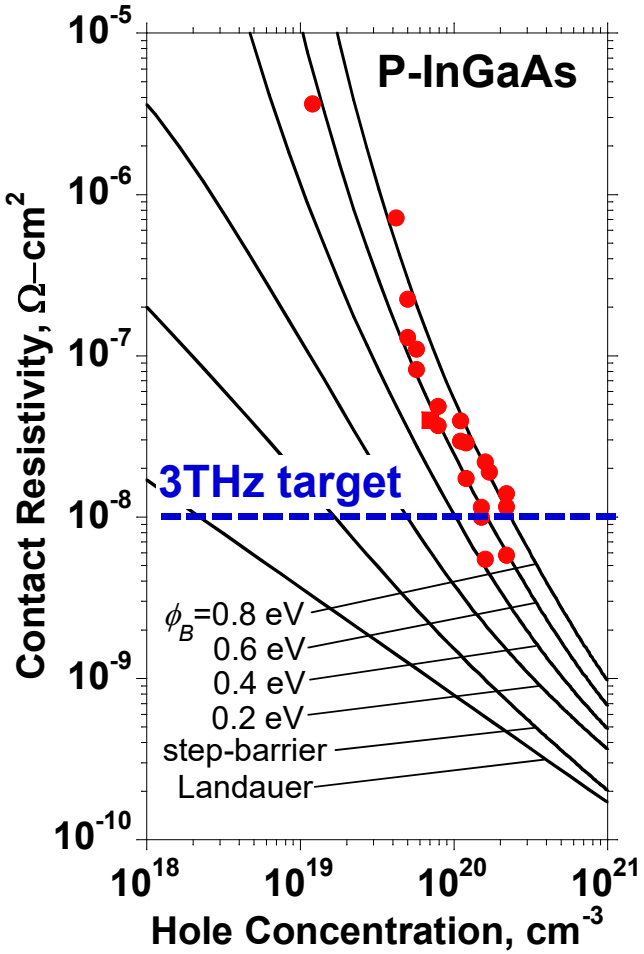
Urteaga et al, 2017 IEEE Proceedings



Towards a 2THz HBT: The key challenges

Obtaining good base contacts

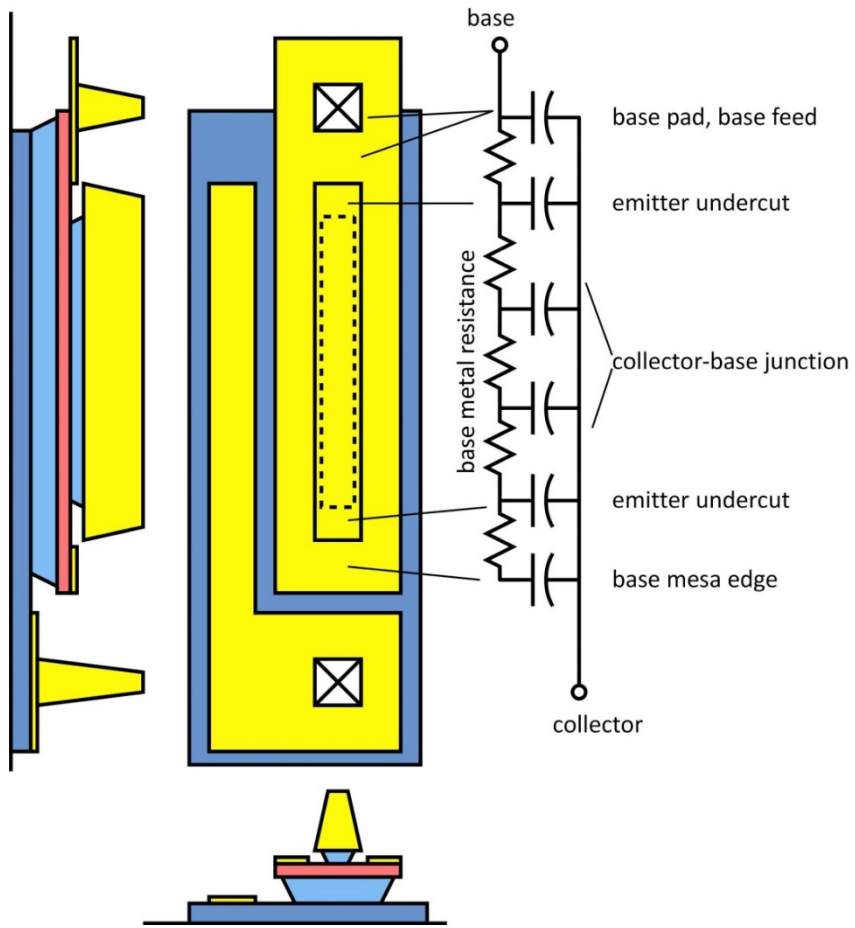
in HBT vs. in contact test structure
(emitter contacts are fine)



Baraskar *et al*, Journal of Applied Physics, 2013

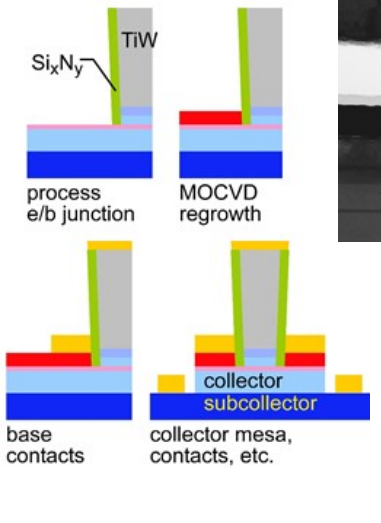
RC parasitics along finger length

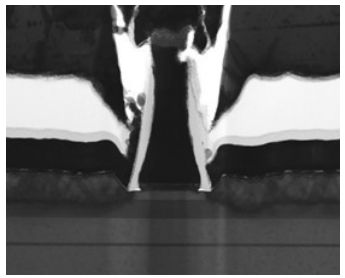
metal resistance, excess junction areas

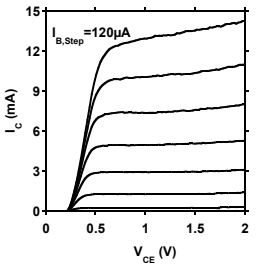


Solution ?

base regrowth

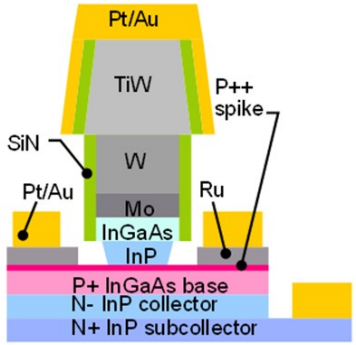






Solution ?

nm P++ base doping spike,
refractory base contact



Towards a 2 THz SiGe Bipolar Transistor

Similar scaling
InP: 3:1 higher collector velocity
SiGe: good contacts, buried oxides

Key distinction: Breakdown
InP has:
thicker collector at same f_τ,
wider collector bandgap

Key requirements:
low resistivity Ohmic contacts
note the high current densities

	InP	SiGe	
emitter			
junction width	64	**18**	nm
access resistivity	2	**0.6**	Ω–μm^2
base			
contact width	64	18	nm
contact resistivity	2.5	**0.7**	Ω–μm^2
collector			
thickness	53	15	nm
current density	36	**125**	mA/μm^2
breakdown	2.75	1.3?	V
f_τ	~1.0	~1.0	THz
f_{max}	~2.0	~2.0	THz

Assumes collector junction 3:1 wider than emitter.
Assumes SiGe contacts no wider than junctions: pessimistic

InP HBTs: applications

Complex ICs ✗

ADCs, DACs, fast serial links …

Many transistors, tight CMOS integration

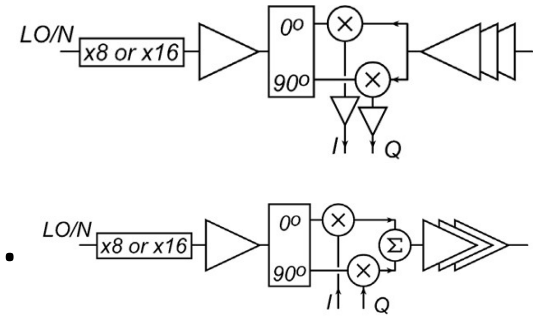
Small high-value instrument market: front-ends for 100GS/s ADCs…

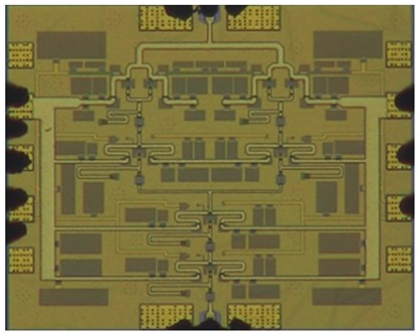
50-300GHz wireless front-ends ✓

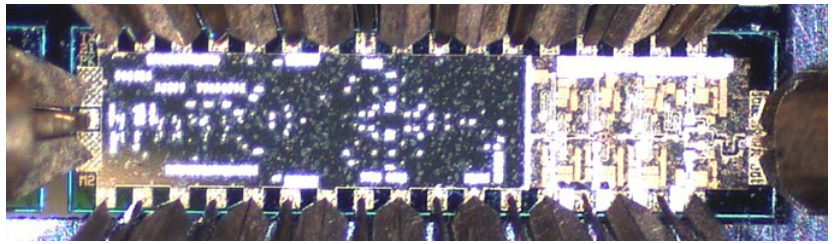
Application: record-efficiency PAs (30-300mW)

Application: low-power, high-performance RF front-ends.

Just like GaAs HBT in today's 4G cell phones

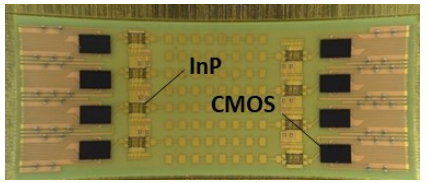






InP HBTs: research and development

InP/CMOS monolithic integration ✗
Instead, put close together in same RF package



Manufacturability and cost ✓
High yield for ~100-transistor RF front-end ICs.

Improved 50-300GHz PA efficiency ✓
More f_{max} at the same f_{τ}, and V_{br}: more gain→ higher PAE, class B, Doherty, etc.
Scaling to 128nm and 64nm nodes but with 256nm node collector thickness.

Integration density ✓
Denser interconnects: denser ICs for 200+GHz arrays, for PA efficiency

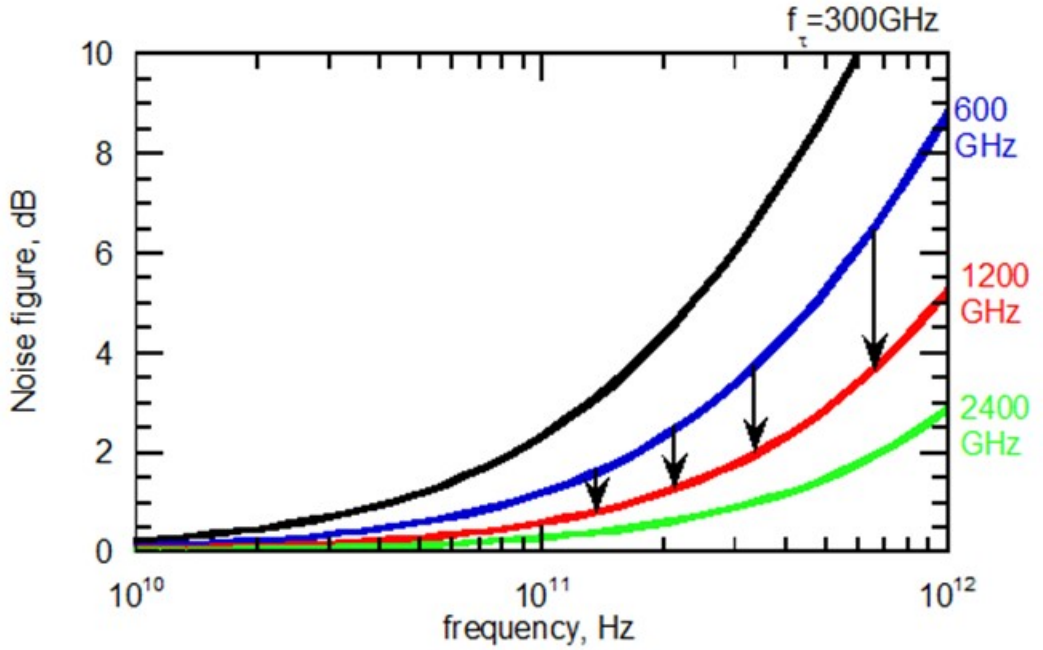
300-2000GHz wireless ✗
High atmospheric loss: just a few applications (space, short-range concealed weapons imaging radar)

FETs (HEMTs): key for low noise

Increased f_τ : less receiver noise

3dB less receiver noise: 2:1 less transmit power

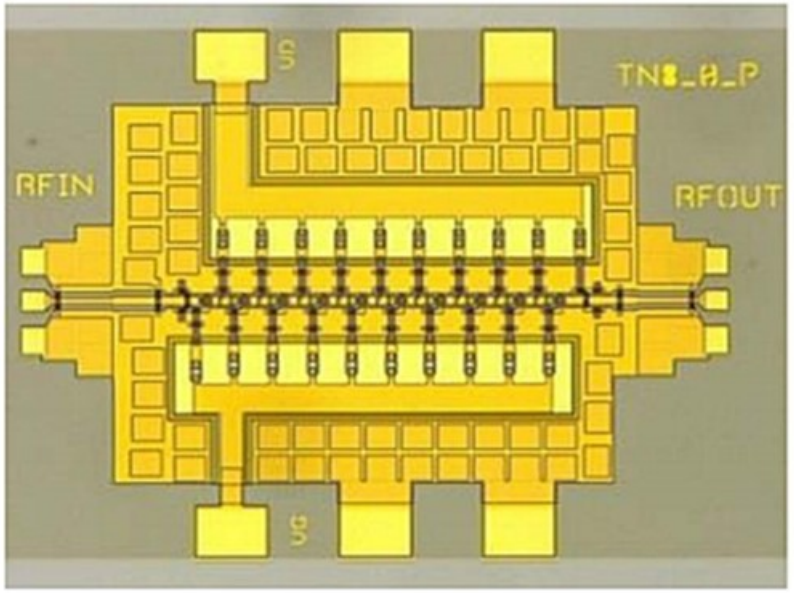
smaller PAs, less DC power



State of the art:

1.5 THz transistor f_{max}

1.0 THz amplifiers

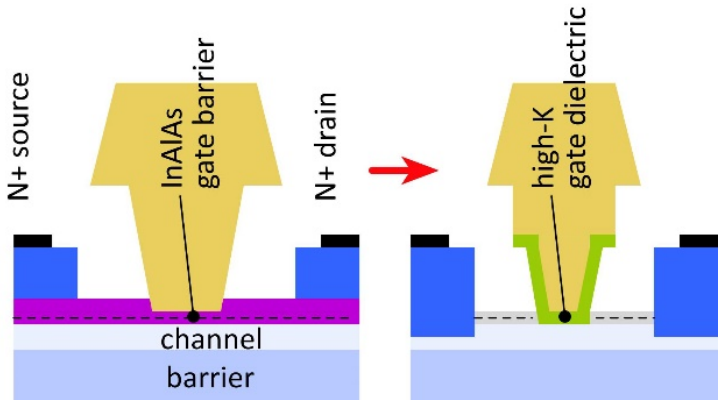


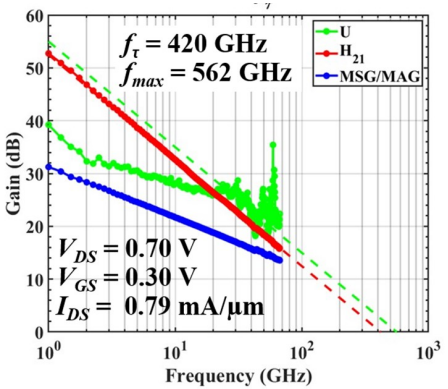
Xiaobing Mei, et al, IEEE EDL, April 2015 (Northrop-Grumman)

InP MOS-HEMTs: faster, more manufacturable ?

Scaling limit: gate insulator thickness
HEMT: InAlAs barrier: tunneling, thermionic leakage
solution: replace InAlAs with thin ZrO_2 dielectric

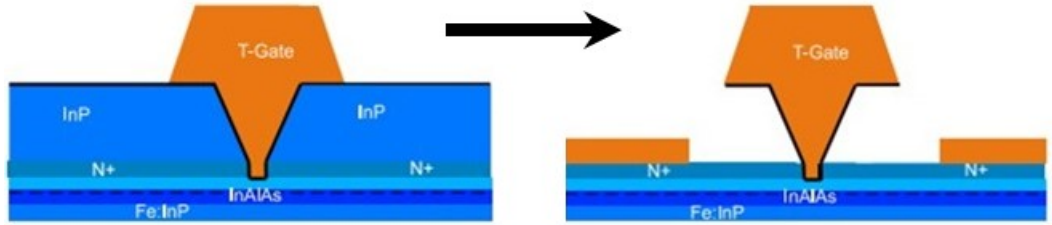
Scaling limit: source access resistance
HEMT: InAlAs barrier is under N+ source/drain
solution: regrowth, place N+ layer <u>on</u> InAs channel

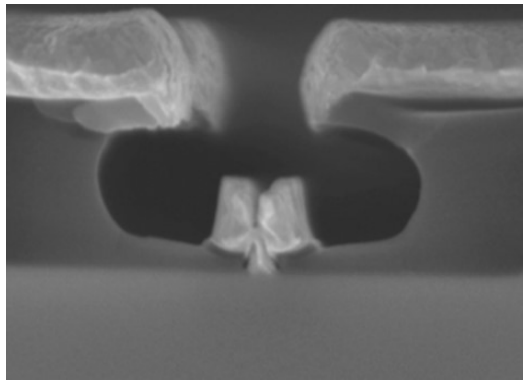


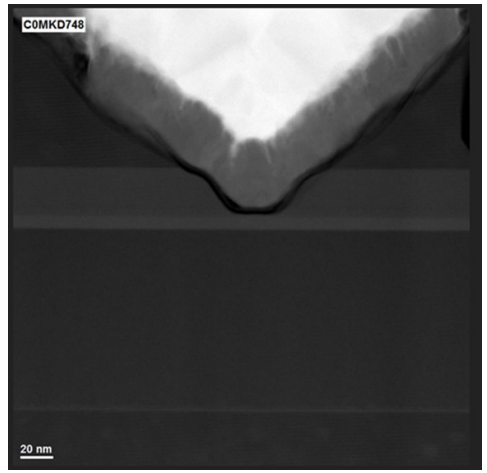


Markman et al, 2021 DRC

Sacrificial-layer gate process for manufacturability
Standard 20nm E-beam T-gate: limits IC yield
MOS-HEMT: can use sacrificial-layer process instead



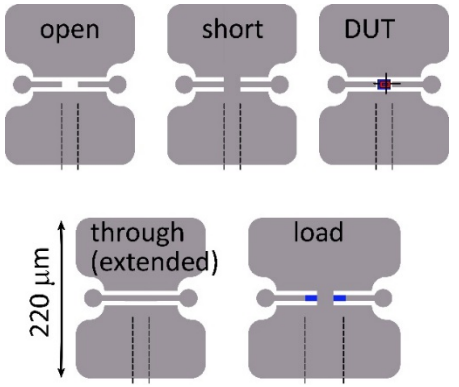


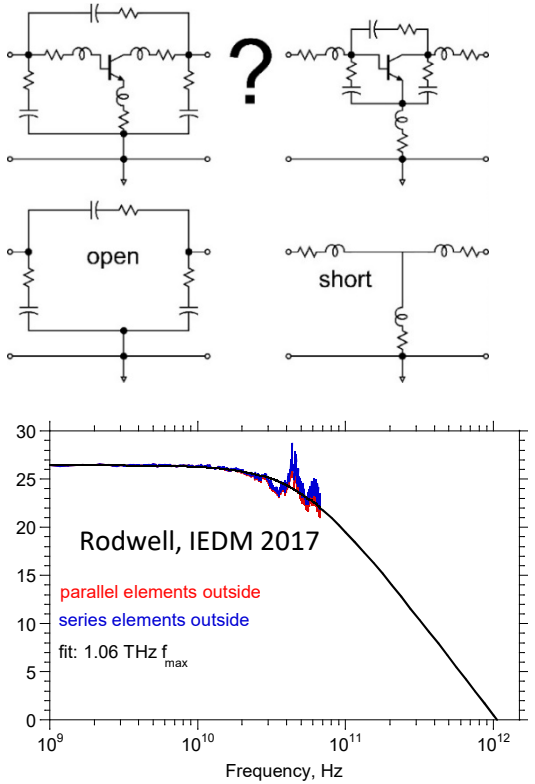


For Q&A discussion

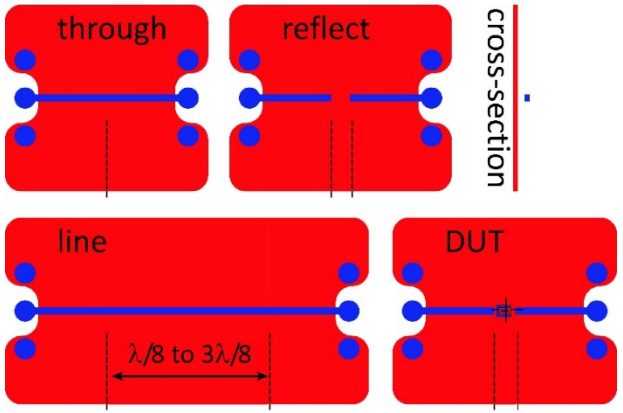
THz Transistor Measurements

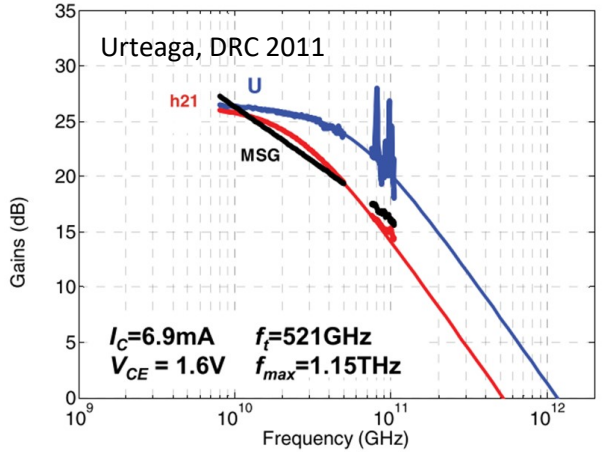
Simple pads:
Substrate coupling: need small pads, narrow CPW
Ambiguity in pad stripping order.
UCSB 130nm HBTs: order not important.
Add through & load to remove ambiguity





On-wafer through-reflect-line:
No ambiguity from pad stripping.
Calibration to line Zo
Still must avoid substrate mode coupling
CPW particularly vulnerable.
better: thin-film microstrip
or ~25 µm substrate with TSV's





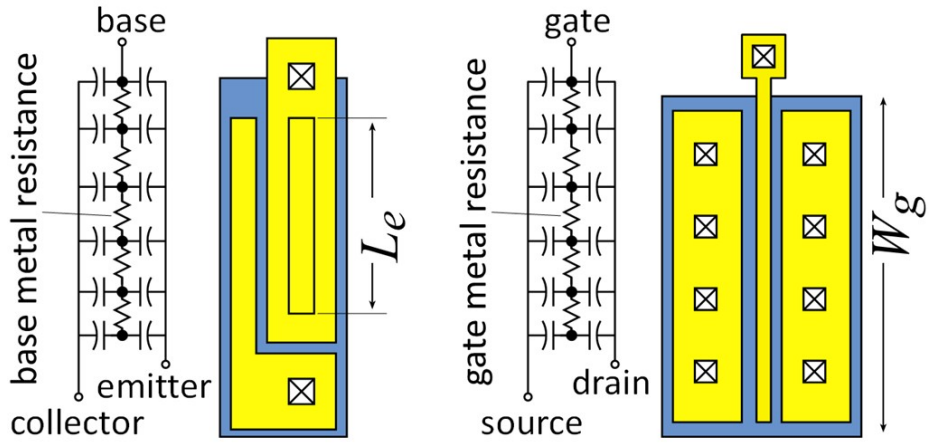
D. F. Williams, A. Young, M. Urteaga, "A Prescription for Sub-Millimeter-Wave Transistor Characterization," IEEE Transactions on Terahertz Science and Technology, July 2013

Current density, finger pitch limit cell output power

Electrode RC charging time $\propto$ (finger length)^2

Maximum finger length $\propto 1/\sqrt{\text{frequency}}$

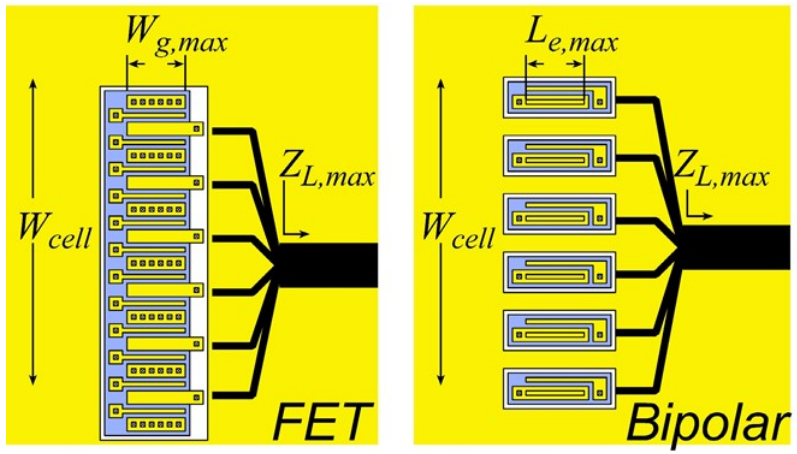
Current per finger $\propto 1/\sqrt{\text{frequency}}$



Maximum cell width $\propto 1/\text{frequency}$

Maximum number fingers $\propto 1/\text{frequency}$

Maximum current per cell $\propto 1/\text{frequency}^{3/2}$



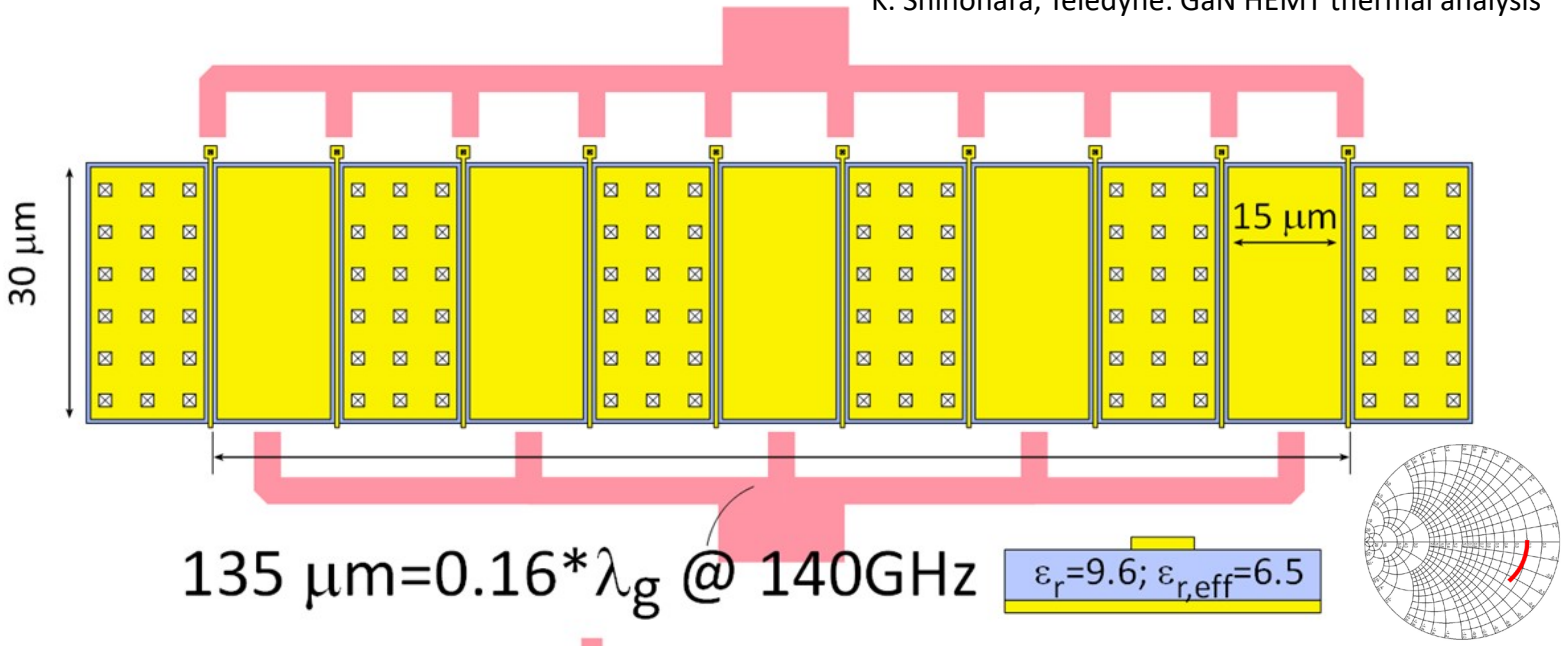
Maximum RF power per cell $\propto$ (maximum load resistance)$\cdot$(maximum current)$^2 \propto 1/$(frequency)^3

Compare to Johnson F.O.M.: maximum power per cell $\propto$ (maximum voltage)$^2/$(minimum load resistance) $\propto 1/$(frequency)^2

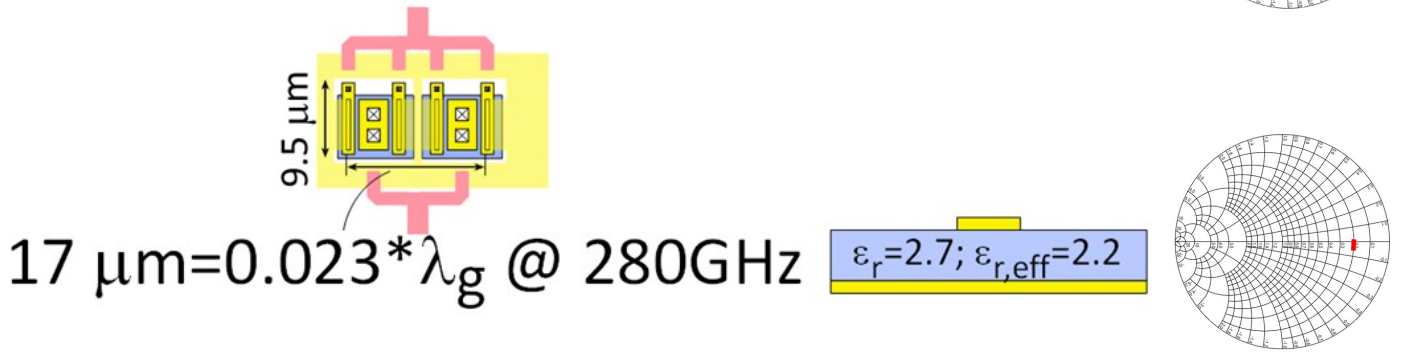
Current density, finger pitch limit cell output power

K. Shinohara, Teledyne: GaN HEMT thermal analysis

50Ω GaN PA cell @ 140GHz (1.6W)
25V swing, 1.67mA/μm,
gates: 30 μm width, 15 μm pitch



50Ω InP HBT PA cell @ 280GHz (40mW)
4V swing, 3.3mA/μm,
emitters: 6 μm length, 6 μm pitch



High V_{br}, low I_{max} ? Device sized to drive 50Ω might approach $\lambda_g/4$ width.
Small finger pitch is critical; limited by thermal design