Challenges in Architecture & Synthesis for 3D ICs

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Dr. Rob Aitken

Rob Aitken is a Distinguished Architect and leads the Office of Technology Strategy at Synopsys, where he is looking into future technical opportunities for the company, including AI/ML, security, and next generation design methodology including multi-die systems. Dr. Aitken is an IEEE Fellow.

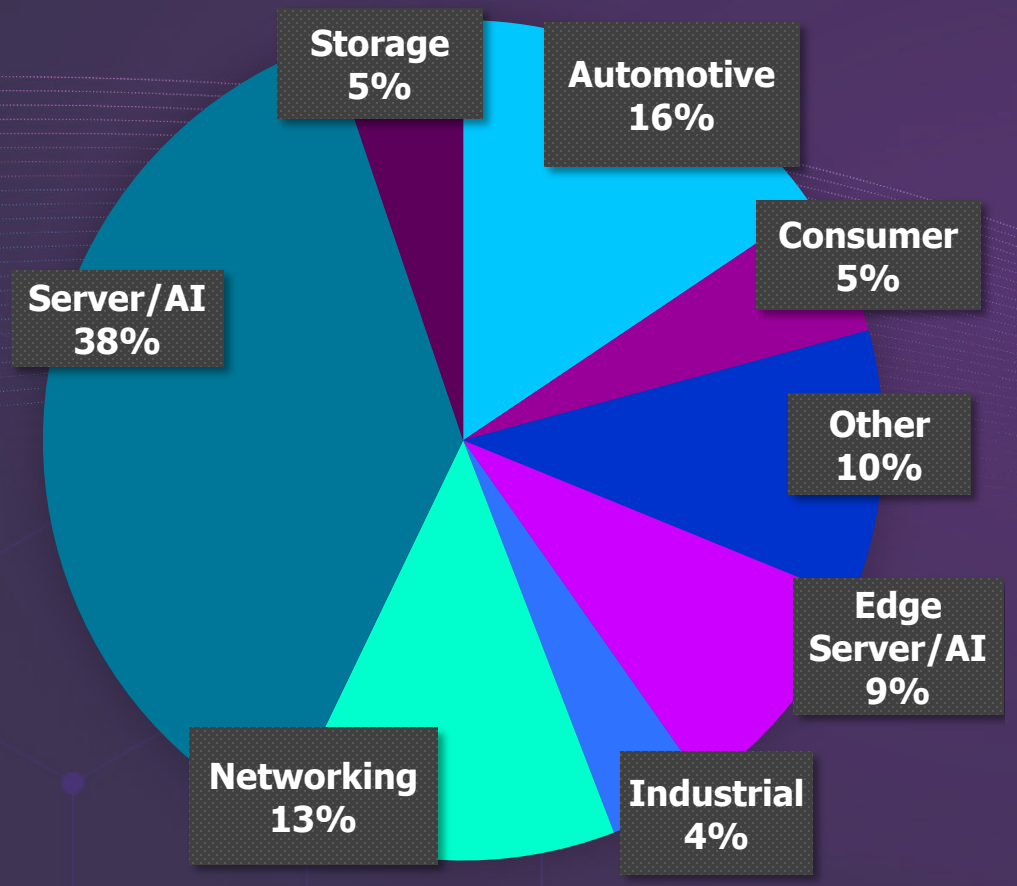
Vision

Synopsys helps our customers innovate from silicon to software so they can bring amazing new products to life.

Mission

Synopsys is the world's leading EDA and services company, #1 in Interface, foundation & physical IP and a global leader in application security.

Multi-Die Systems are Here



Synopsys Tracking >100 Multi-Die System Designs

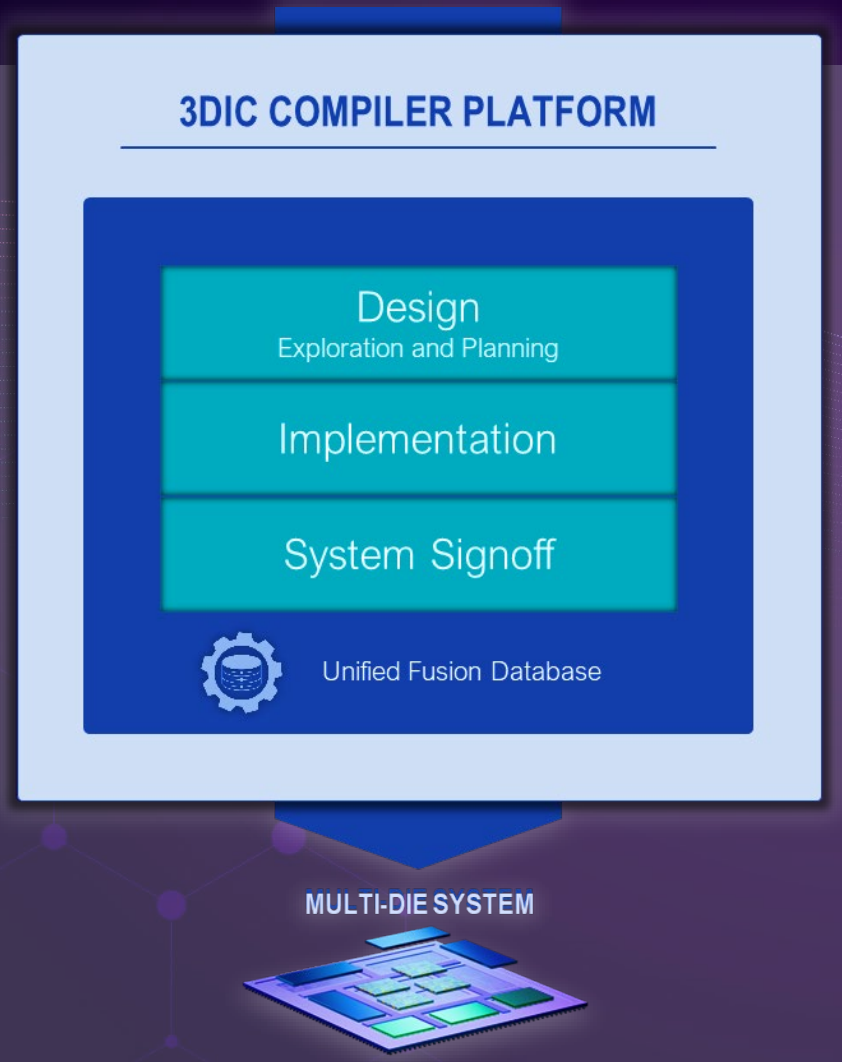
- Servers / AI dominate
- NICs, Switches common use case
- Automotive, smartphones ramping

Can 3D bring back Moore?

41%

- Classic Moore scale factor is √2 or a 41% improvement
- Two die stack reduces inter-cell distance by √2
- Shorter wires allow faster communication at lower power
- But devices don’t change…
- **Achieving Moore style gains requires new architectures and new approaches**

Multi-Die Systems are Here



- If you want to build a multi-die system today, there are EDA solutions that you can use
- Future EDA innovations will enable new architectures and make designers even more productive

Multi-Die Systems are Here

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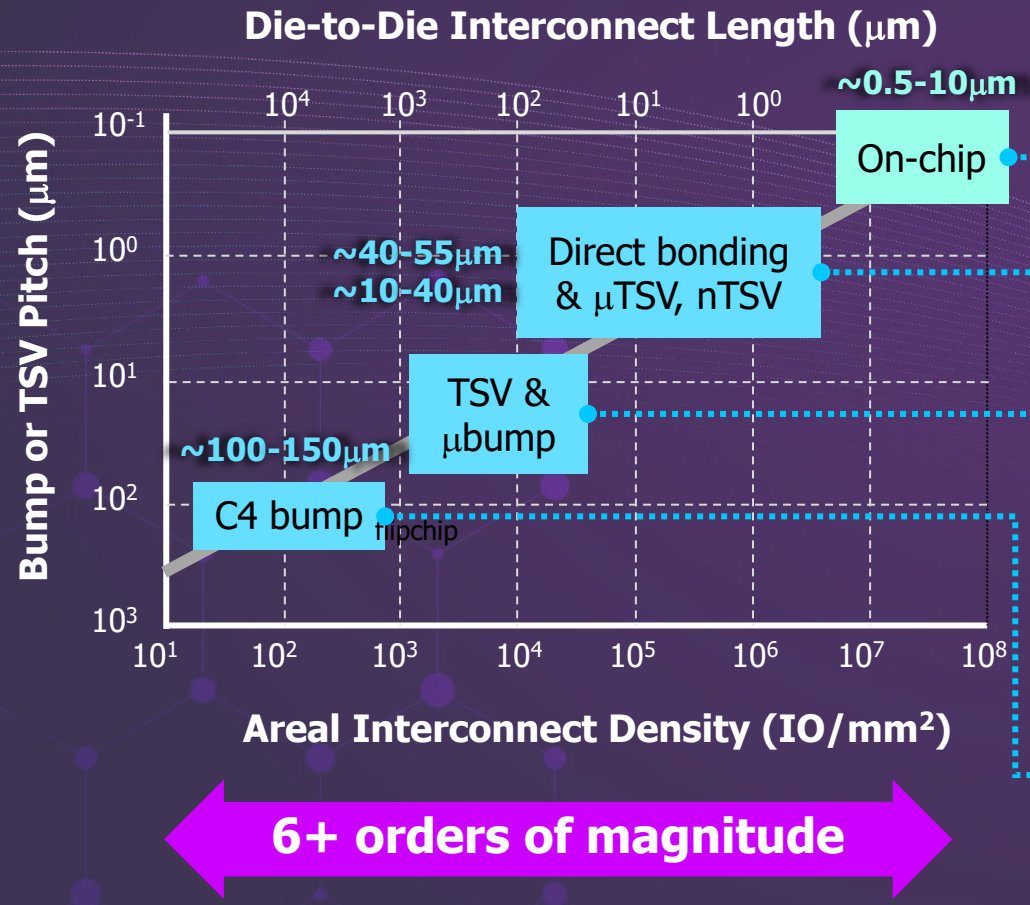
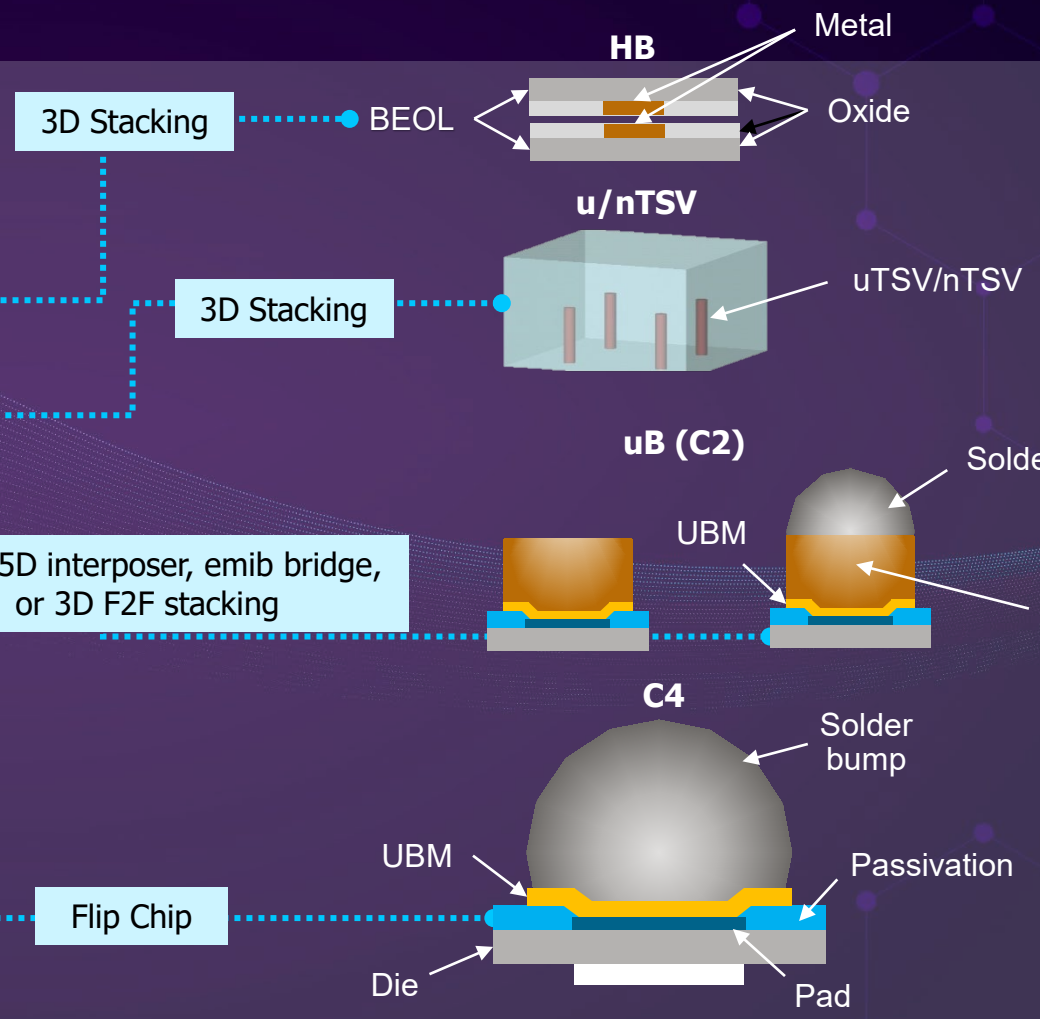
Multi-scale Interconnect Options





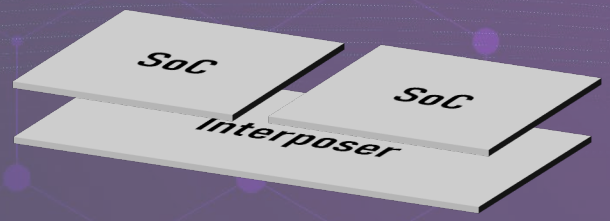
Multi-Die System Architecture

Technology Progression for Architecture, Synthesis, Place & Route…

OBJECTIVE: IMPROVE SWAP, REDUCE REQUIRED GUARDBANDS

Before

Stack of individual 2D dies

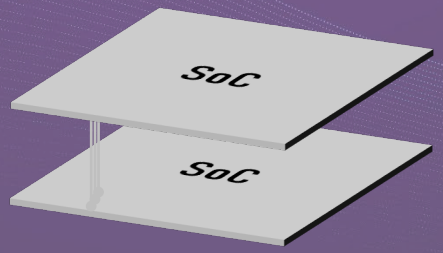


Planned in 2.5D or 3D
Implemented as individual 2D die
Function-level partitioning
Source-synchronous D2D communication

Some performance improvement

Now

Stack of Co-Designed dies

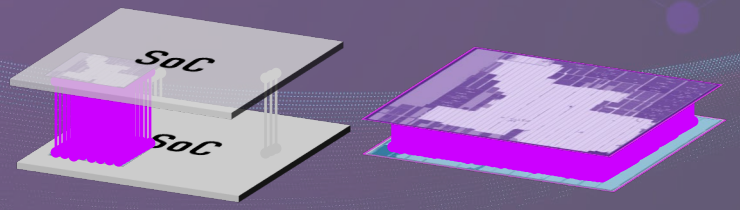


Planned in 3D
Implemented as multiple 2D dies
Coarse-grained partitioning
Synchronous D2D communication

Promising gains reported

Next

Stack of Co-Optimized "Multi-tier" dies



Planned and implemented in 3D
Multi-tier, optimized as one
Fine-grained partitioning
Synchronous D2D communication

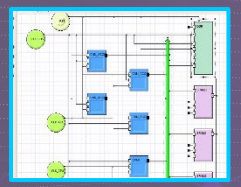
Where the 41% could be found

The Path to True 3D

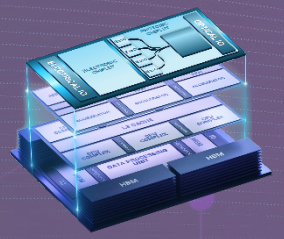
Crawl

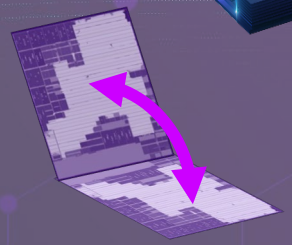
Design for stacked die

HW Partitioning



Integration



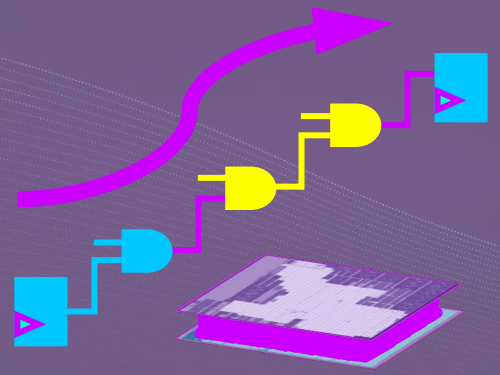


Allocate blocks between die
Optimize metal, thermal etc.
Example: stacked/folded 2D design

Some performance improvement

Walk

Break physical boundary



Full dies-stack optimization

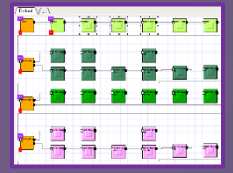
Logical hierarchy independent of physical Individual design block spans multiple die; includes clocking and power delivery

Promising gains reported

Run

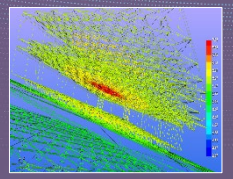
Native 3D system design flow

Application Workload



Bottleneck Analysis

Resilience



Design-for-...

Rearchitect full system across multi-tier stack workload/memory/power; optimized co-design-for-test/yield/resilience/heat…

Where the 41% could be found

THANK YOU