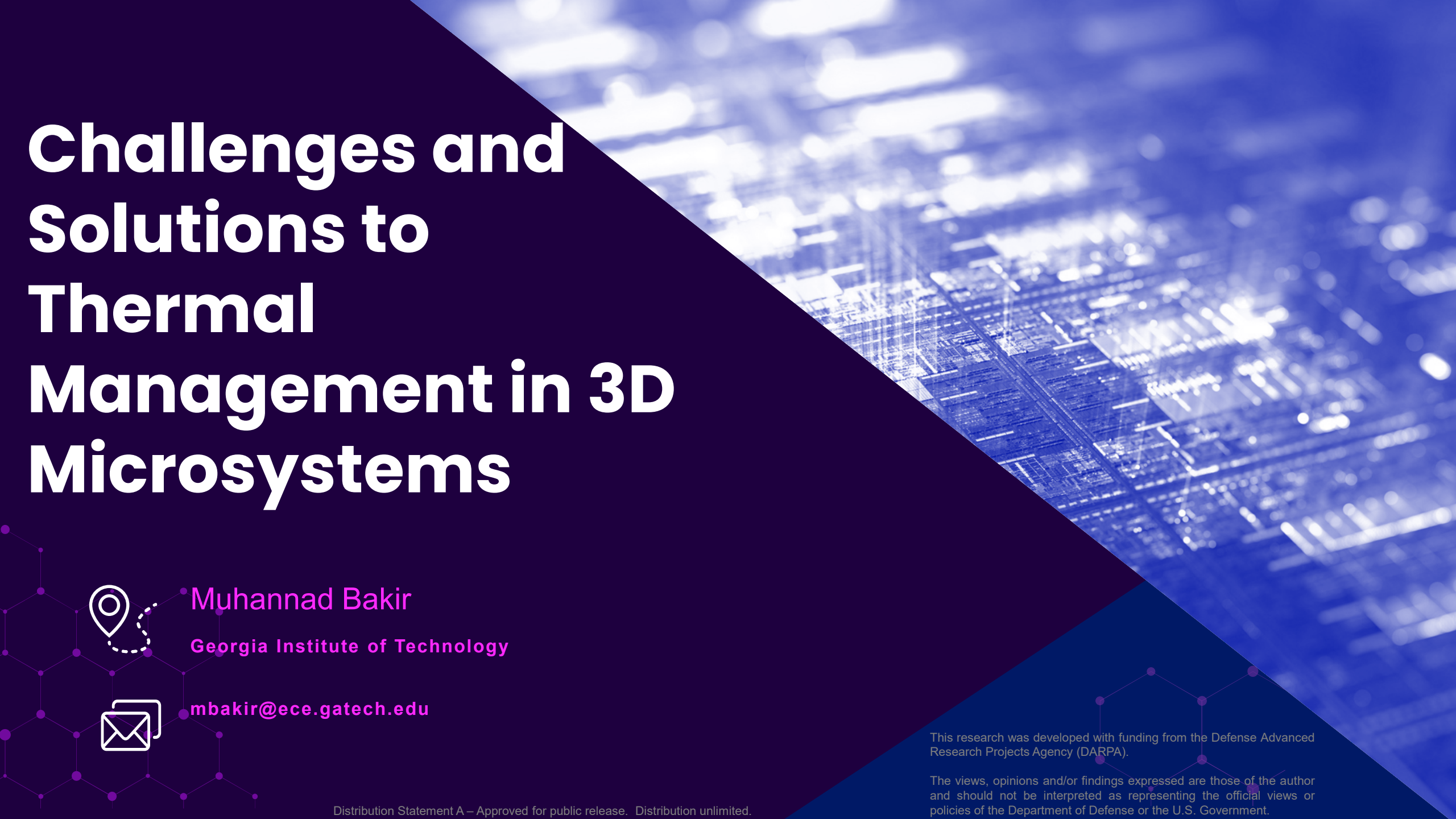
Challenges and Solutions to Thermal Management in 3D Microsystems



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Thermal Challenges in 3DHI

Forced air cooling

Tier 5
Tier 4
Tier 3
Tier 2
Tier 1

*T_{max}: >400 °C

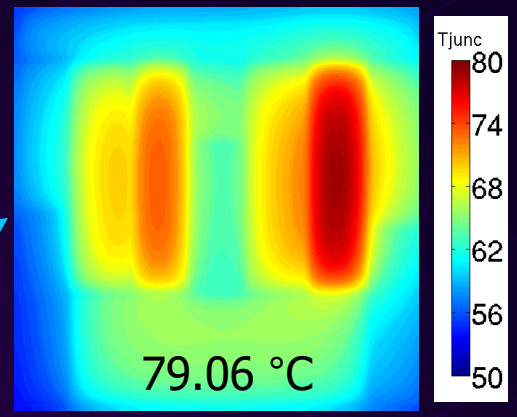
Liquid Cooling
Tier 5
Tier 4
Tier 3
Tier 2
Tier 1

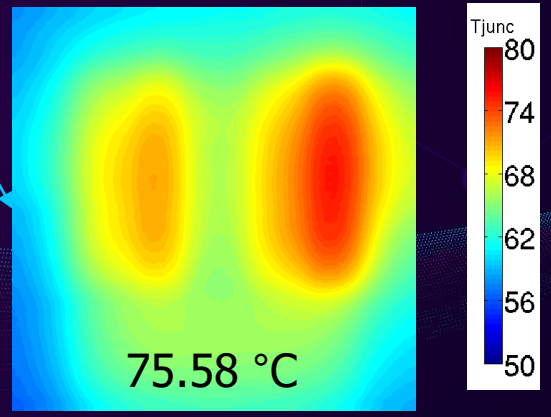
215 °C

→Limited cooling

High-power tier →
Low-power tier →

Tier 5
Tier 4
Tier 3
Tier 2
Tier 1





→Thermal Cross-talk

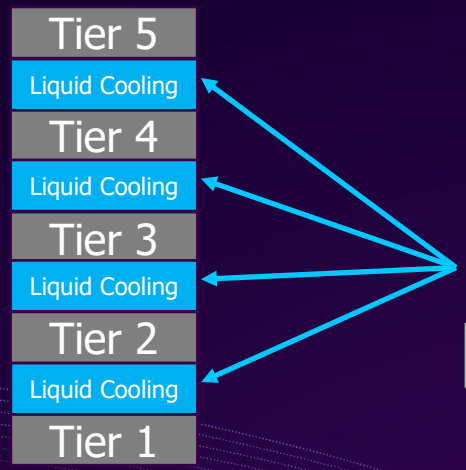
Key thermal challenges are:

- Inability to extract heat from 3DHI, limiting power, performance, and functionality
- Thermal cross-talk in 3DHI, impacting lower-power and temperature sensitive devices
- Typical form factor for cooling is large

*Assuming 300 W/cm^2 per tier

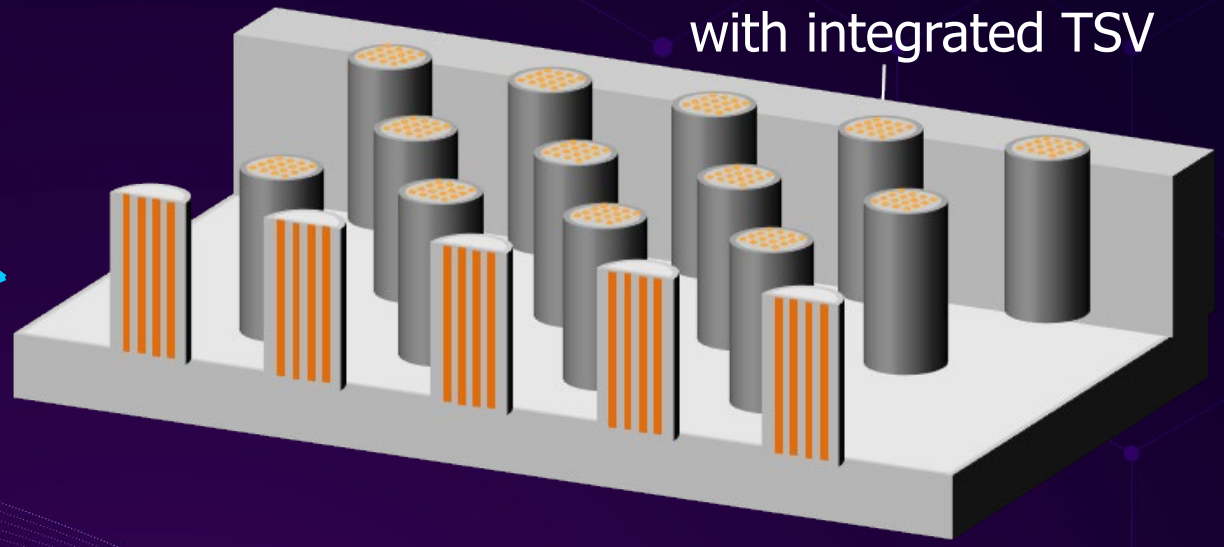
Within 3D Stack Microfluidic Cooling

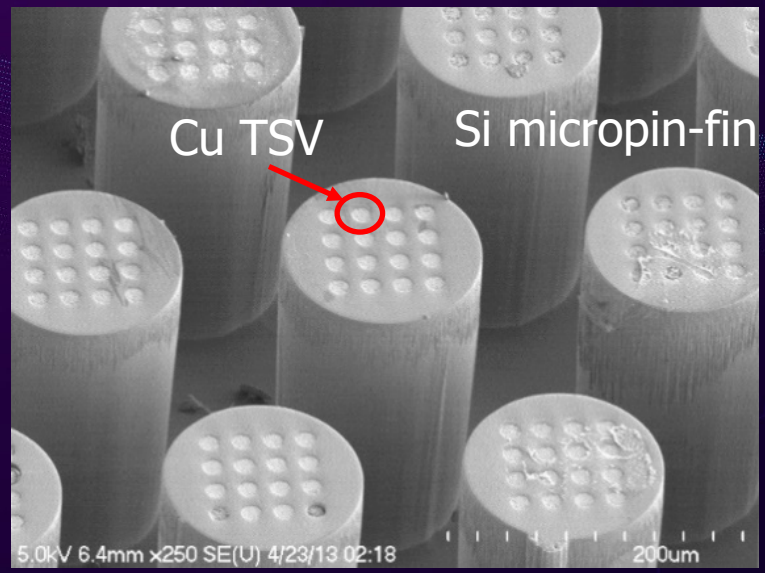
Forced air cooling



*T_{max}: >500 °C 215 °C 48 °C

Silicon micropin-fin heat sink with integrated TSV



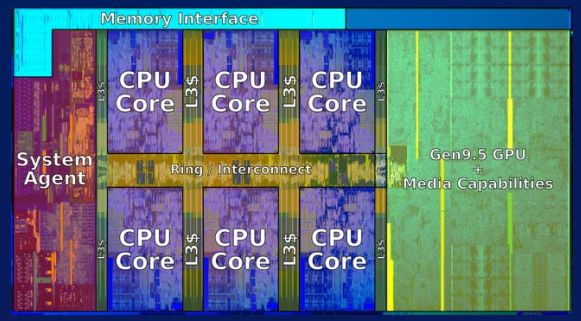


Electrical performance

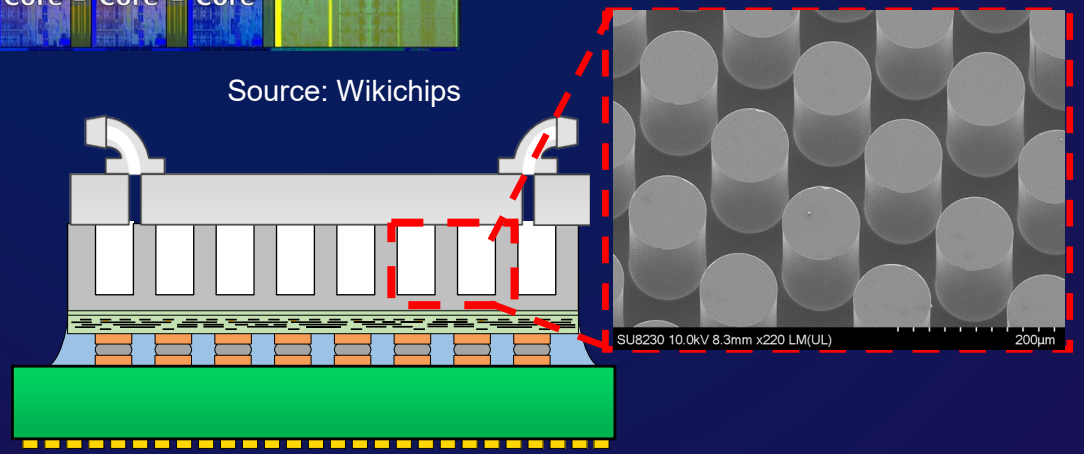
Thermal performance

Manufacturability, Integration, Reliability

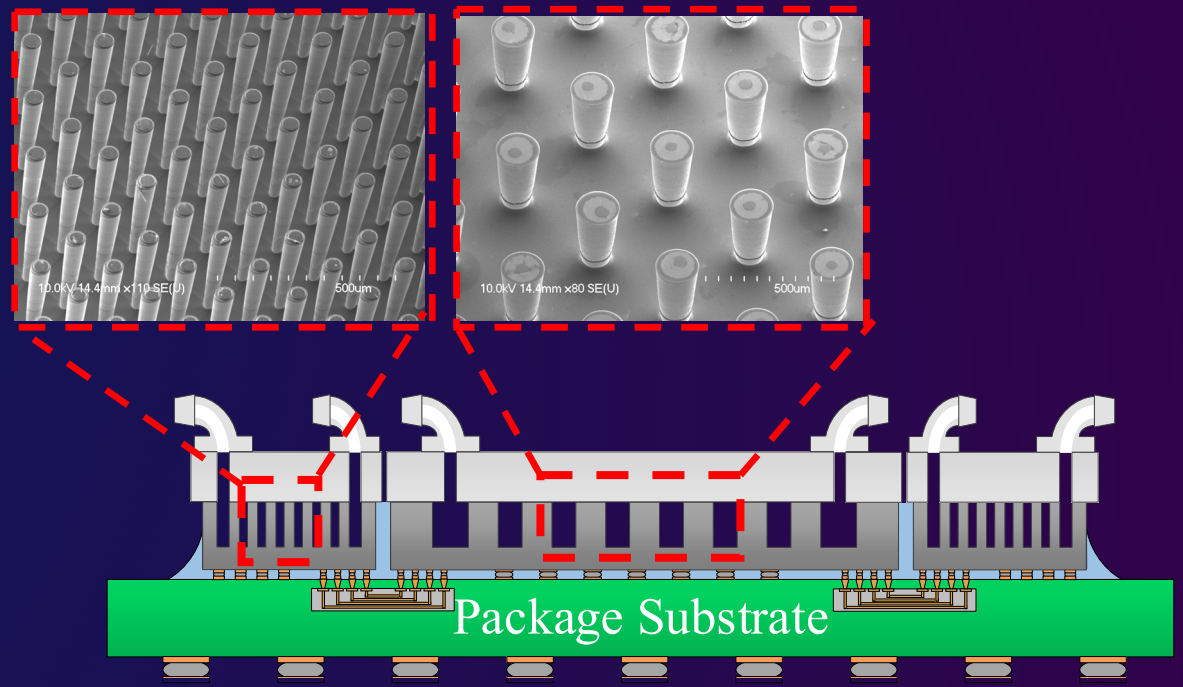
Microfluidic Cooling Integration and Benchmarking



Source: Wikichips



Etched micropin-fins on Intel i7-8700K Die



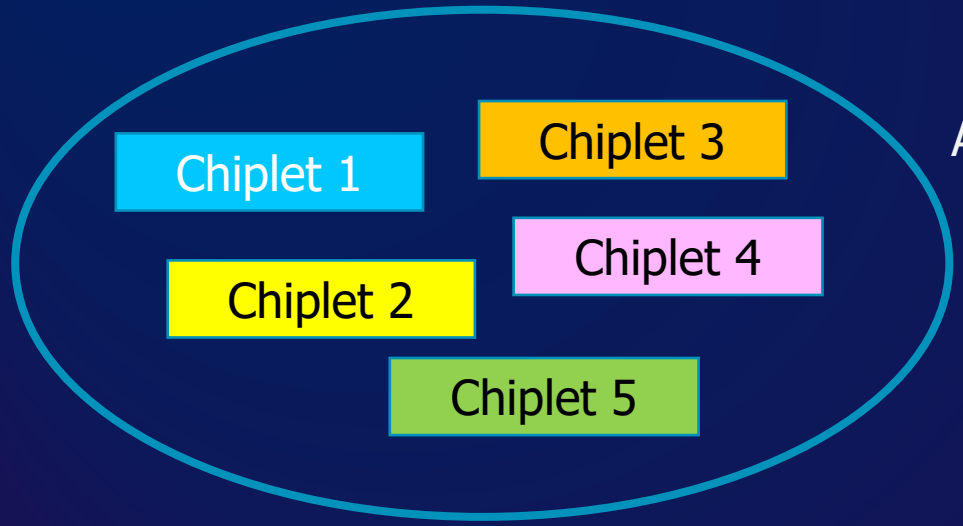
Intel Stratix 10 2.5D FPGA (4 transceivers)

- Significantly smaller form factor (microscale)
- Relative to cold-plate, estimated ~40% lower thermal resistance

- Optimized microscale heat sink for power density
- >10x reduction in thermal-crosstalk relative to air-cooled heat sink

Using Chiplets to Build 'Package Functions'

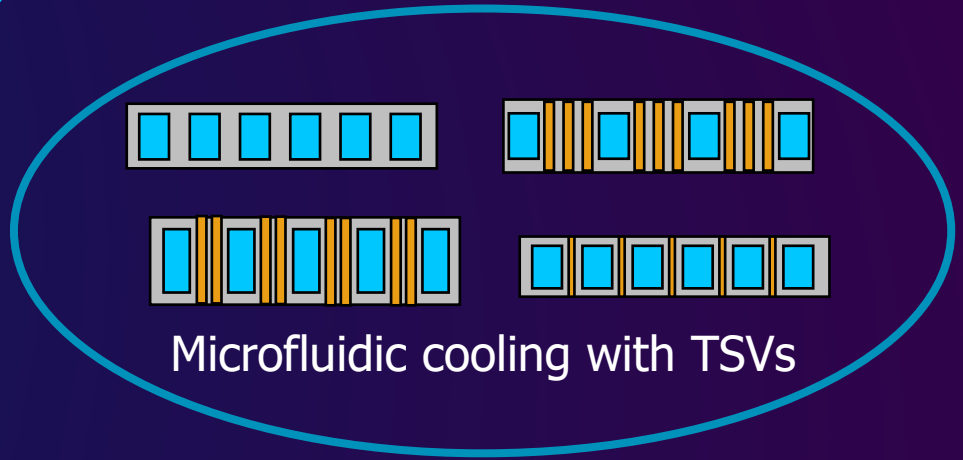
Chiplets: digital, analog, IO, power, mm-wave, photonic, etc



Active chiplets

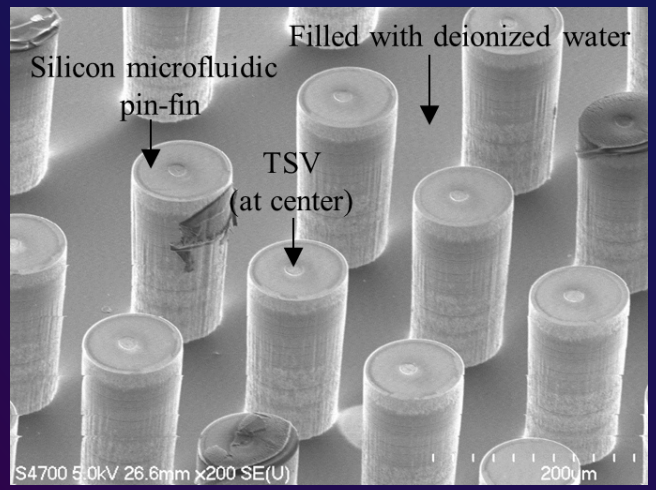
Passive chiplets

Cooling Chiplets

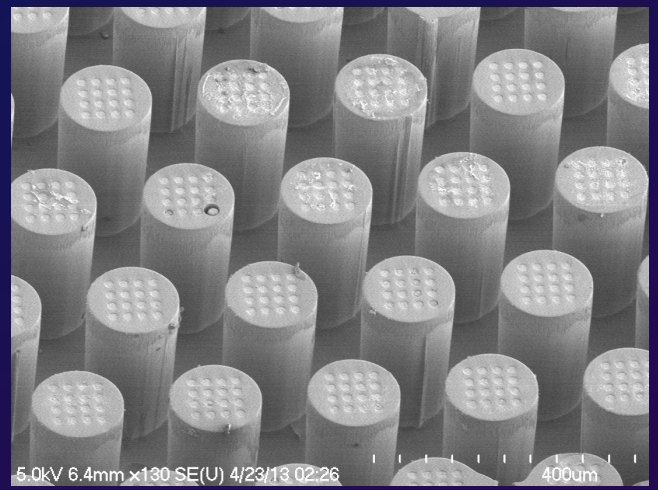


Microfluidic cooling with TSVs

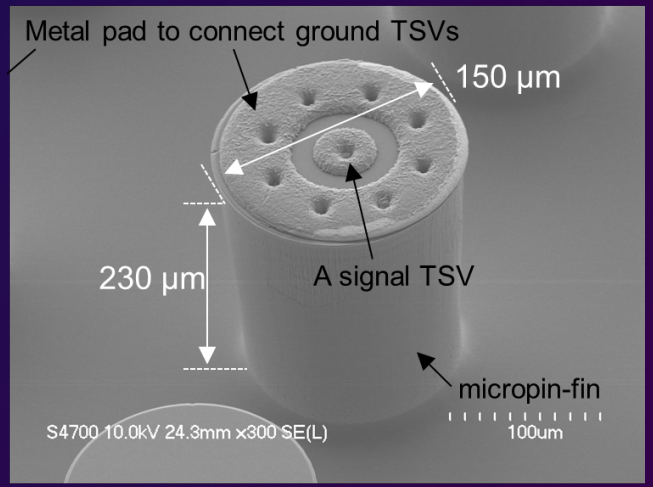
Single TSV in dense heat sink



TSV bundle in coarse heat sink

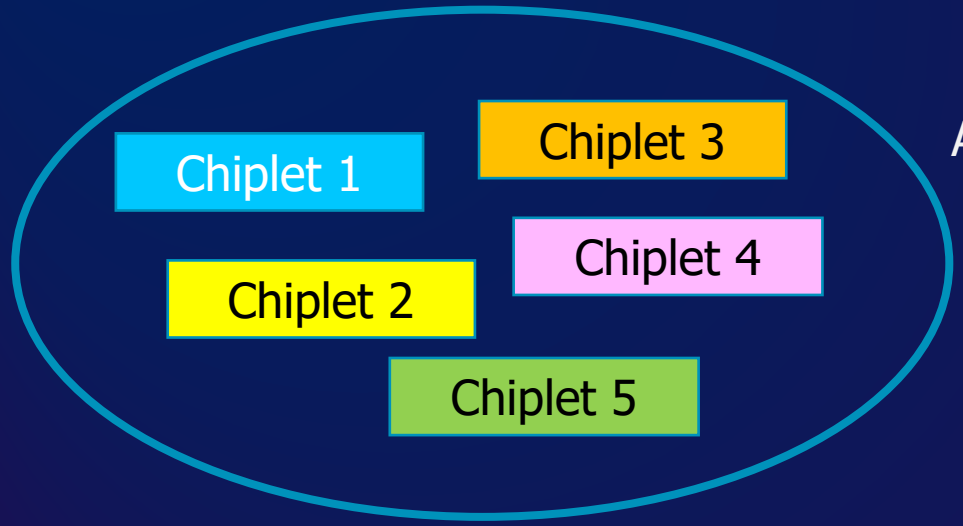


Coax TSV in microfluidic heat sink



Using Chiplets to Build 'Package Functions'

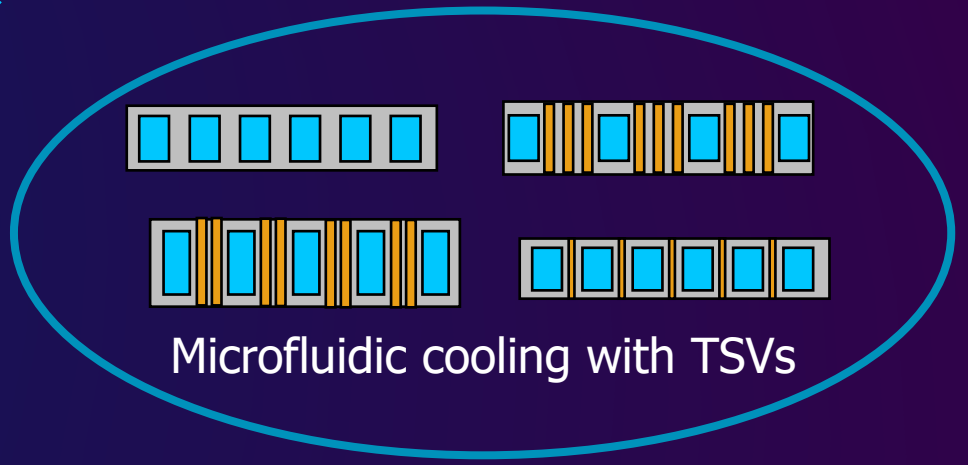
Chiplets: digital, analog, IO, power, mm-wave, photonic, etc



Active chiplets

Passive chiplets

Cooling Chiplets



Using Chiplets to Build 'Package Functions'

Chiplets: digital, analog, IO, power, mm-wave, photonic, etc

Active chiplets

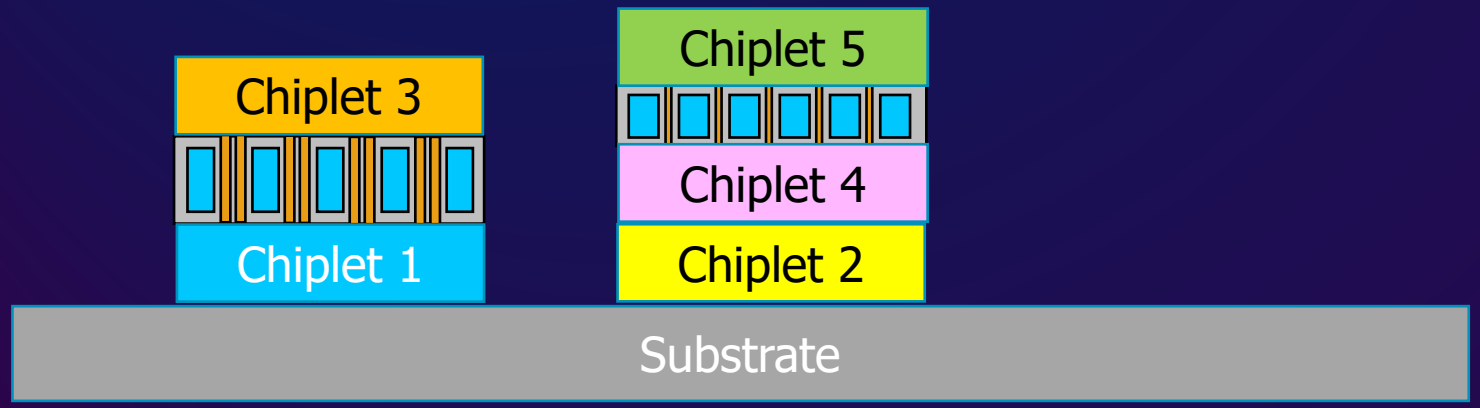
Passive chiplets

Cooling Chiplets

Microfluidic cooling with TSVs

Fiber Align & Attach chiplets

mm-wave Stitch chiplets



THANK YOU