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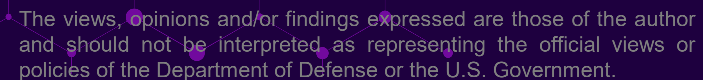
Results and Upcoming Challenges in Physical Design of 3D-ICs



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Vinay Patwardhan

Product Management Group Director, Cadence Design System

Vision

Design Automation for implementation of complex multi-die designs.

Mission

Develop algorithms and methodologies for system technology co-optimization for multi-tier 3D-ICs, to enable next wave of technology innovation.

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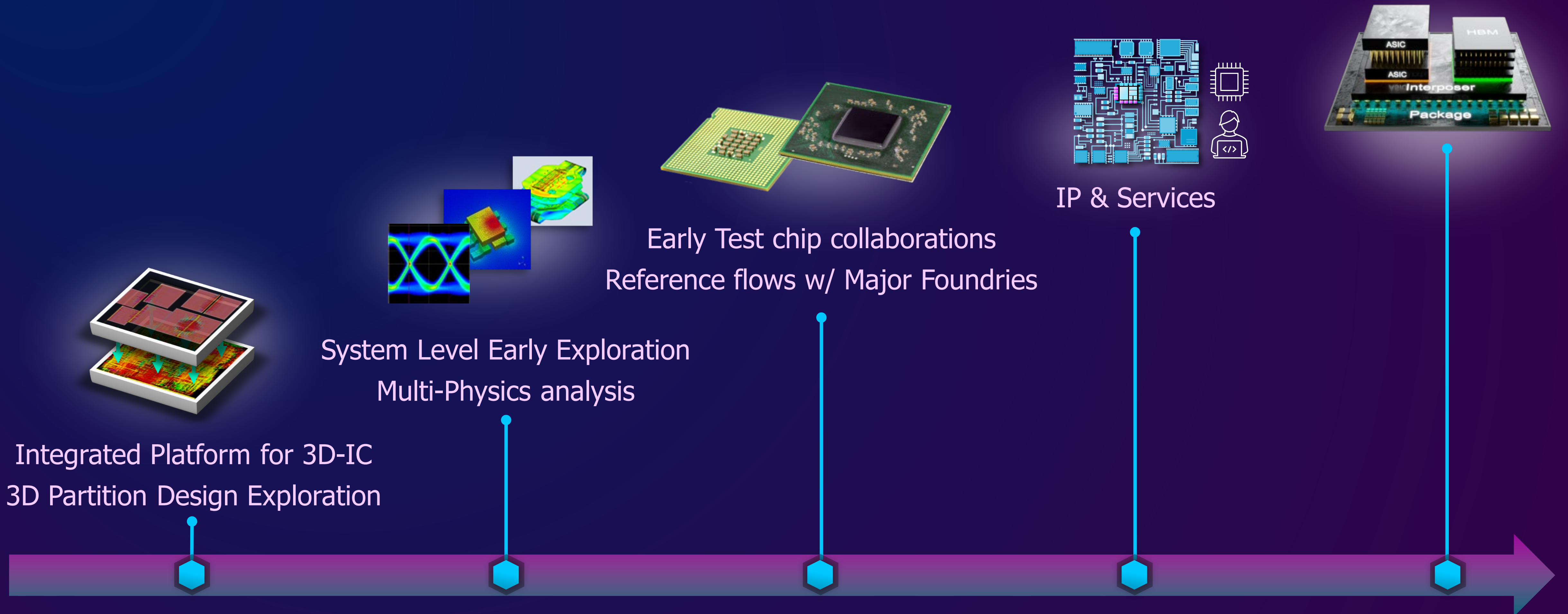
Creating 3D-ICs with Cadence Technology



Innovation in Multi-Die design with leading customers and industry partners

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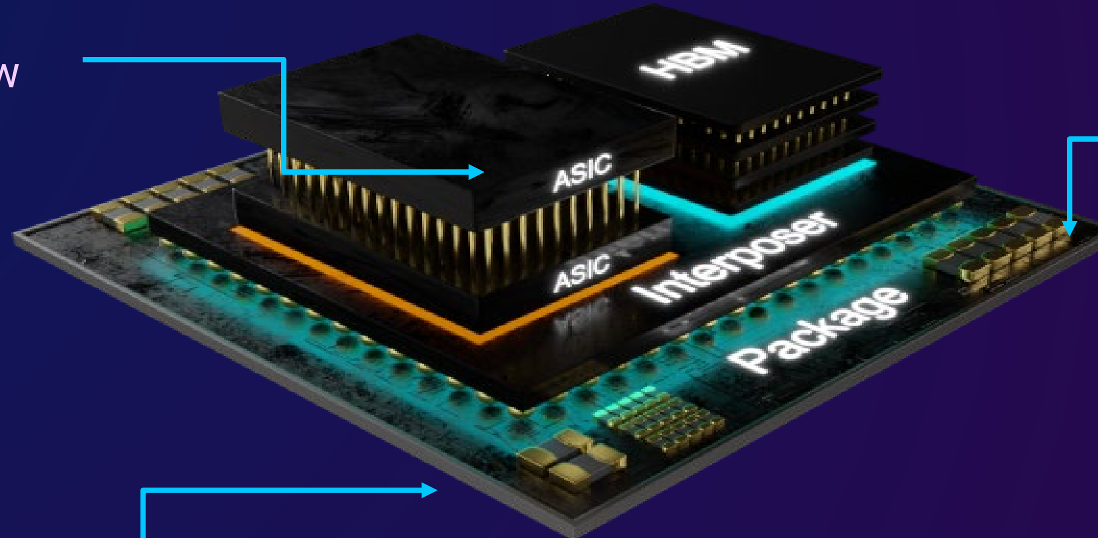
Heterogeneous Integration Physical Design Complexity

Chip stacking (Bumpless)
Homogenous or Heterogeneous
Bottom-Up flow or Top-Down Flow

Interposer : Silicon or Organic
Needs Offchip Design
and Analysis
Interface with ASIC and Package



Package Implementation
Package Routing
Package level flows

Connection Type	Solder Ball	C4 Bump	Micro Bump	Hybrid Bond
Typical Pitch of Connection	>1000um	250um	50um	<10um
# of Connection (in $1mm^2$ area)	<1	16	400	>10000

EDA tools need to model and implement

Physical and Electrical object Properties

Die Interconnections

Electro thermal & mechanical effects

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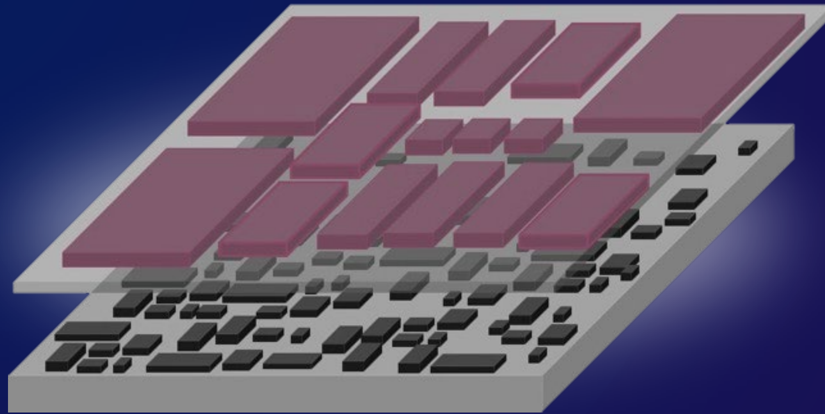
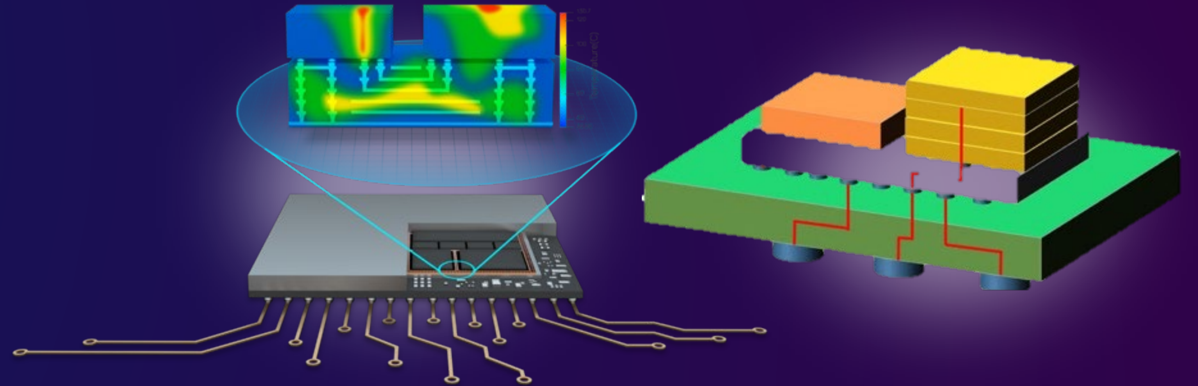
3D-ICs Physical Design **Challenges (EDA perspective)**





3D Chip Stacking

- Design size capacity – Multiple Dies optimization
- Support for chiplets across multiple nodes
- Concurrent editing of multiple devices

- On-the-fly die splitting and re-partitioning in Z direction
- Timing driven cross-chip(let) routing
- Co-design with packaging

3D Analysis and Sign-Off

- STA with automated corner reduction
- SystemLVS with rule-deck-free methodology
- Multi-die EMIR

- Early-stage and signoff level thermal analysis
- Stress and CMP planarity checks
- New 3D-IC test standards

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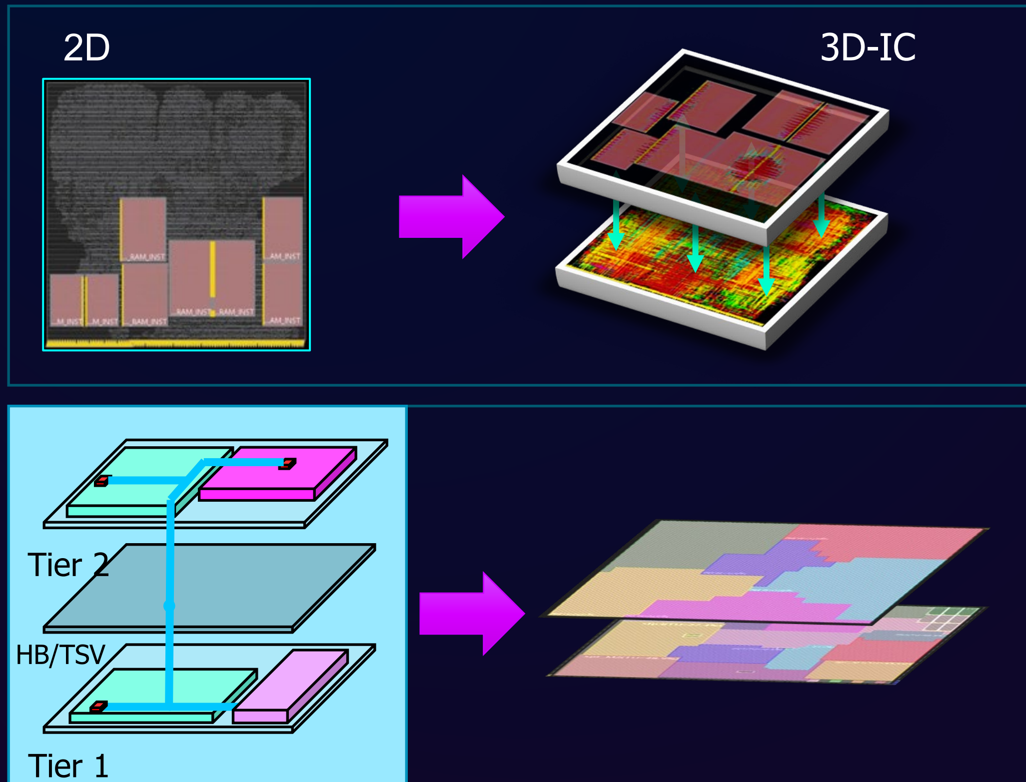
Power Performance Area Gains Achieved by 3D Partitioning

Homogeneous and heterogenous die stacks



Designs (Descriptor)	Results
Wearable	20% area savings, 20% wirelength savings
CPU	30% power reduction 85% area scaling
Mobile Core	21% wirelength , 43% area improvement,
Multi-core Processor	38% better performance , 13% power savings
NPU	26.7% total PPA gain

Fine Grain Auto Partitioning based on multi-objective 3D placement
3D-IC configuration shows improvement in performance and saves power

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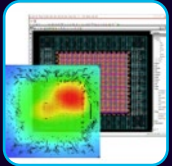
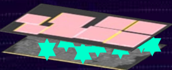
Cadence Strategy to Further Accelerate 3D-IC Physical Design



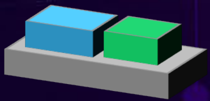
Unified platform-based flow with system level analysis

- **Integrity™ 3D-IC Platform**
- High-performance analysis



Fine Grain die partitioning

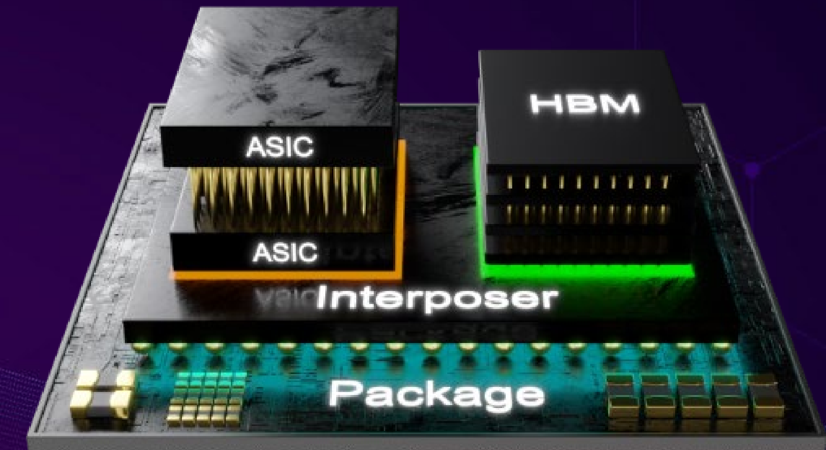
- Early-stage thermal/power analysis
- Seamless die-to-die signal integrity



Bottleneck reduction thru co-optimization

- High-capacity Auto-routing
- Cross die bump optimization

AI/ML



3D-IC Schedule Acceleration

Time

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THANK YOU