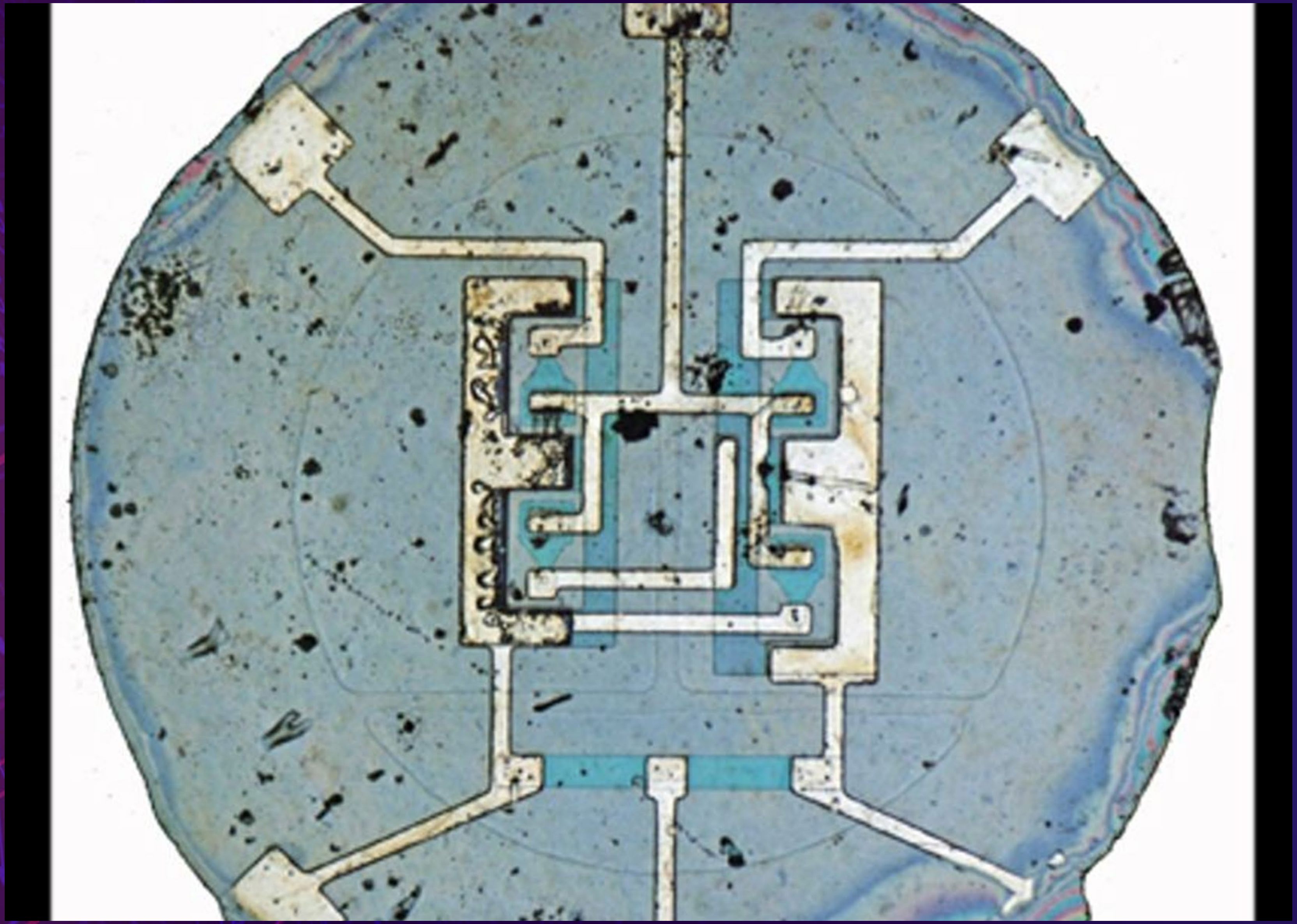
DARPA Strategy

Mark Rosker

MTO Director

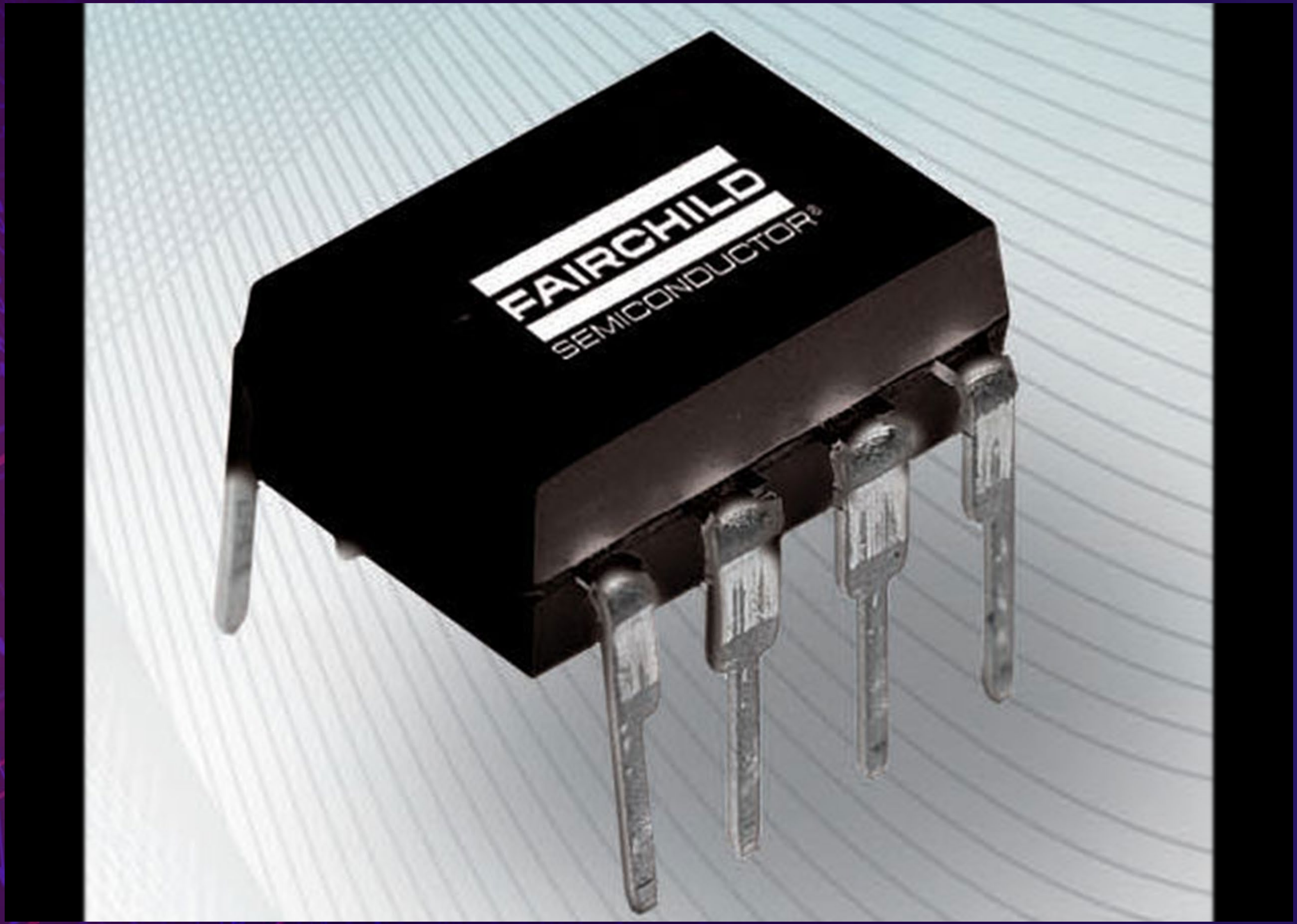
Source: DARPA

Source: PBS

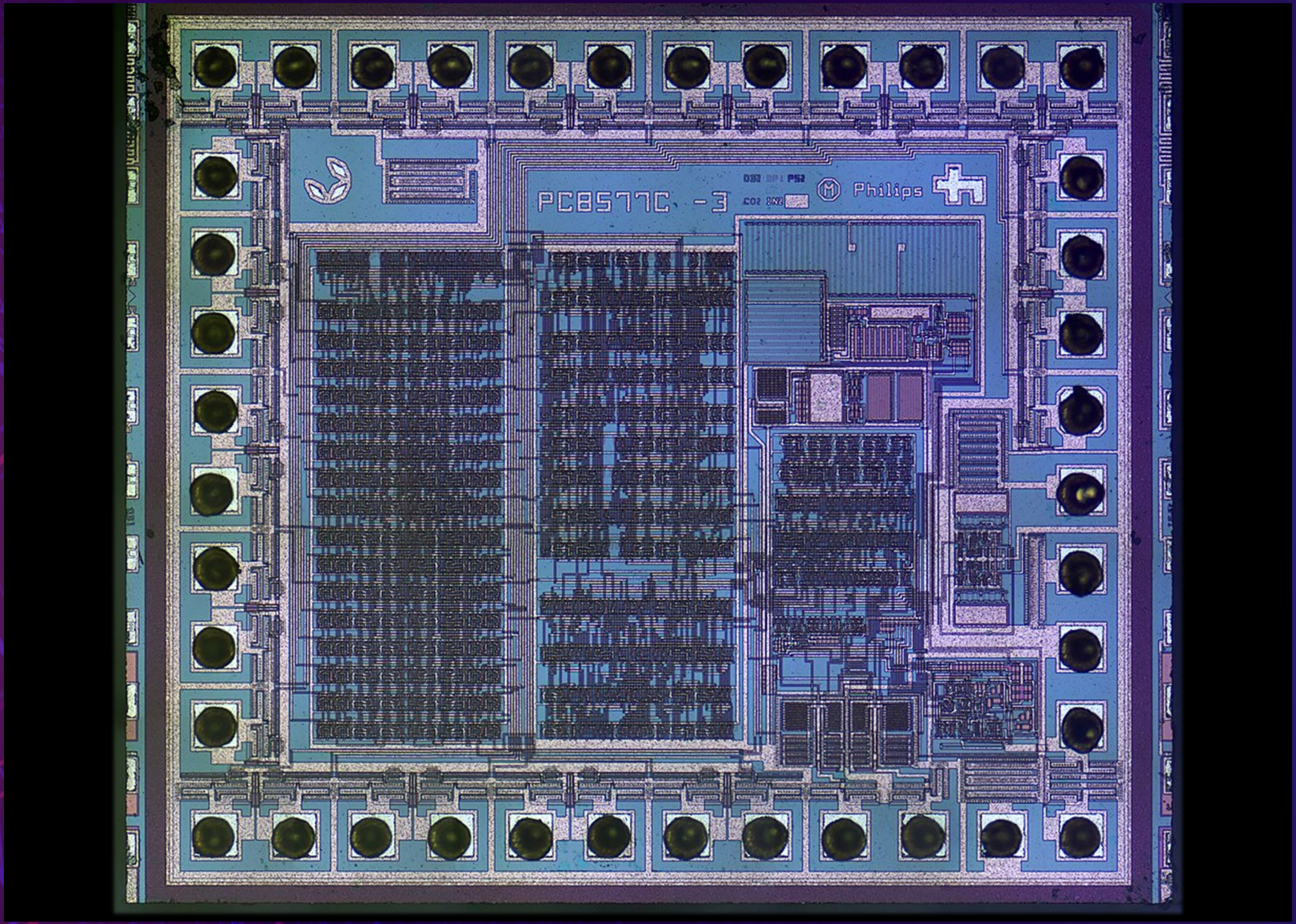


Source: computerhistory.org

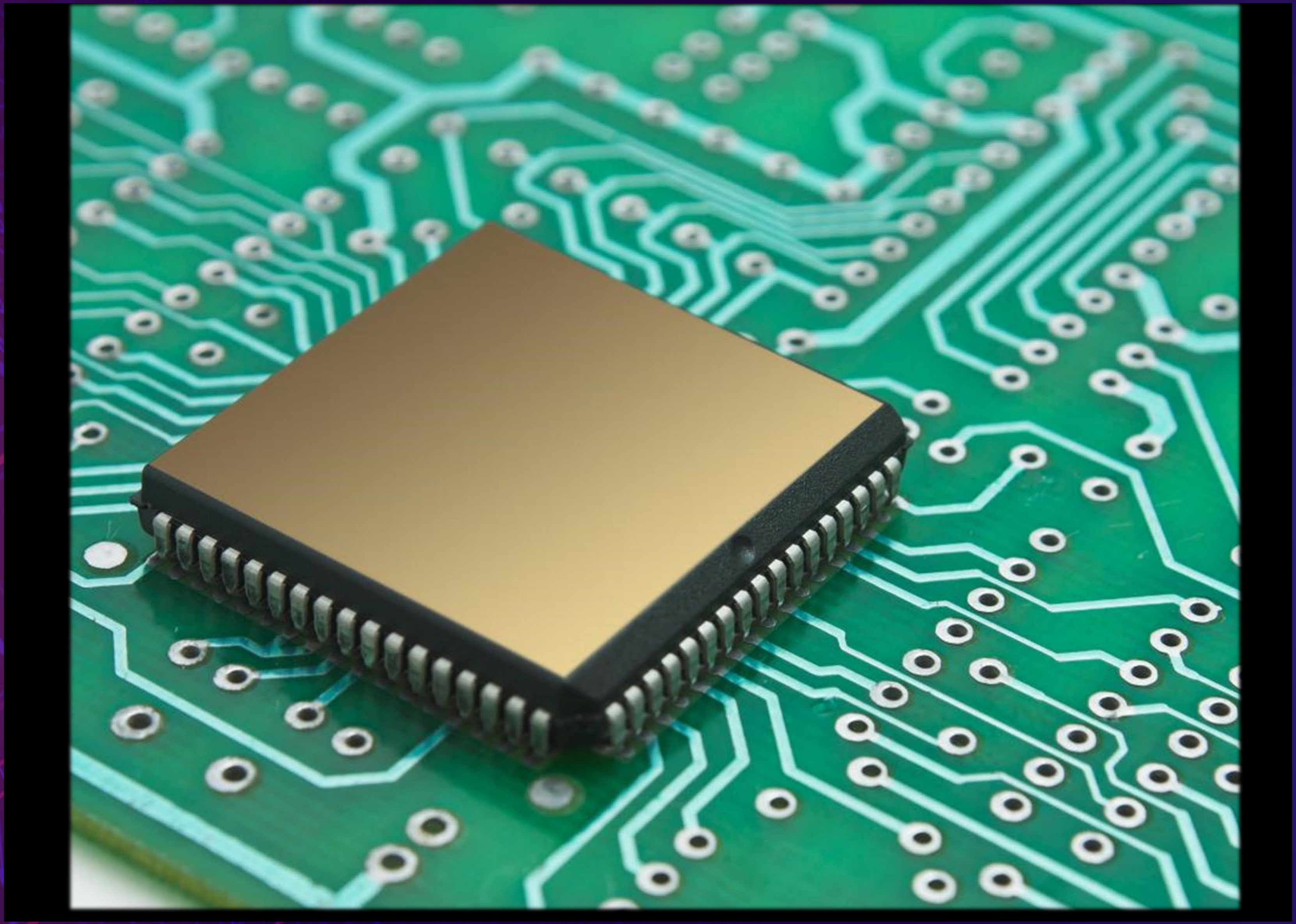
Source: Wikimedia Commons "Bardeen Shockley Brattain 1948" public domain



Source: directindustry.com

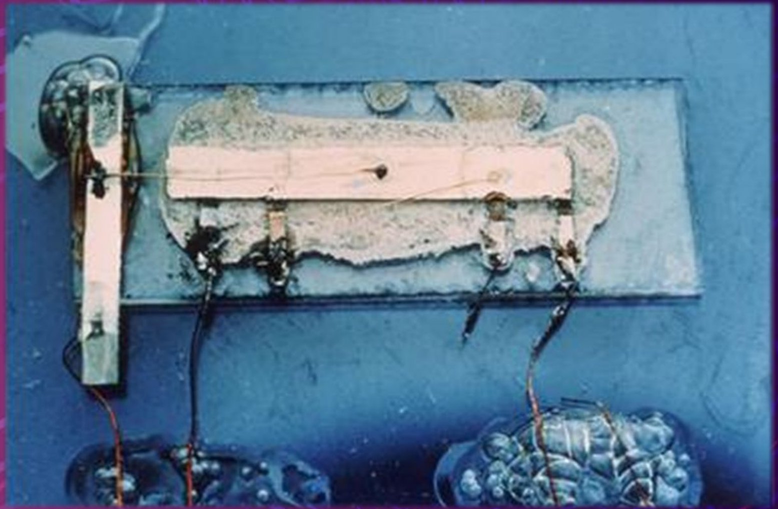


Source: Wikimedia Commons "NXP PCF8577C LCD driver with I²C (Colour Corrected)" by cole8888 CC BY-SA 2.0

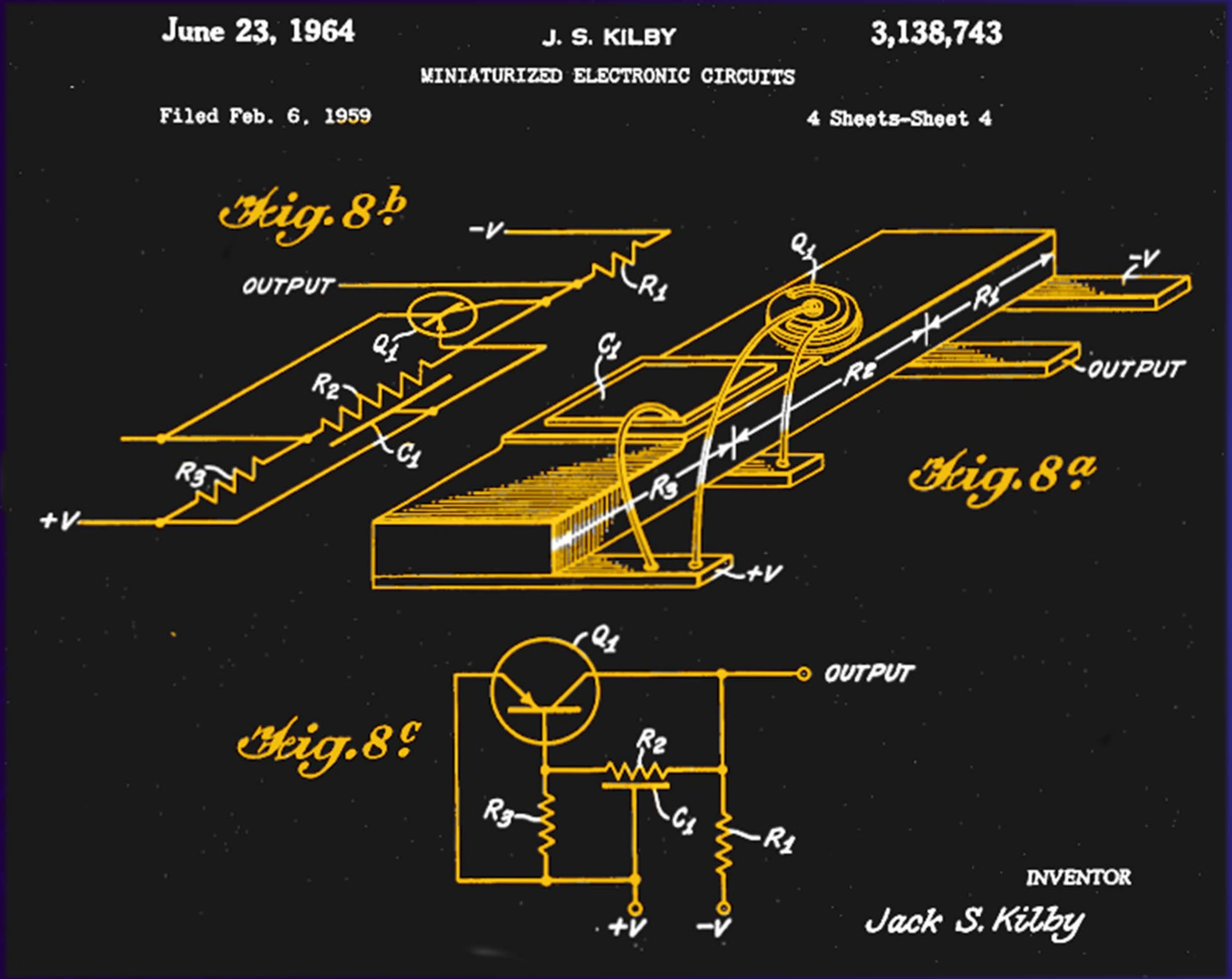


Source: easytechjunkie.com

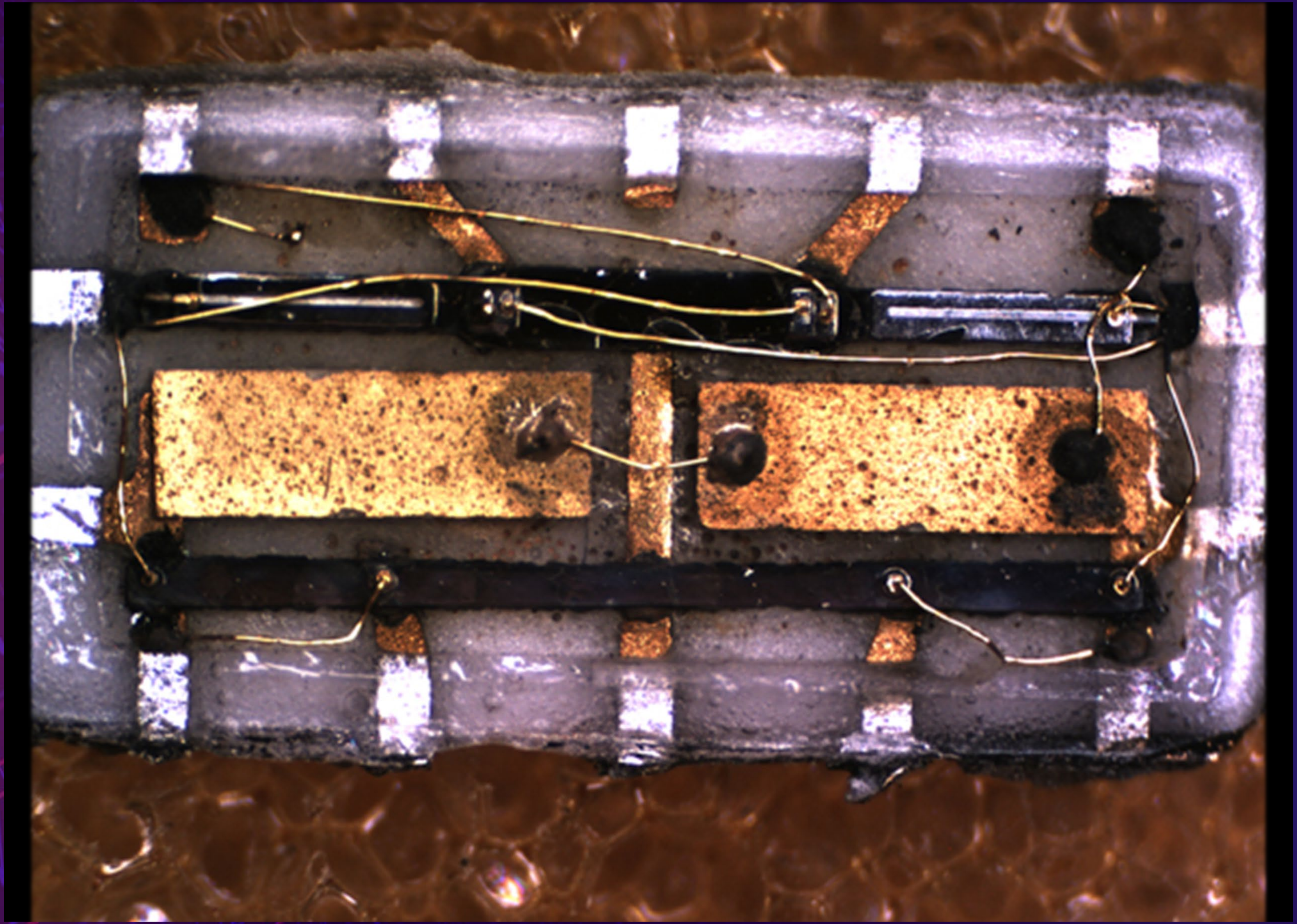
Source: computerhistory.org



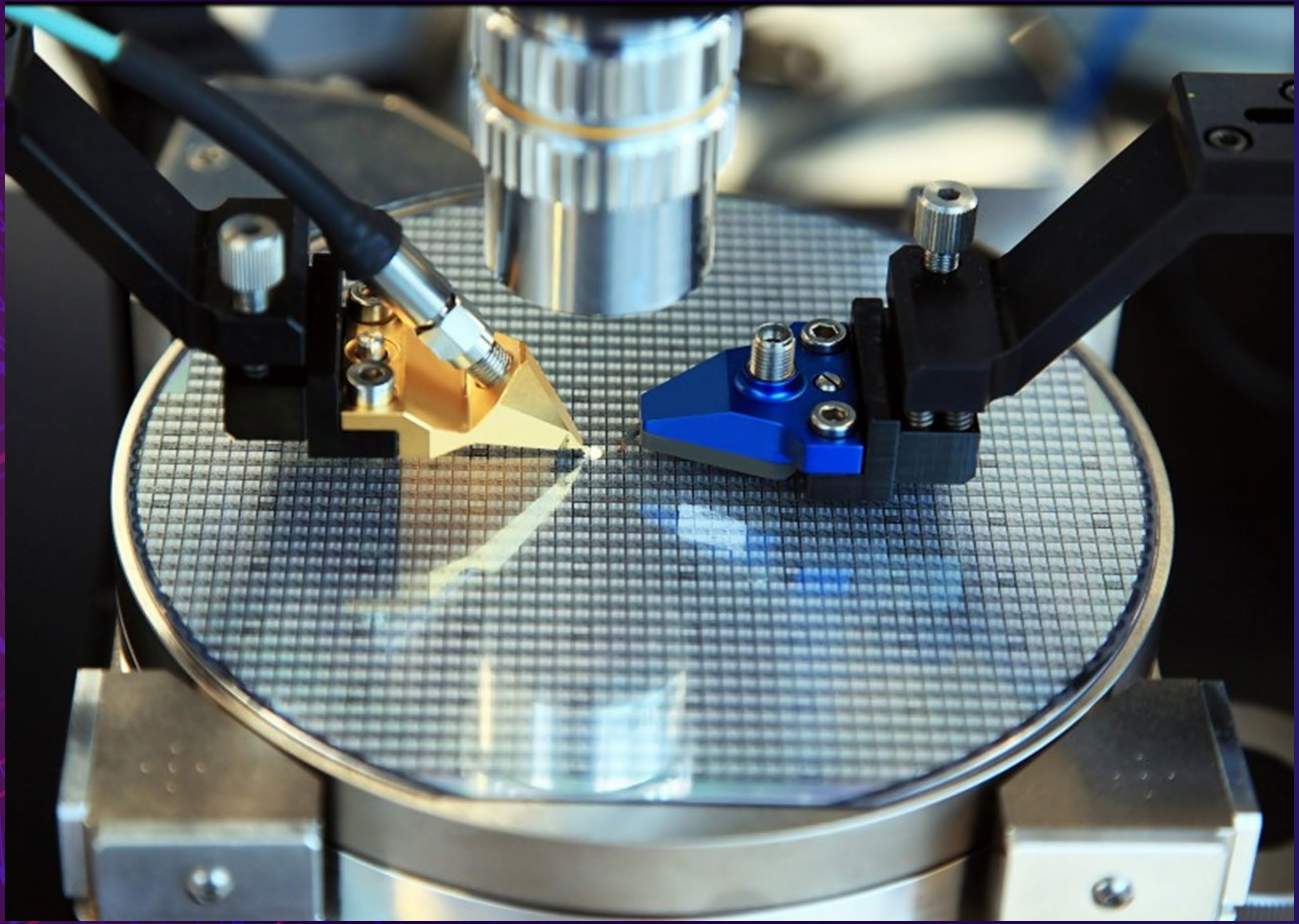
Source: Wikipedia "Kilby solid circuit"



Source: hackaday.com



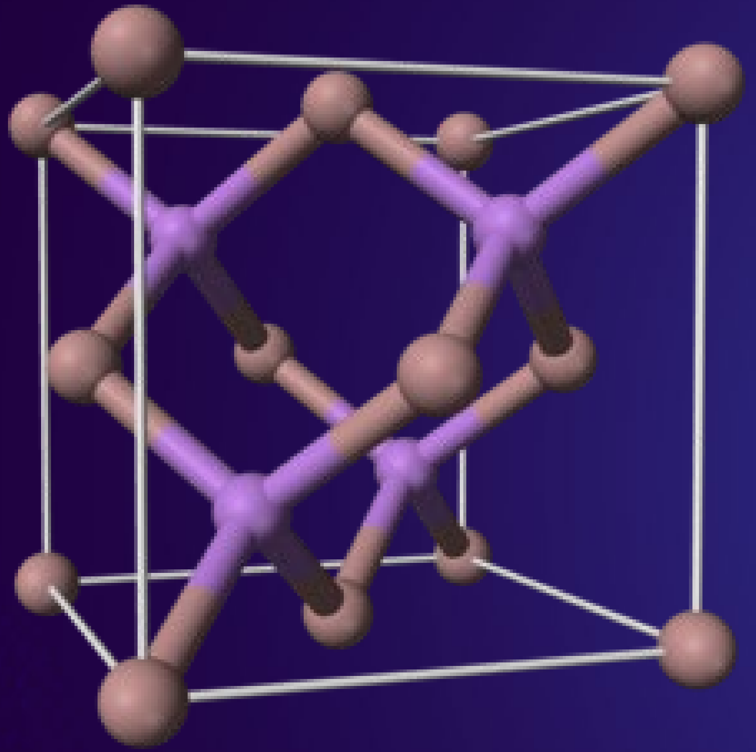
Source: computerhistory.org


Source: waferpro.com

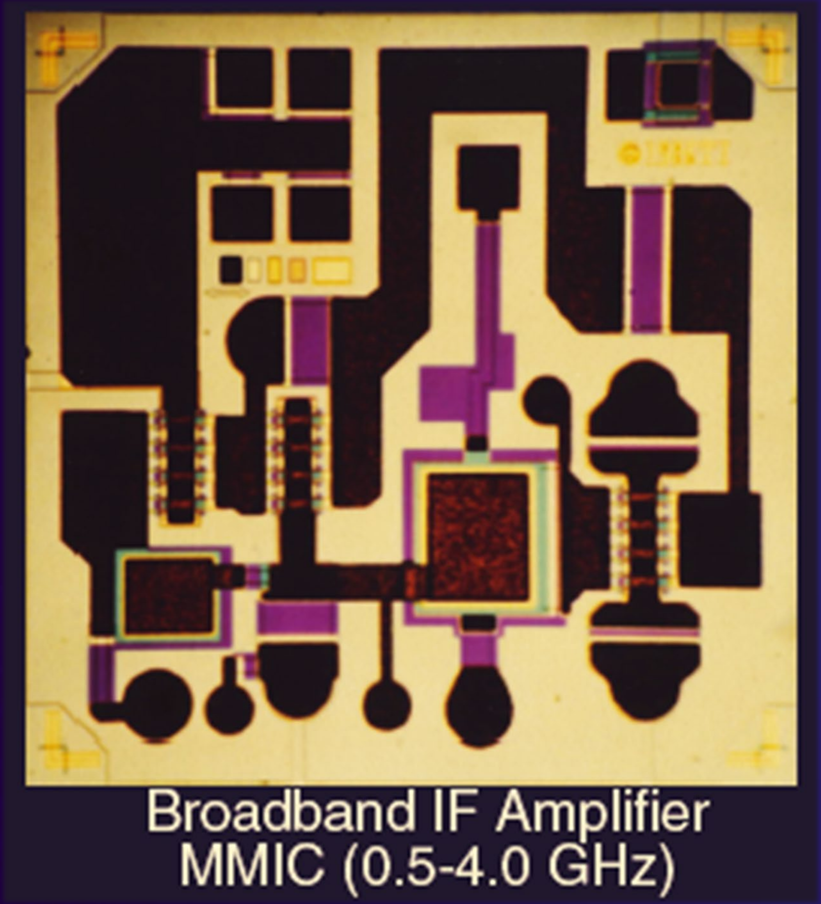
DEFENSE ADVANCED RESEARCH PROJECTS AGENCY

ARPA

Source: DARPA

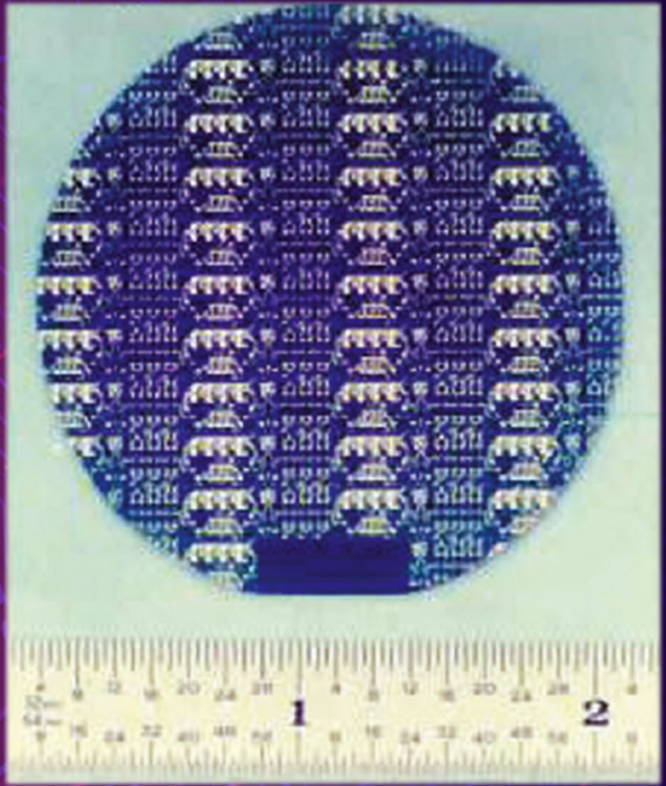


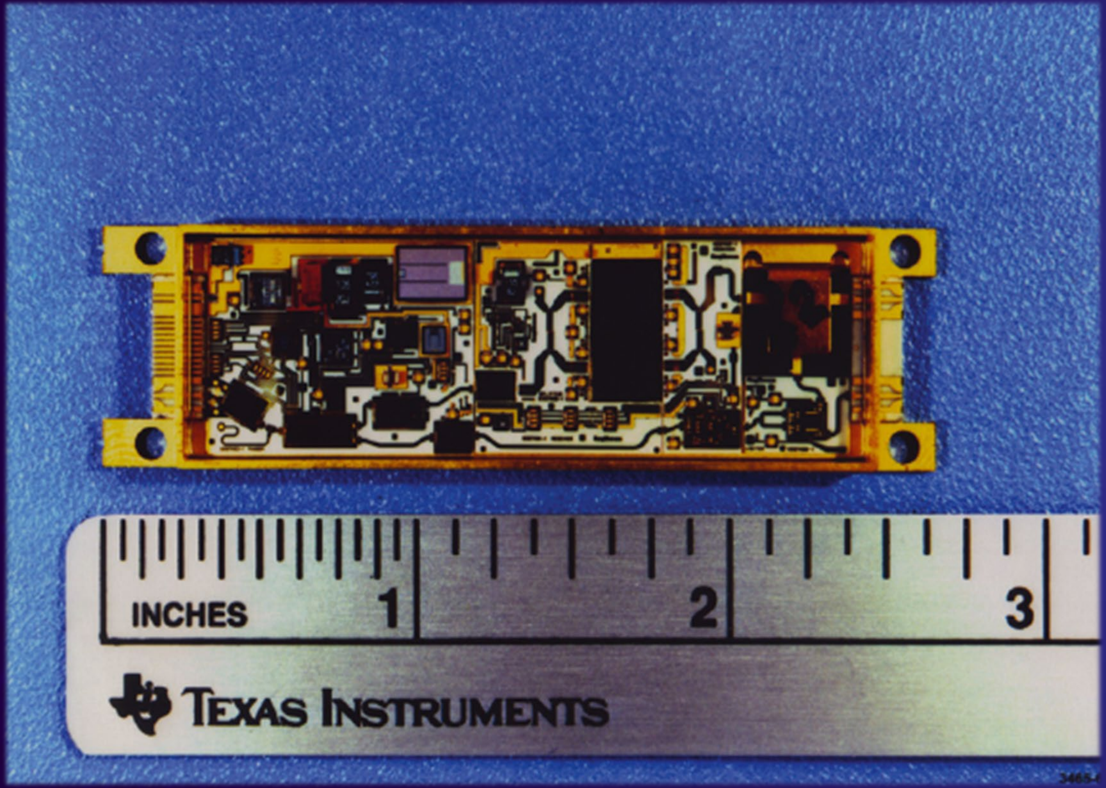
Source: Wikimedia Commons "Gallium arsenide unit cell 3D balls" public domain



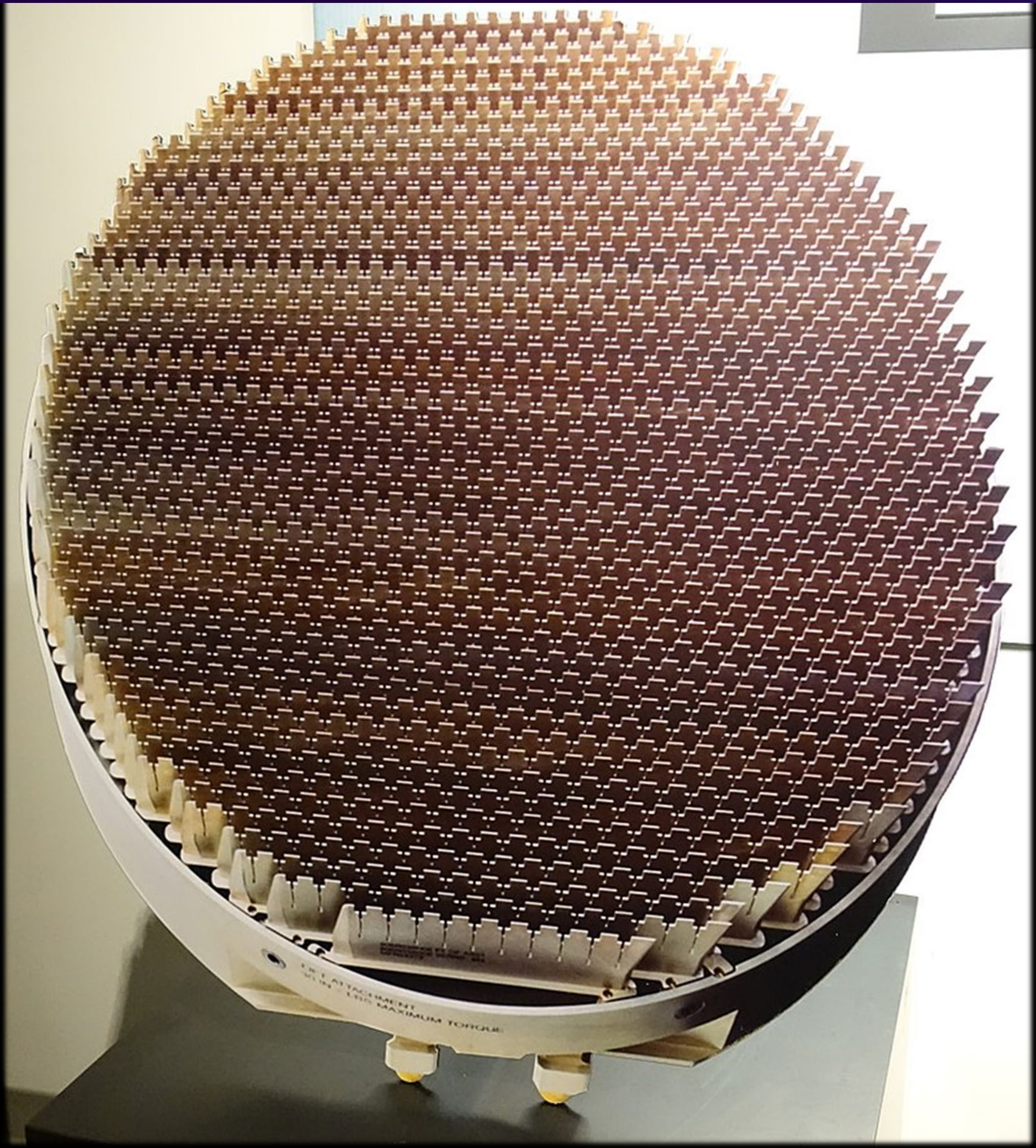
Intermediate frequency amplifier from the Microwave and Millimeter-wave Monolithic Integrated Circuit (MIMIC) program

Source: The MIMIC Program - A Retrospective, paper by Eliot D. Cohen. Authorized licensed use limited to: DARPA.





DARPA Microwave and Millimeter-wave Monolithic Integrated Circuit (MIMIC) program
Source: The MIMIC Program - A Retrospective, paper by Eliot D. Cohen. Authorized licensed use limited to: DARPA.



Source: Wikimedia Commons “AN-APG-81 Antenna“ public domain

Source: practicallynetworked.com

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore
Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

But the biggest potential lies in the production of large systems. In telephone communications, integrated circuits in digital filters will separate channels on multiplex equipment. Integrated circuits will also switch telephone circuits and perform data processing.

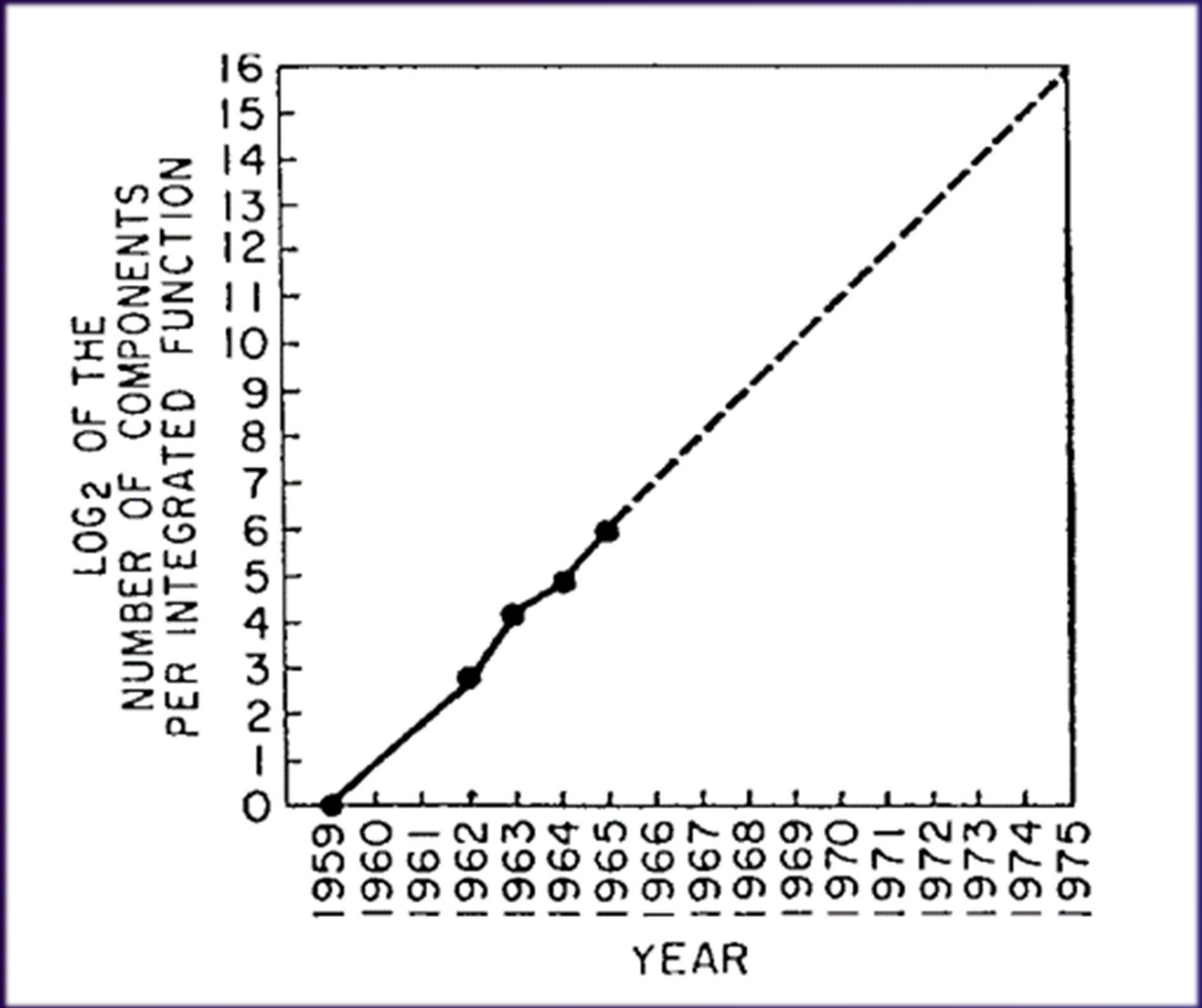
Computers will be more powerful, and will be organized in completely different ways. For example, memories built of integrated electronics may be distributed throughout the machine instead of being concentrated in a central unit. In addition, the improved reliability made possible by integrated circuits will allow the construction of larger processing units. Machines similar to those in existence today will be built at lower costs and with faster turn-around.

Present and future

By integrated electronics, I mean all the various technologies which are referred to as microelectronics today as well as any additional ones that result in electronics functions supplied to the user as irreducible units. These technologies were first investigated in the late 1950's. The object was to miniaturize electronics equipment to include increasingly complex electronic functions in limited space with minimum weight. Several approaches evolved, including microassembly techniques for individual components, thin-film structures and semiconductor integrated circuits.

Each approach evolved rapidly and converged so that

Source: Electronics, Volume 38, Number 8, April 19, 1965



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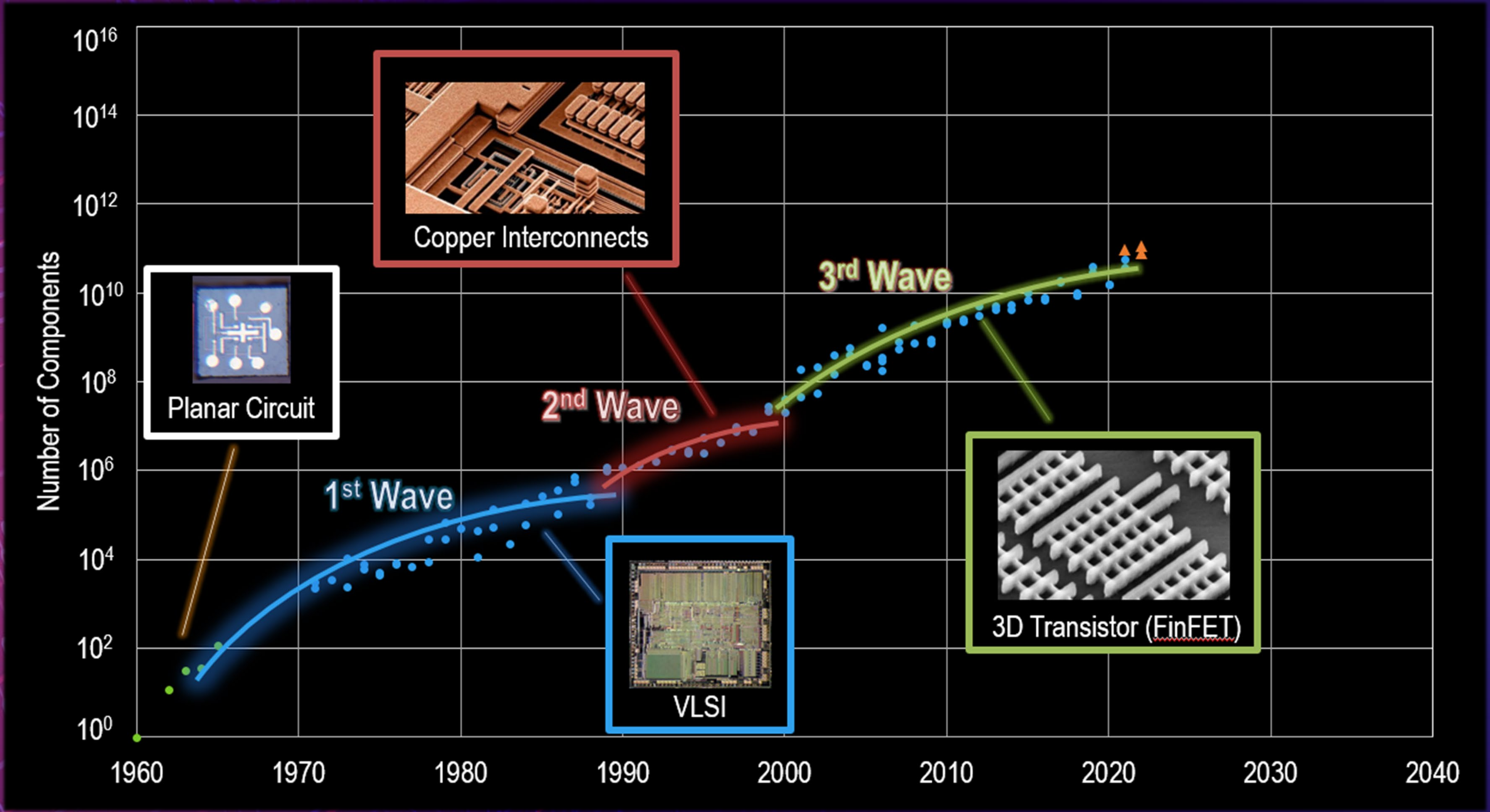
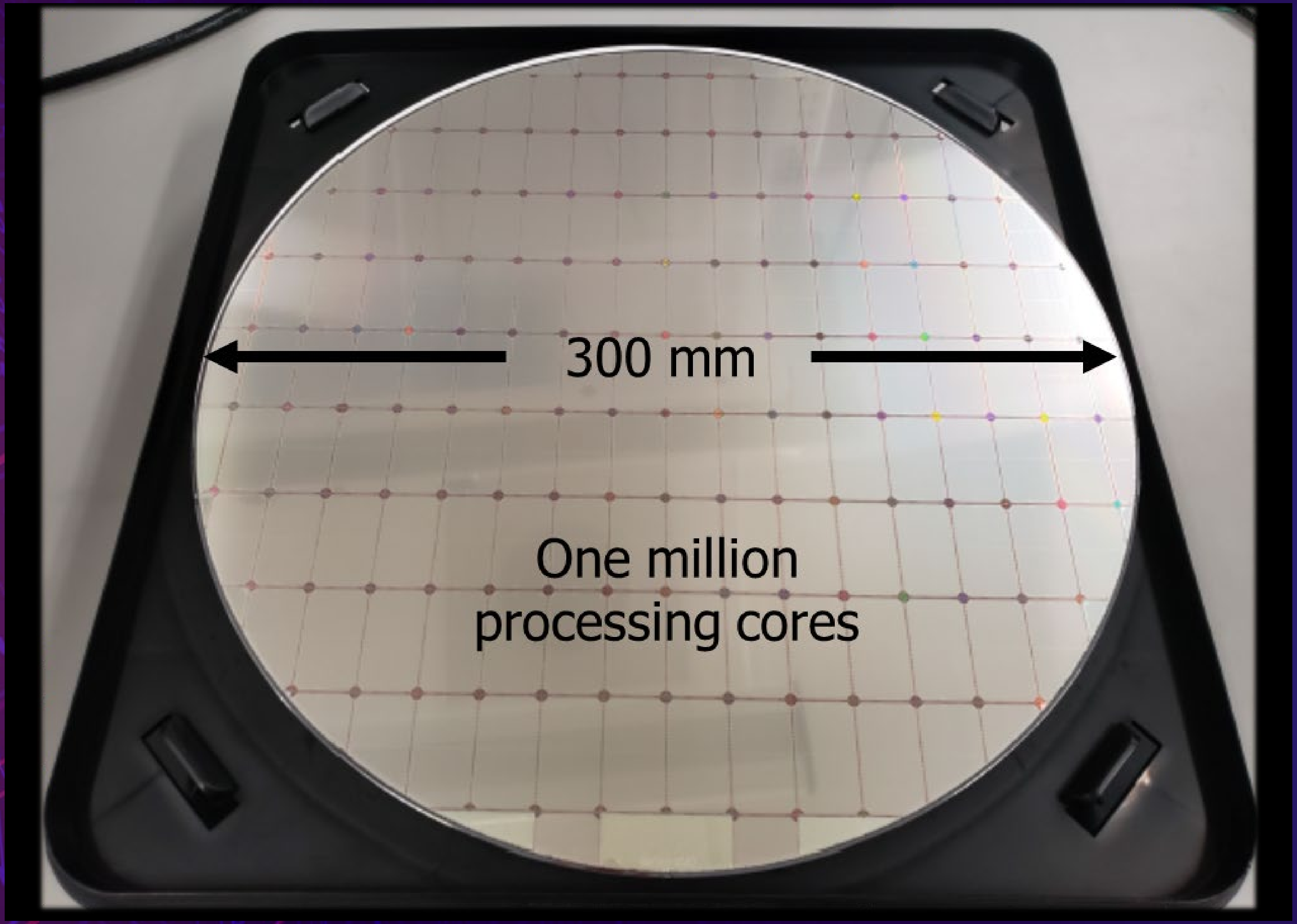


Source: DARPA



Source: DARPA

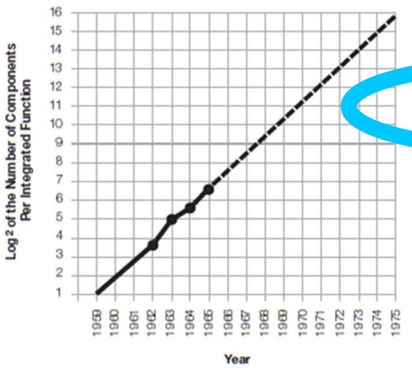
a two-mil square can also contain several kilohms of resistance or a few diodes. This allows at least 500 components per linear inch or a quarter million per square inch. Thus, 65,000 components need occupy only about one-fourth a square inch.

On the silicon wafer currently used, usually an inch or more in diameter, there is ample room for such a structure if the components can be closely packed with no space wasted for interconnection patterns. This is realistic, since efforts to achieve a level of complexity above the presently available integrated circuits are already underway using multilayer metalization patterns separated by dielectric films. Such a density of components can be achieved by present optical techniques and does not require the more exotic techniques, such as electron beam operations, which are being studied to make even smaller structures.

Increasing the yield

There is no fundamental obstacle to achieving device yields of 100%. At present, packaging costs so far exceed the cost of the semiconductor structure itself that there is no incentive to improve yields, but they can be raised as high as is economically justified. No barrier exists comparable to the thermodynamic equilibrium considerations that often limit yields in chemical reactions; it is not even necessary to do any fundamental research or to replace present processes. Only the engineering effort is needed.

In the early days of integrated circuitry, when yields were extremely low, there was such incentive. Today ordinary integrated circuits are made with yields comparable with those obtained for individual semiconductor devices. The same pattern will make larger arrays economical, if other considerations make such arrays desirable.



Heat problem

Will it be possible to remove the heat generated by tens of thousands of components in a single silicon chip?

If we could shrink the volume of a standard high-speed digital computer to that required for the components themselves, we would expect it to glow brightly with present power dissipation. But it won't happen with integrated circuits. Since integrated electronic structures are two-dimensional, they have a surface available for cooling close to each center of heat generation. In addition, power is needed primarily to drive the various lines and capacitances associated with the system. As long as a function is confined to a small area on a wafer, the amount of capacitance which must be driven is distinctly limited. In fact, shrinking dimensions on an integrated structure makes it possible to operate the structure at higher speed for the same power per unit area.

Day of reckoning

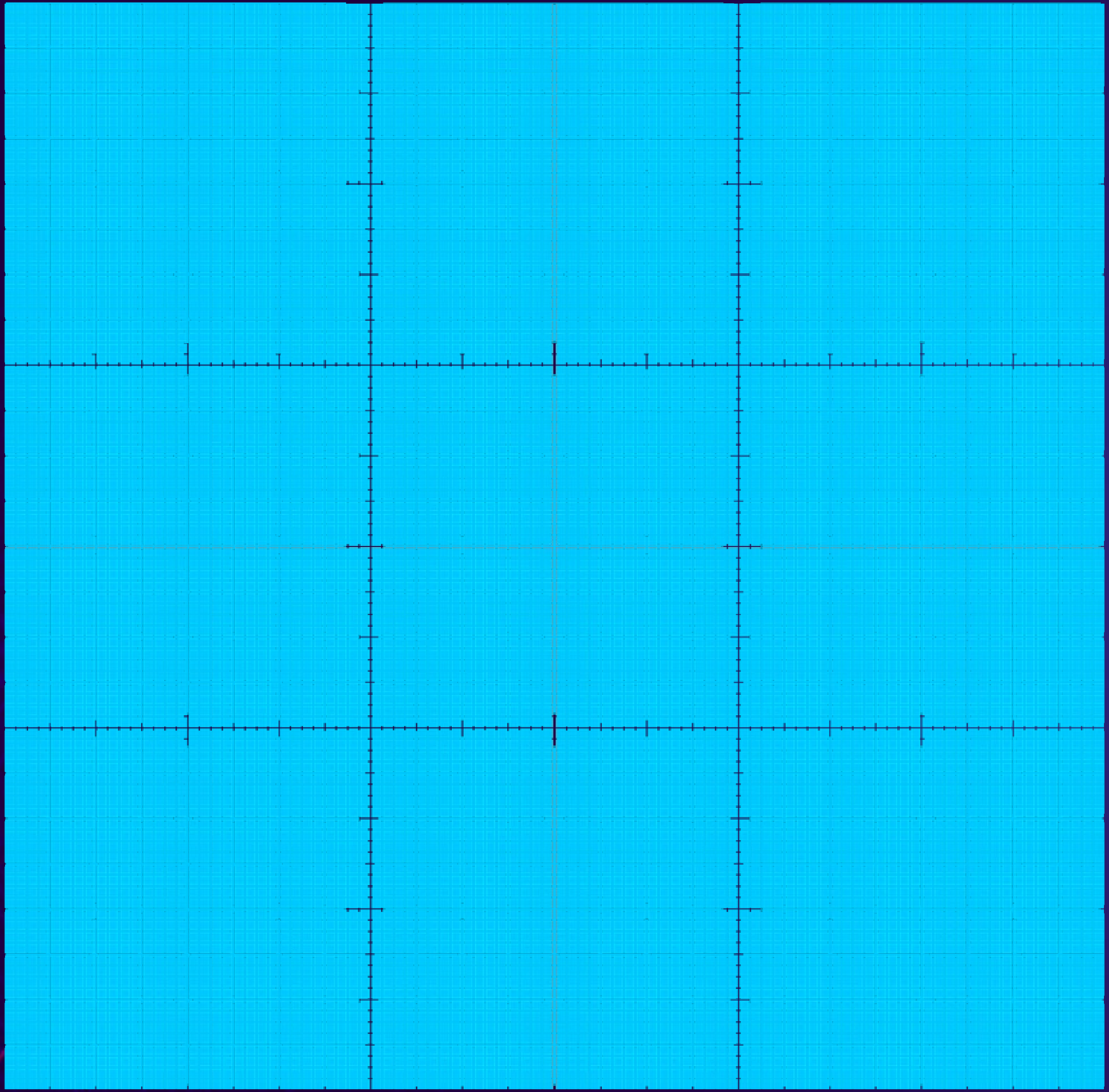
Clearly, we will be able to build such component-crammed equipment. Next, we ask under what circumstances we should do it. The total cost of making a particular system function must be minimized. To do so, we could amortize the engineering over several identical items, or evolve flexible techniques for the engineering of large functions so that no disproportionate expense need be borne by a particular array. Perhaps newly devised design automation procedures could translate from logic diagram to technological realization without any special engineering.

It may prove to be more economical to build large

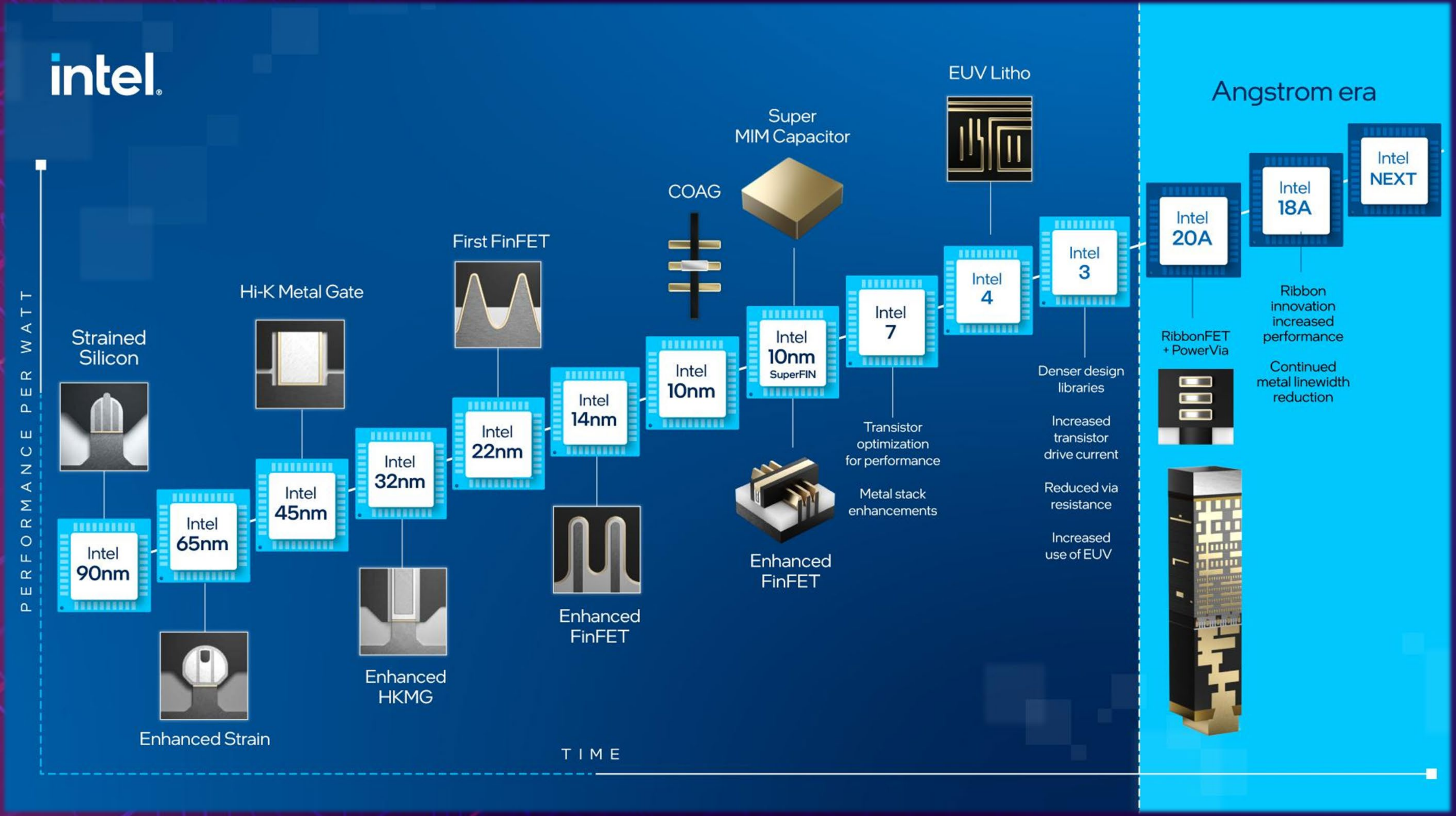
"Day of reckoning"

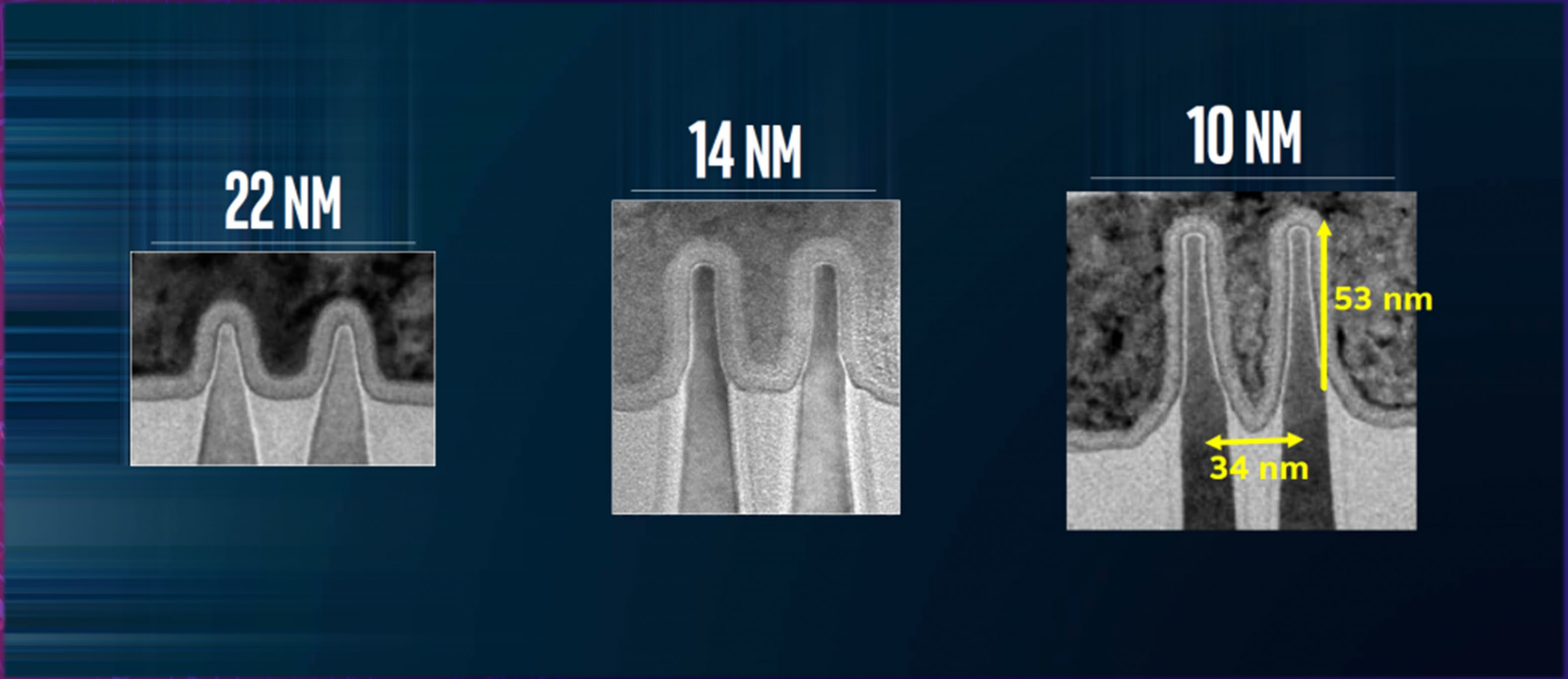
– Gordon Moore

Source: Electronics, Volume 38, Number 8, April 19, 1965

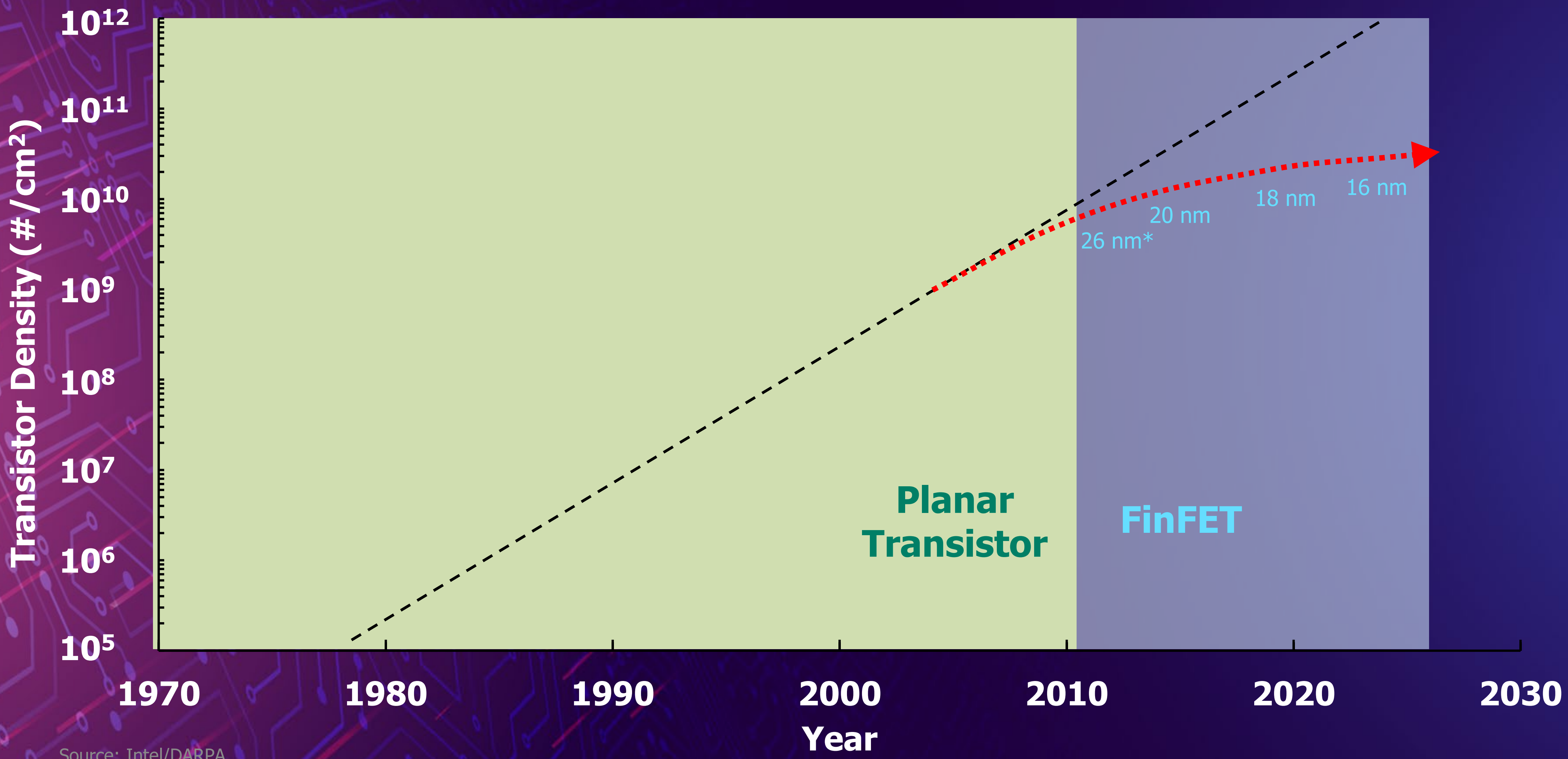


Source: DARPA


intel
Angstrom era
PERFORMANCE PER WATT
TIME
Strained Silicon
Intel 90nm
Enhanced Strain
Intel 65nm
Hi-K Metal Gate
Intel 45nm
Enhanced HKMG
Intel 32nm
First FinFET
Intel 22nm
Intel 14nm
Enhanced FinFET
COAG
Intel 10nm
Super MIM Capacitor
Intel 10nm SuperFIN
Enhanced FinFET
Intel 7
Transistor optimization for performance
Metal stack enhancements
EUV Litho
Intel 4
Intel 3
Denser design libraries
Increased transistor drive current
Reduced via resistance
Increased use of EUV
Intel 20A
RibbonFET + PowerVia
Intel 18A
Ribbon innovation increased performance
Continued metal linewidth reduction
Intel NEXT



Source: Intel



Source: Intel/DARPA

* Physical gate length of 22nm technology node

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The author

Dr. Gordon E. Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather than in electronics. He earned a B.S. degree in chemistry from the University of California and a Ph.D. degree in physical chemistry from the California Institute of Technology. He was one of the founders of Fairchild Semiconductor and has been director of the research and development laboratories since 1959.

Present and future

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Each approach evolved rapidly and converged so that each borrowed techniques from another. Many researchers believe the way of the future to be a combination of the various approaches.

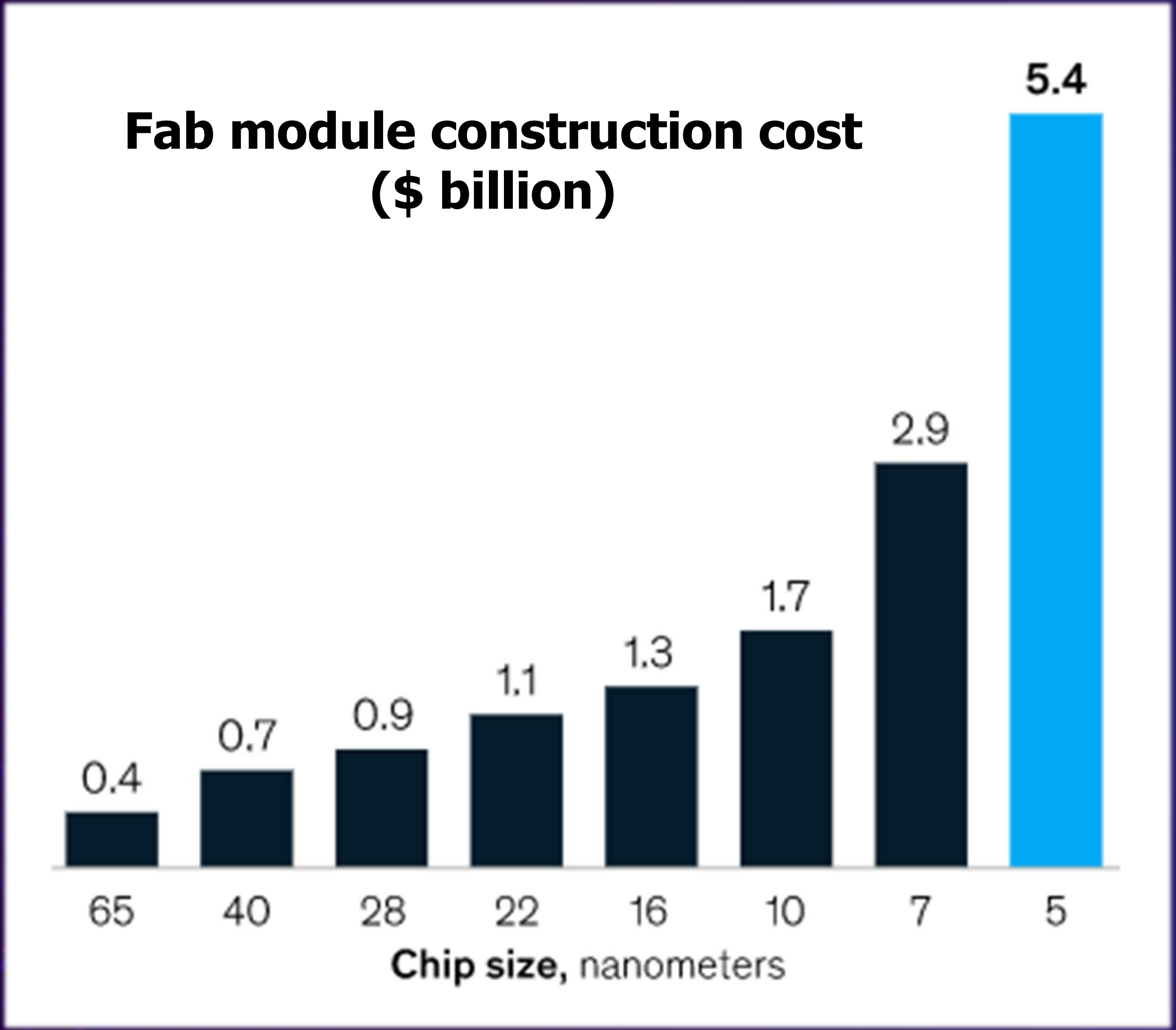
The advocates of semiconductor integrated circuitry are already using the improved characteristics of thin-film resistors by applying such films directly to an active semiconductor substrate. Those advocating a technology based upon films are developing sophisticated techniques for the attachment of active semiconductor devices to the passive film arrays.

Both approaches have worked well and are being used in equipment today.

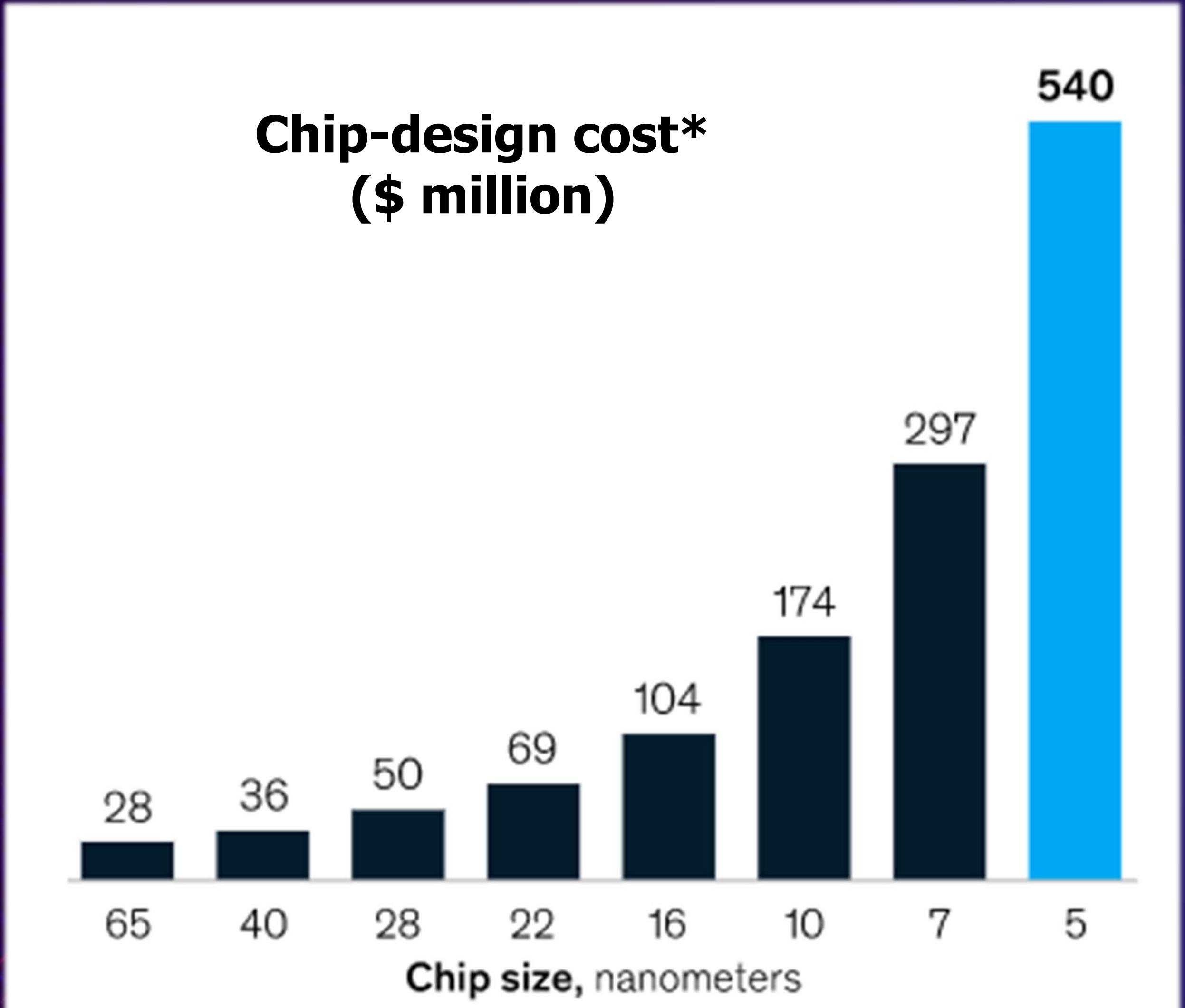
"It may prove more economical to **build large systems out of smaller functions, which are separately packaged and interconnected**. The availability of large functions, combined with functional design and construction, should allow the manufacturer of large systems to design and construct a considerable variety of equipment both rapidly and economically."

– Gordon Moore

Source: Electronics, Volume 38, Number 8, April 19, 1965

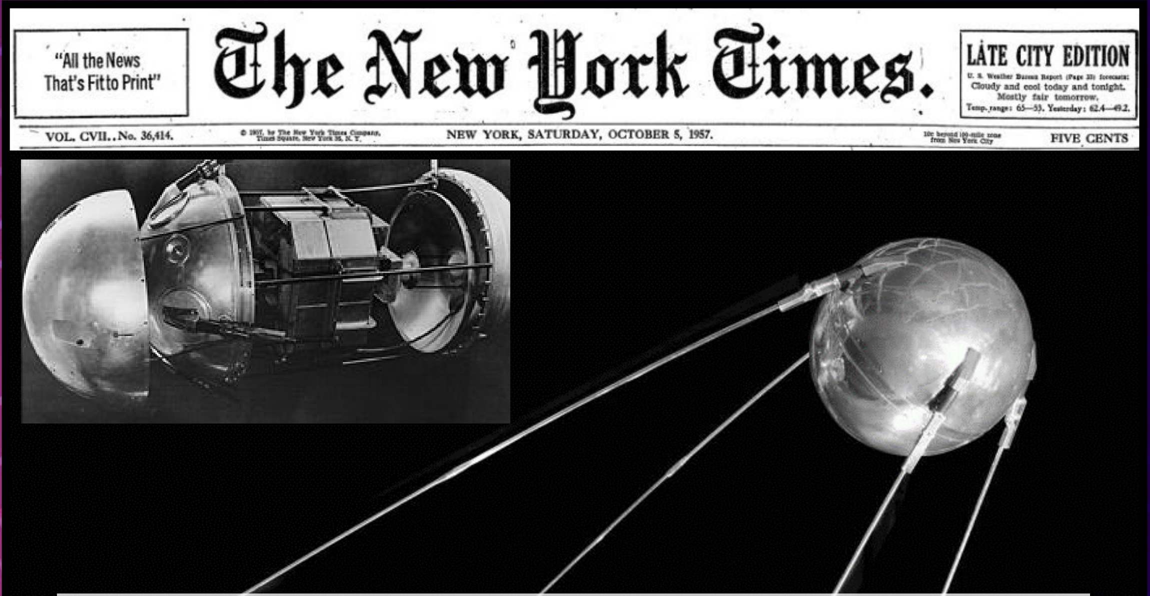


Source: IBS/McKinsey, "Semiconductor design and manufacturing: Achieving leading-edge capabilities," McKinsey, 2020



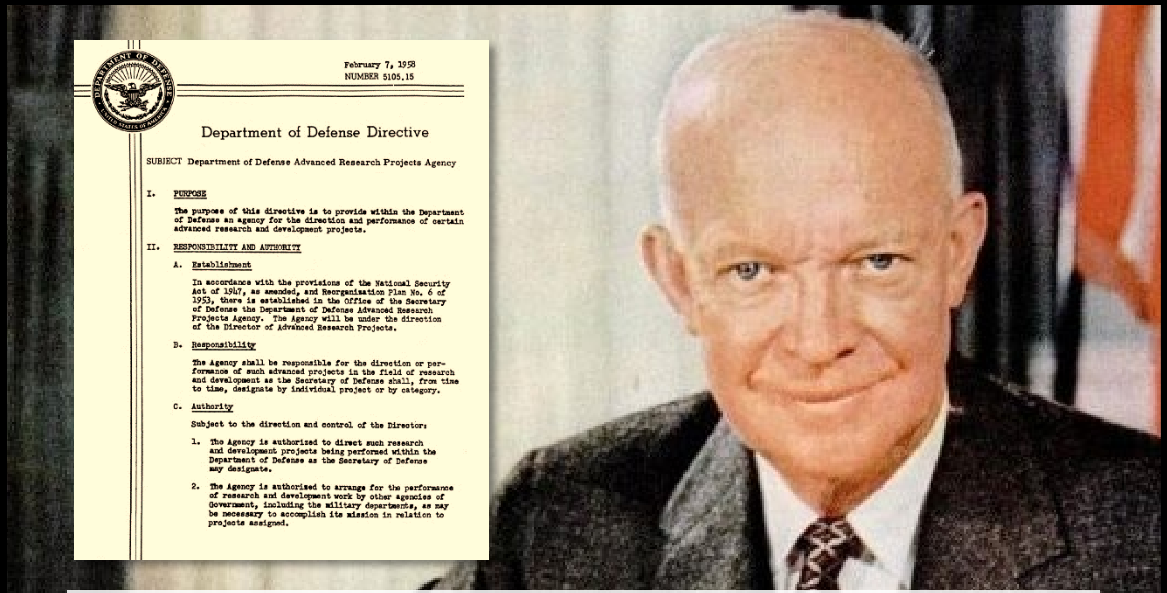
*Major components include IP qualification, architecture, verification, physical, software, prototyping, and validation.

Source: IBS/McKinsey, "Semiconductor design and manufacturing: Achieving leading-edge capabilities," McKinsey, 2020



October 4, 1957

U.S.S.R. beats U.S. to space with Sputnik satellite; U.S. should never again be surprised by technology.



February 7, 1958
NUMBER 5105.15

Department of Defense Directive

SUBJECT Department of Defense Advanced Research Projects Agency

I. PURPOSE

The purpose of this directive is to provide within the Department of Defense an agency for the direction and performance of certain advanced research and development projects.

II. RESPONSIBILITY AND AUTHORITY

A. Establishment

In accordance with the provisions of the National Security Act of 1947, as amended, and Reorganization Plan No. 6 of 1953, there is established in the Office of the Secretary of Defense the Department of Defense Advanced Research Projects Agency. The Agency will be under the direction of the Director of Advanced Research Projects.

B. Responsibility

The Agency shall be responsible for the direction or performance of such advanced projects in the field of research and development as the Secretary of Defense shall, from time to time, designate by individual project or by category.

C. Authority

Subject to the direction and control of the Director:

1. The Agency is authorized to direct such research and development projects being performed within the Department of Defense as the Secretary of Defense may designate.

2. The Agency is authorized to arrange for the performance of research and development work by other agencies of Government, including the military departments, as may be necessary to accomplish its mission in relation to projects assigned.

February 7, 1958

"The purpose of this directive is to provide within the Department of Defense an agency for the direction and performance of certain advanced research and development projects."

ELECTRONICS RESURGENCE INITIATIVE SUMMIT
2018 | SAN FRANCISCO, CA | JULY 23-25

ERI ELECTRONICS RESURGENCE INITIATIVE SUMMIT & MTO Symposium

PCAST Report on Semiconductor Leadership


REPORT TO THE PRESIDENT
Ensuring Long-Term U.S. Leadership in Semiconductors

Executive Office of the President
President's Council of Advisors on Science and Technology

January 2017

ERI

FY17 | FY18 | FY19 | FY20 | FY21 | FY22

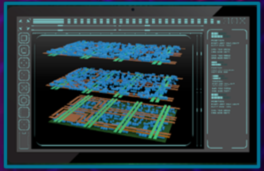
ERI announced

ERI starts

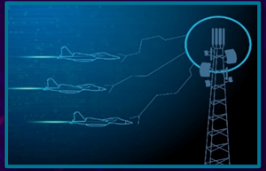
ERI thrusts

Overcoming security threats across the entire hardware lifecycle

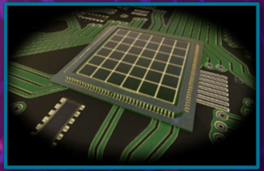
Optimizing design and test for complex circuits and prototypes



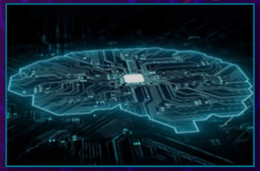
Securing communications



Realizing heterogeneous 3D electronics



Accelerating innovation in artificial intelligence hardware to make decisions at the edge faster

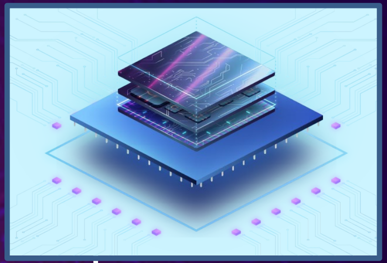


Increasing information processing density and efficiency

Source: Adobe Stock

NGMM Phase 0 BAA
August 2022

ERI Summit 2023
August 22-24 / Seattle, WA



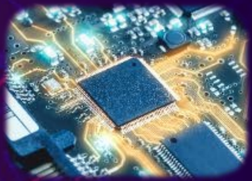
FY22 | FY23 | FY24 | FY25 | FY26 | FY27

Original ERI

ERI 2.0: Reinventing microsystems manufacturing for a new age

TALK

Securing communications

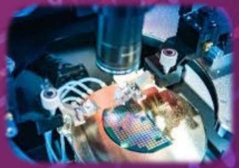


COMPUTE

Increasing information processing efficiency at the edge

DECIDE

Accelerating innovation in AI hardware



BUILD

Manufacturing complex 3D microsystems

COMPOSE

Optimizing design and test for complex circuits

SECURE

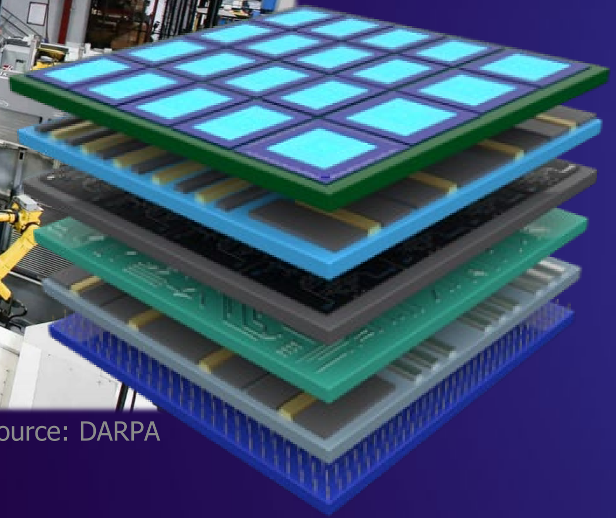
Overcoming security threats across the entire hardware lifecycle

HARDEN

Developing electronics for extreme environments

Manufacturing complex 3D microsystems

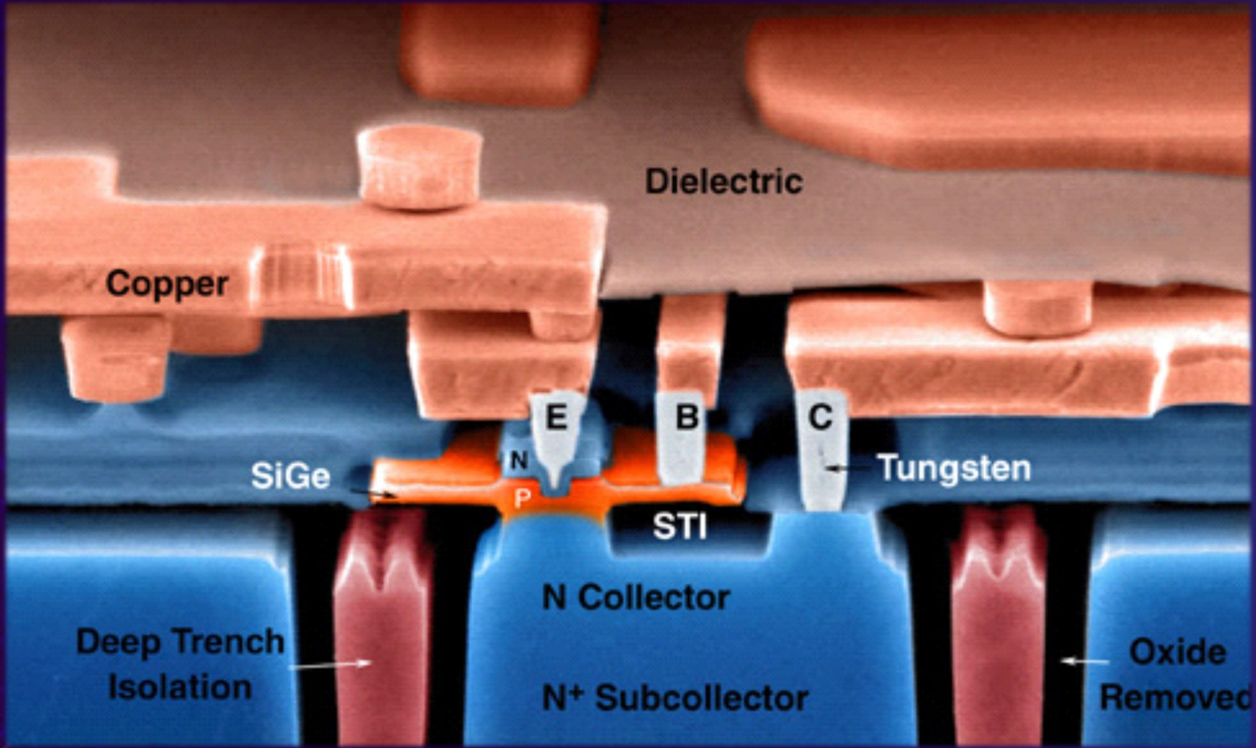
Source: nam.org



Source: DARPA

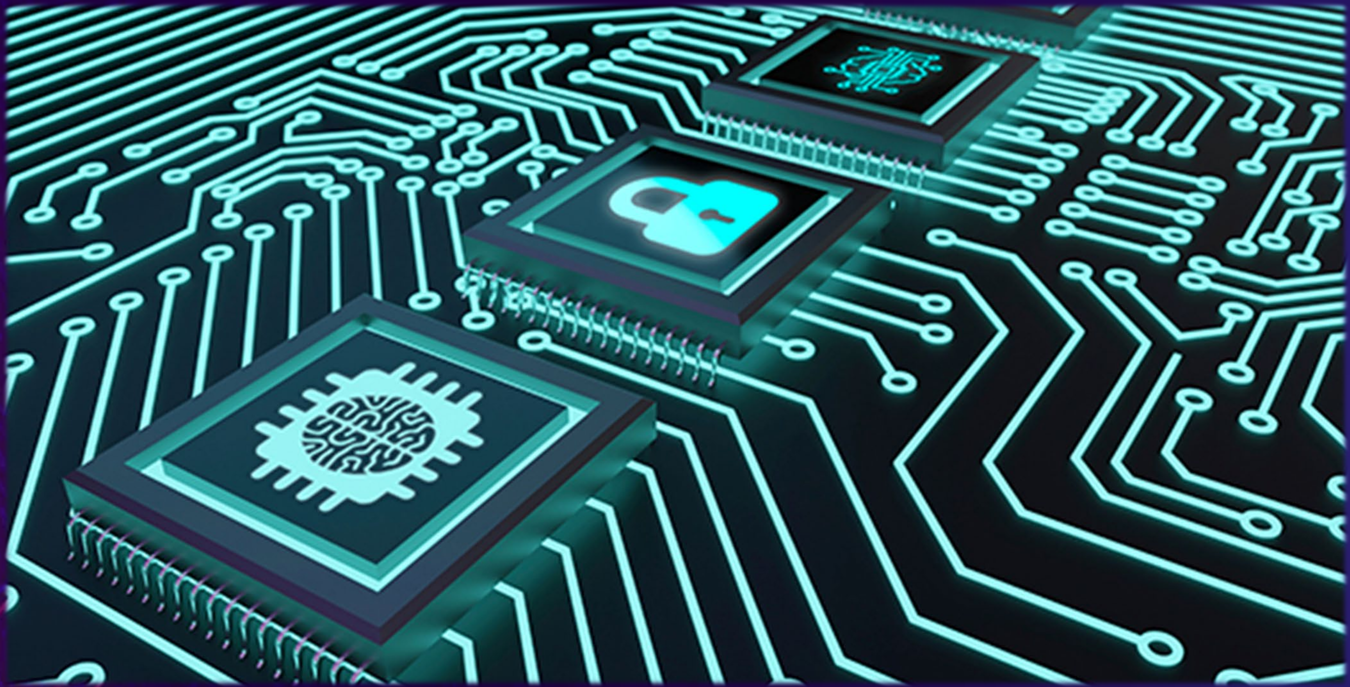
Advanced 3D heterogeneous integration (3DHI) microsystems prototypes

Next-Generation Microelectronics Manufacturing (NGMM) program



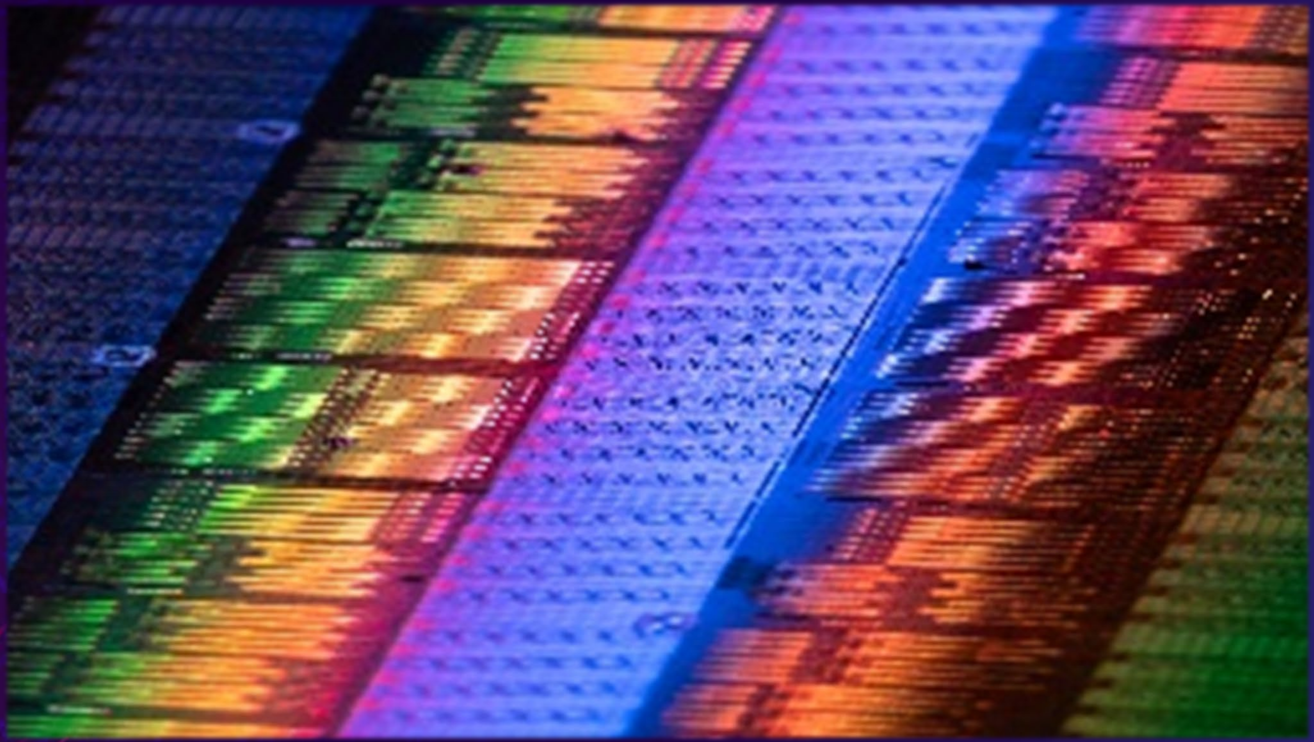
Advanced SiGe electronics for superior mixed-mode electronics

Technologies for Mixed-mode Ultra-Scaled Integrated Circuits (T-MUSIC) program



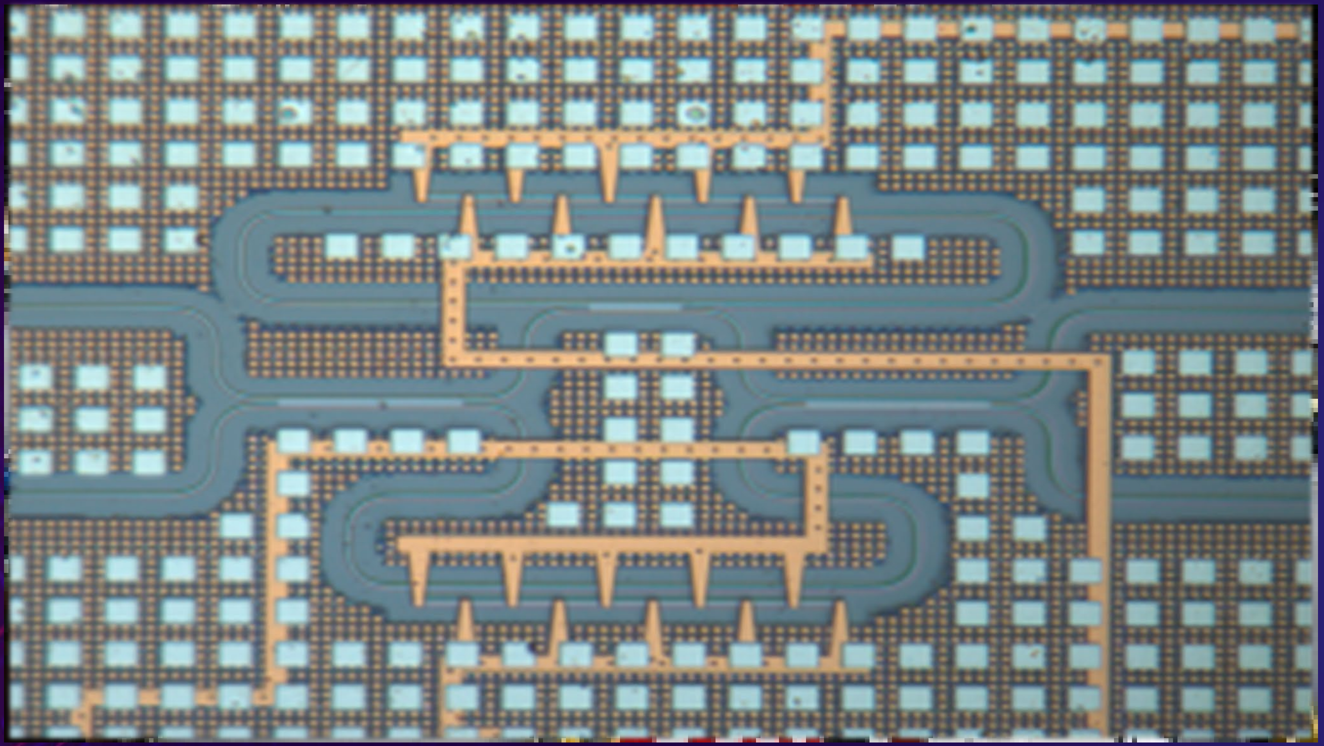
Pathfinding research in new computing and communication technologies

Joint University Microelectronics Program (JUMP) 2.0 program



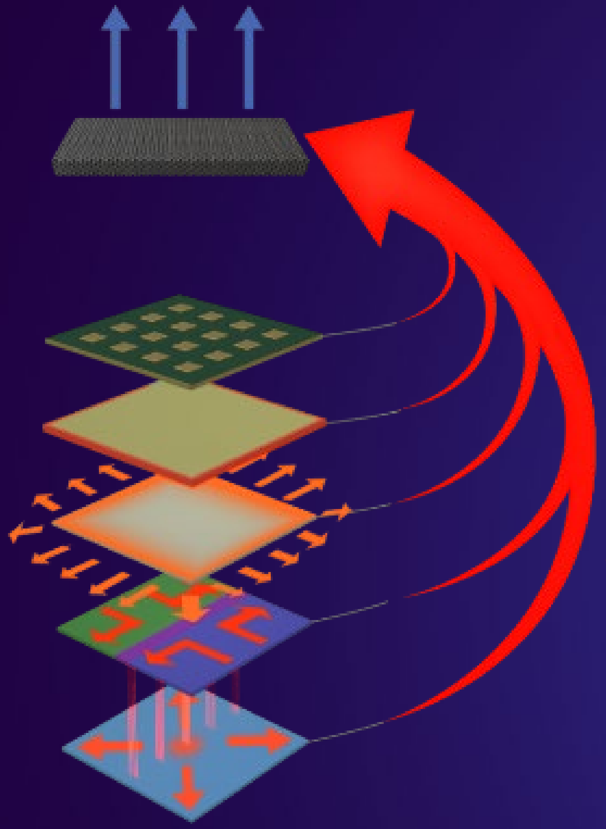
Integrated lasers and amplifiers on high-performance photonics platforms

Lasers for Universal Microscale Optical Systems (LUMOS) program



In-package optical signaling through integration of nanophotonics

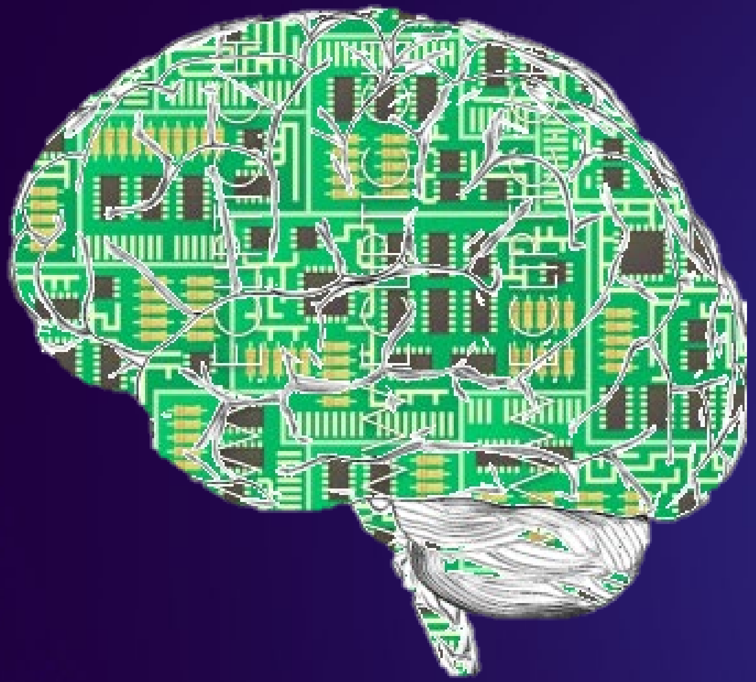
Photonics in the Package for Extreme Scalability (PIPES) program



Cooling technologies to support 3D integration

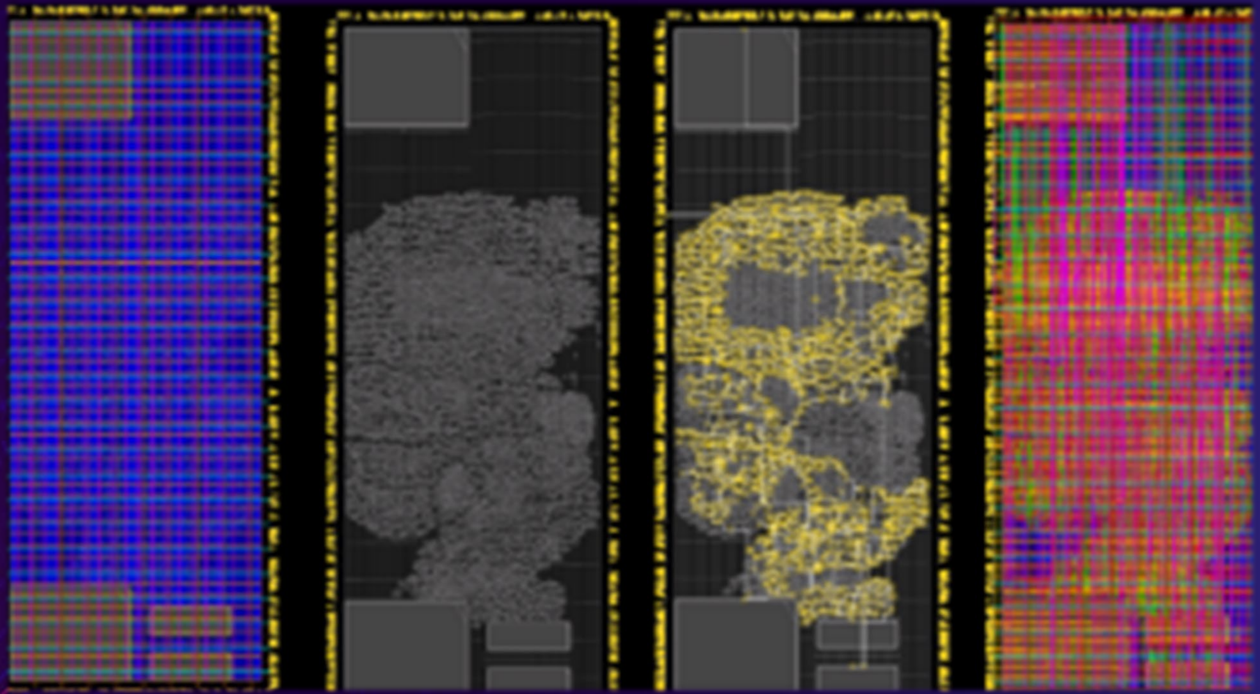
Miniature Thermal Management Systems for Three-Dimensional Heterogeneous Integration (Minitherms3D) program

Optimizing design and test for complex circuits



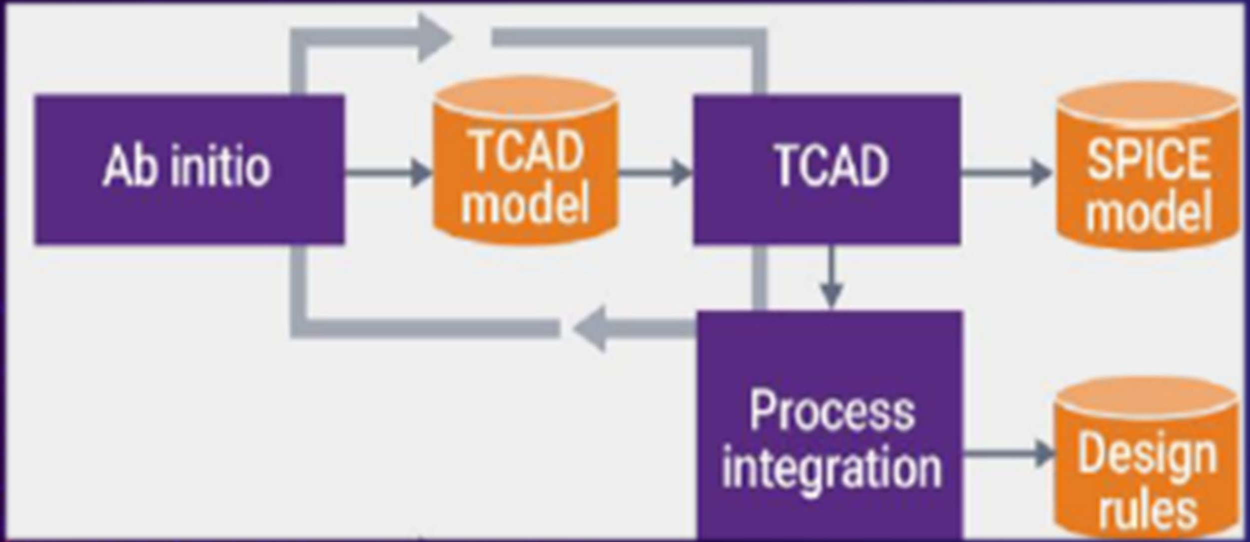
Third wave AI techniques using faster surrogate models

Intelligent Auto-Generation and Composition of Surrogate Models (DITTO) program



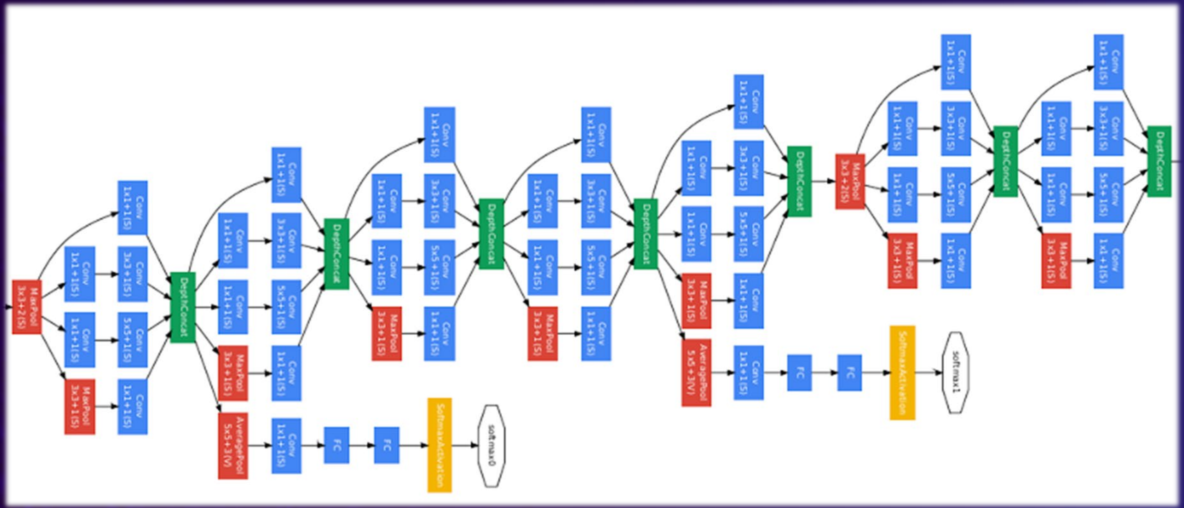
Electronic design automation that learns

Intelligent Design of Electronic Assets (IDEA) program



Predictive advanced device simulation for next-generation electronics

Predictive Nanoscale Simulation for the Terahertz (THz) Regime (NanoSim) program



Source: towardsdatascience.com

Machine learning hardware that adapts in real time

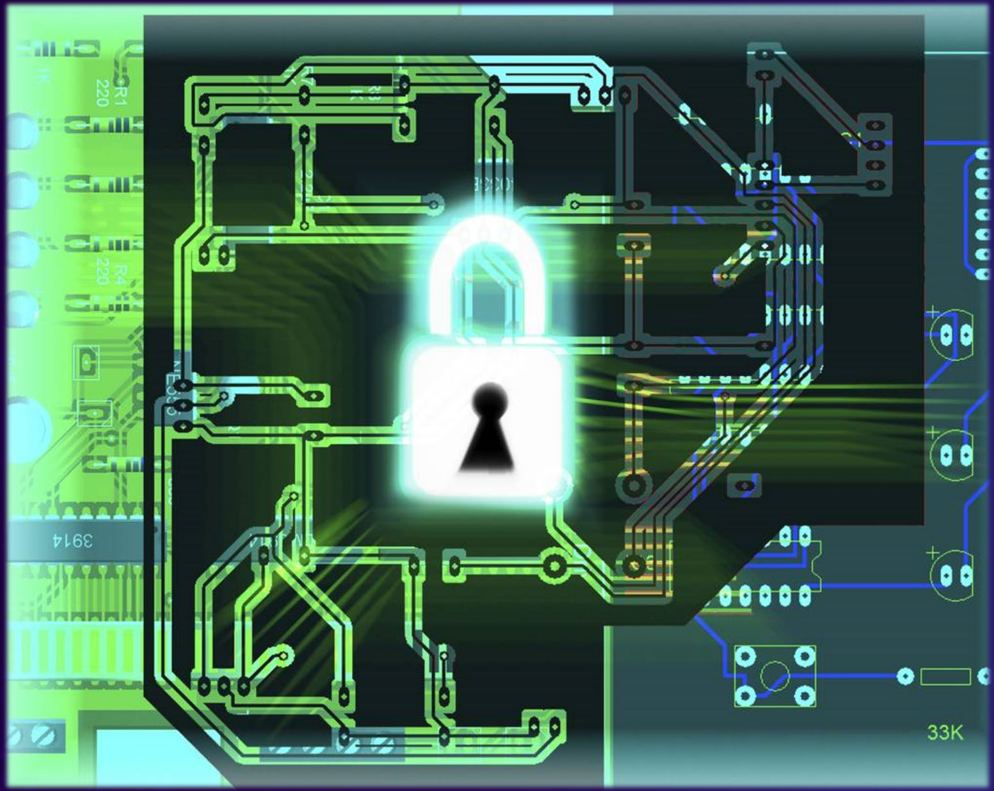
Real-Time Machine Learning (RTML) program

Source: NVIDIA

Trusted components and verification tools for efficient design of complex chips

Posh Open-Source Hardware (POSH) program

Overcoming security threats across the entire hardware lifecycle



Source: federaltimes.com

Security-conscious design for integrated circuits

Automatic Implementation of Secure Silicon (AISS) program

Compartmentalize software systems to prevent initial penetrations

Compartmentalization and Privilege Management (CPM) program

Accelerators to enable fully homomorphic encryption

Data Protection in Virtual Environments (DPRIVE) program

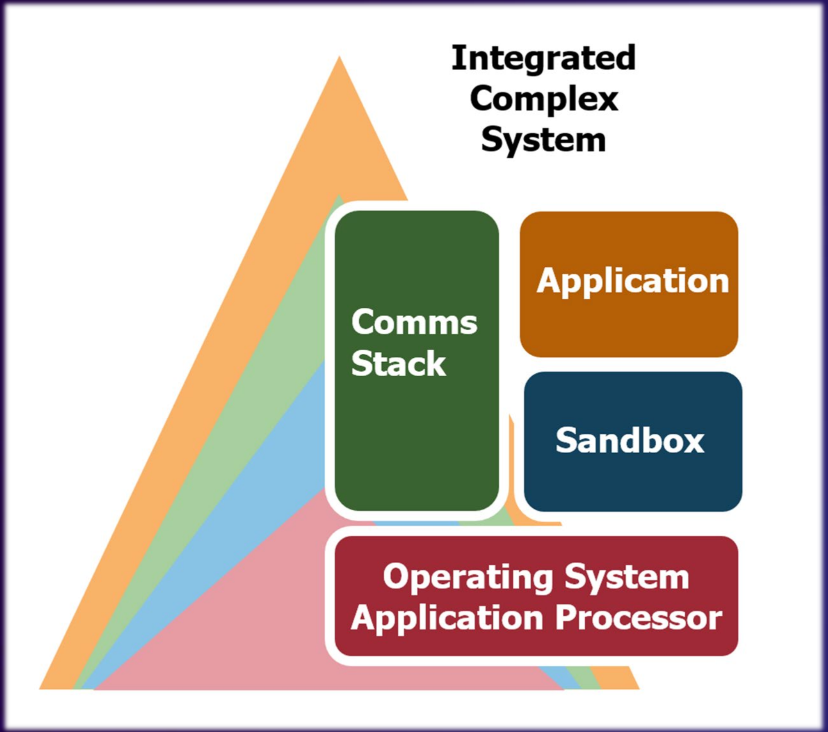
Automated and scalable cyber-physical analysis of systems

Faithful Integrated Reverse-engineering and Exploitation (FIRE) program

Source: networkworld.com

Architectures for provable privacy and security

Guaranteed Architecture for Physical Security (GAPS) program



Source: DARPA

Generate exploit chains to enable offensive and defensive cyber operations

Intelligent Generation of Tools for Security (INGOTS) program

Source: DARPA

Hardware security architectures that are secure, scalable, and adaptable

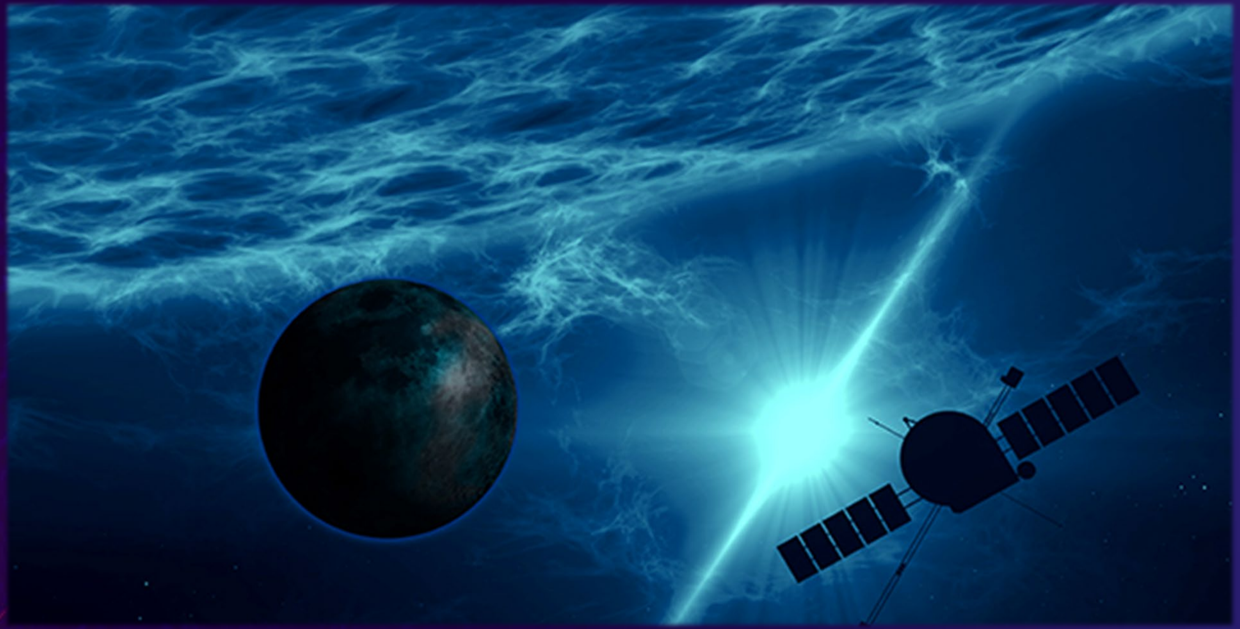
System Security Through Hardware and Firmware (SSITH) program

Developing electronics for extreme environments

Source: DARPA

Extreme high-temperature sensors for high performance

High Operational Temperature Sensors (HOTS) program

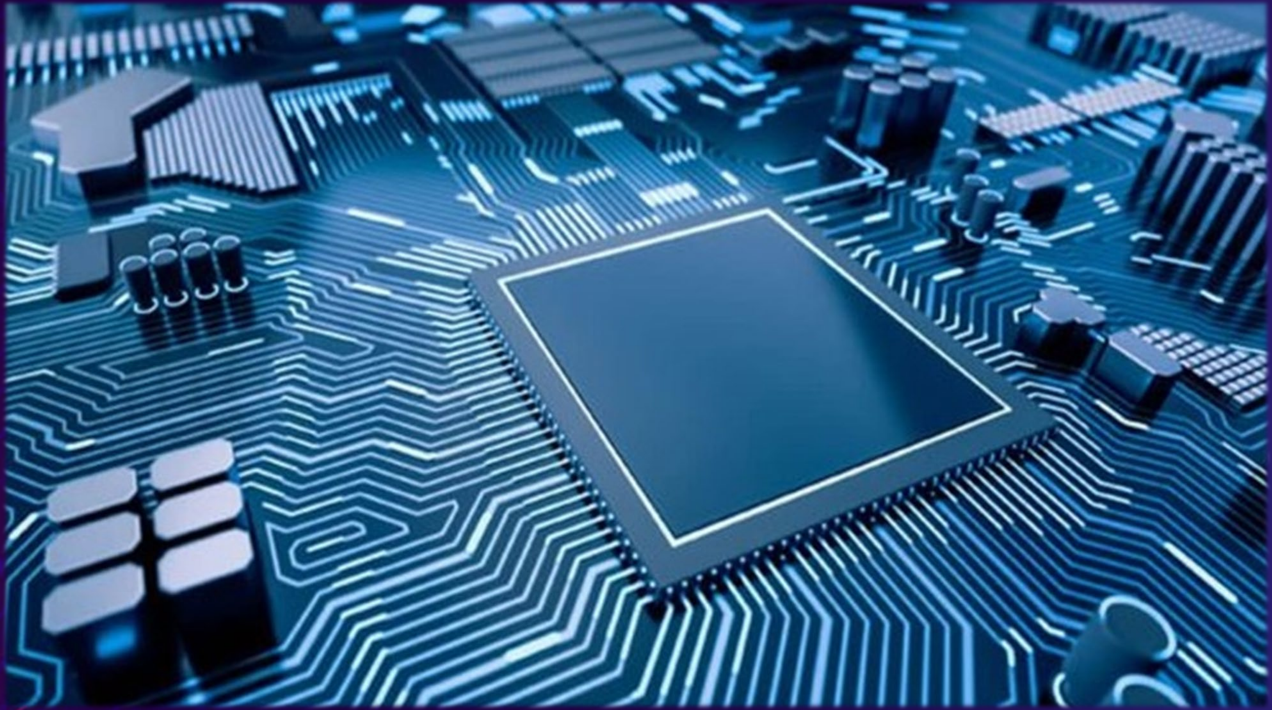


Source: DARPA

Radiation-tolerant switches for low size, weight, and power space payloads

Space Power Conversion Electronics (SPCE) program

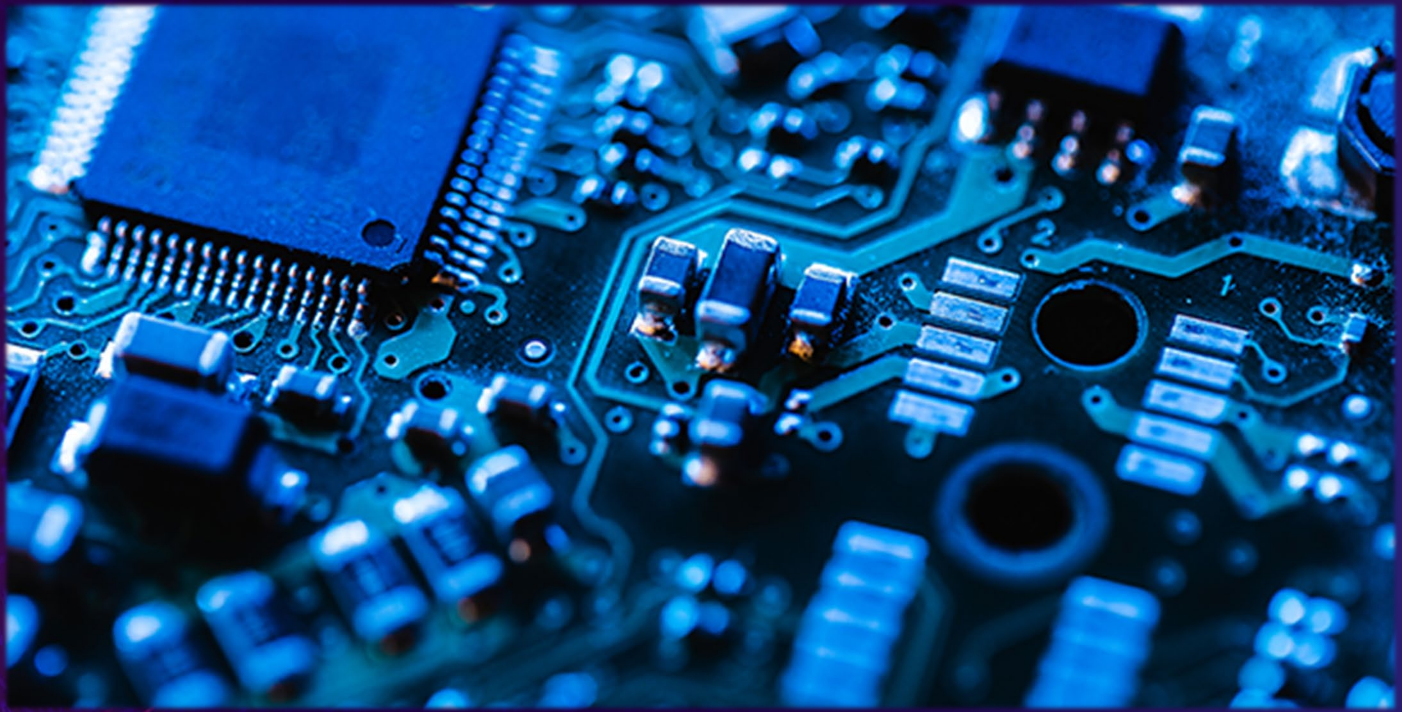
Increasing information processing efficiency at the edge



Source: mytechmag.com

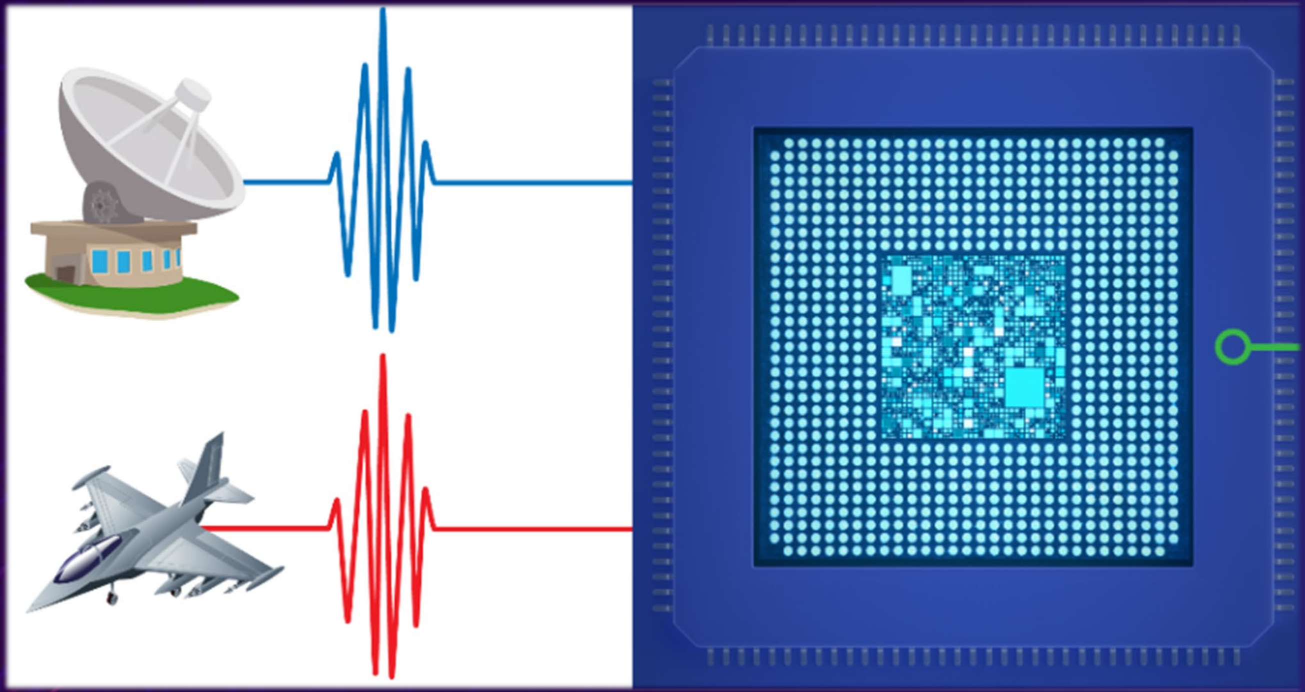
Power- and cost-efficient domain-specific heterogeneous compute architectures

Domain-Specific System-on-Chip (DSSoC) program



Cryogenic operation to enable high-performance computing at reduced power

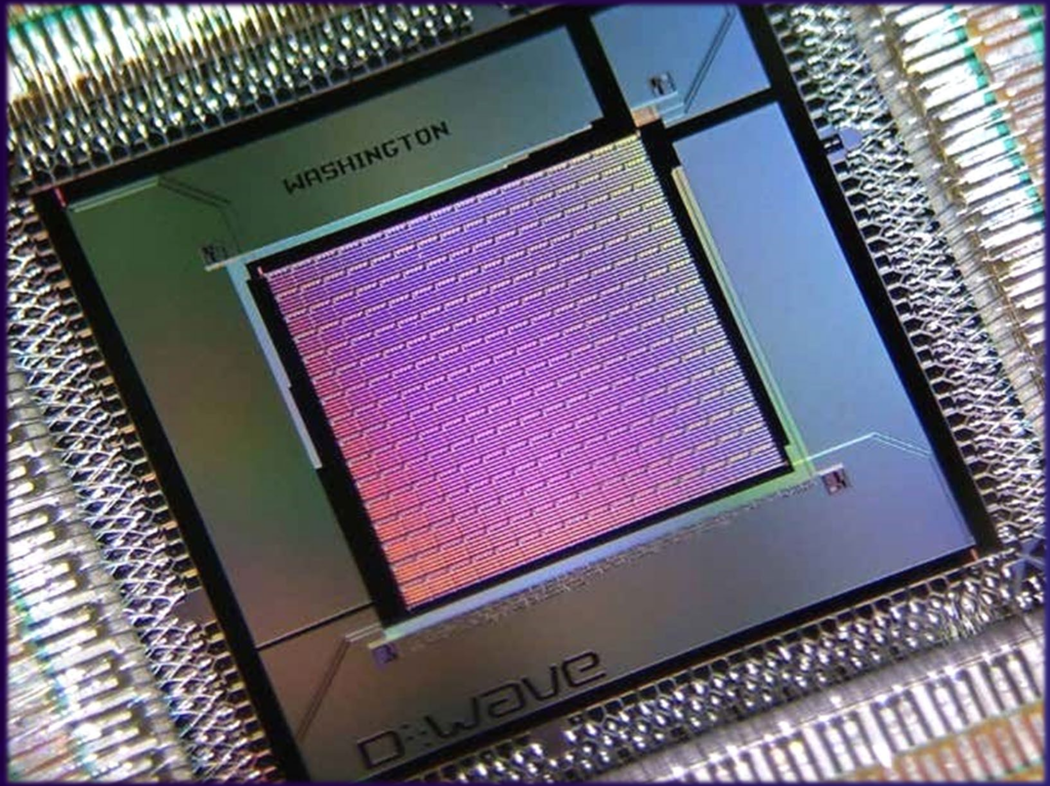
Low Temperature Logic Technology (LTLT) program



Source: DARPA

Power-efficient correlators for signal processing

Massive Cross Correlation (MAX) program



Source: D-Wave

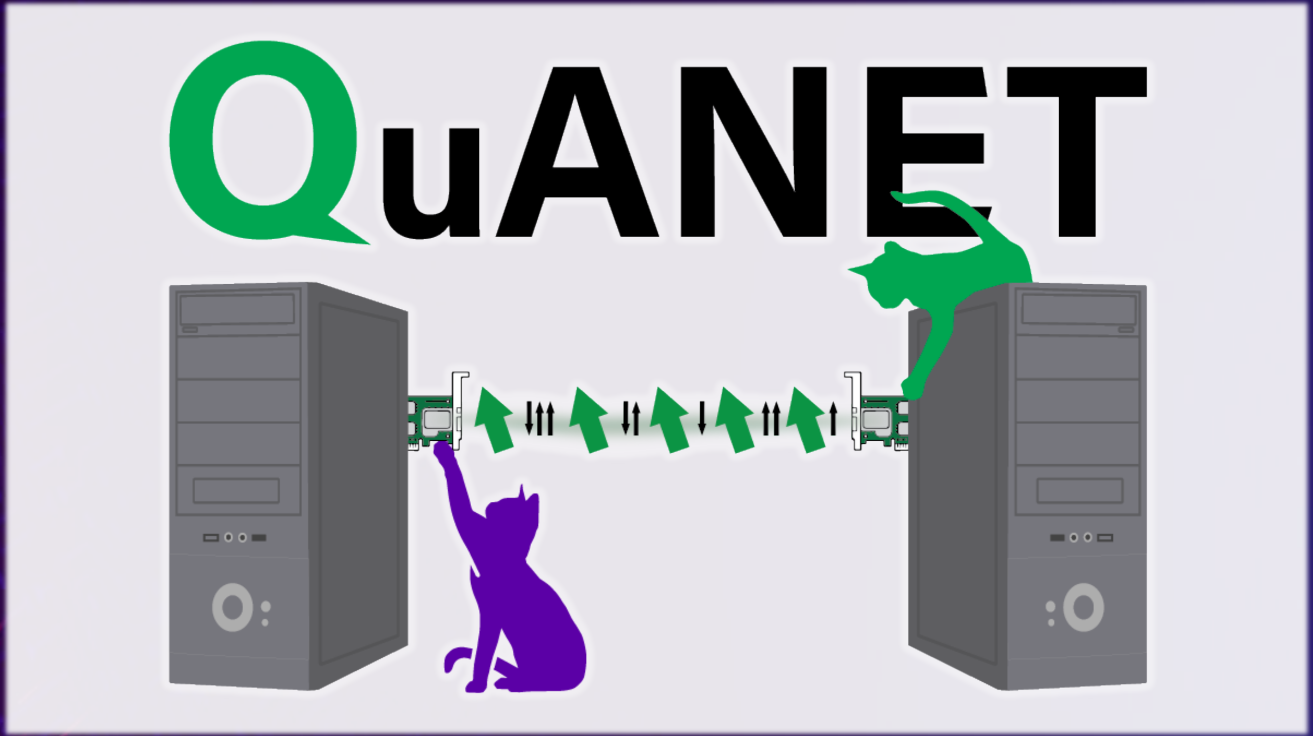
Computational approaches to minimize energy

Quantum-Inspired Classical Computing (QuICC) program

Source: Wikimedia Commons "Social Network Analysis Visualization" Martin Grandjean CC BY-SA 3.0

Fast, small, random, global memory access across a flat, low-latency network

Hierarchical Identify Verify Exploit (HIVE) program



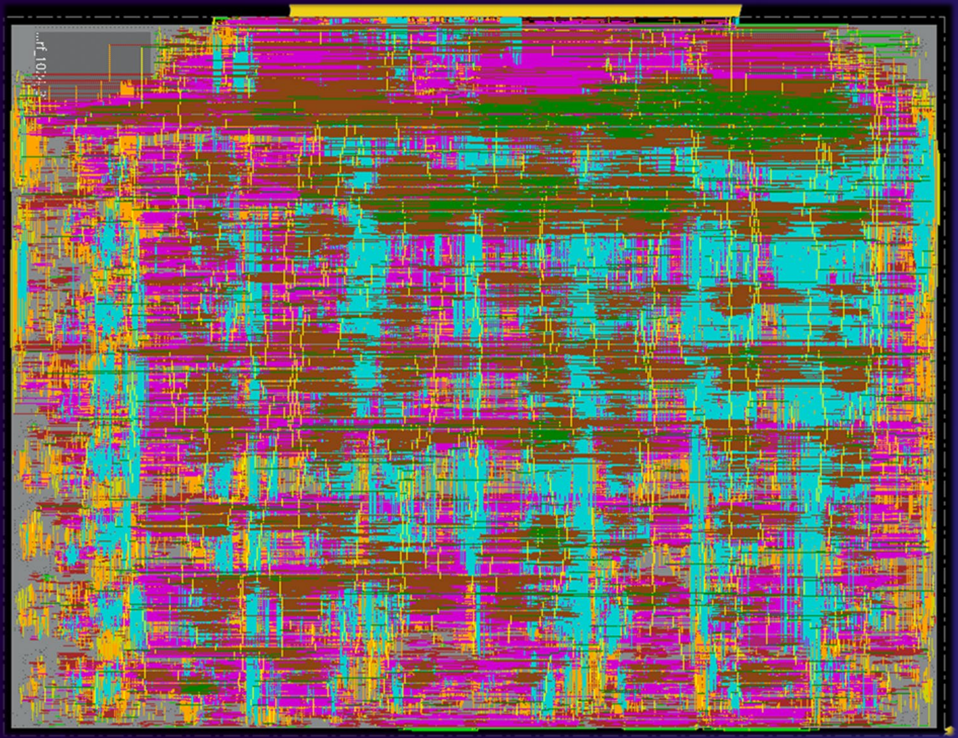
Hybrid quantum-classical communication networks

Quantum-Augmented Network (QuANET) program

Structured ASICs with reconfigurability and near-ASIC performance

Structured Array Hardware for Automatically Realized Applications (SAHARA) program

ASIC: Application-specific integrated circuit

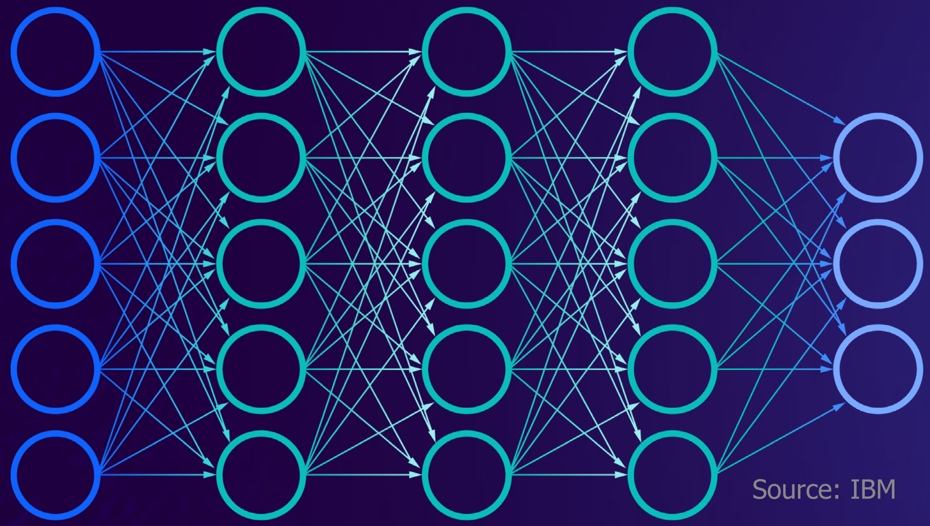


Reconfigurable HW architectures and supporting SW development

Software-Defined Hardware (SDH) program

HW/SW: Hardware/software

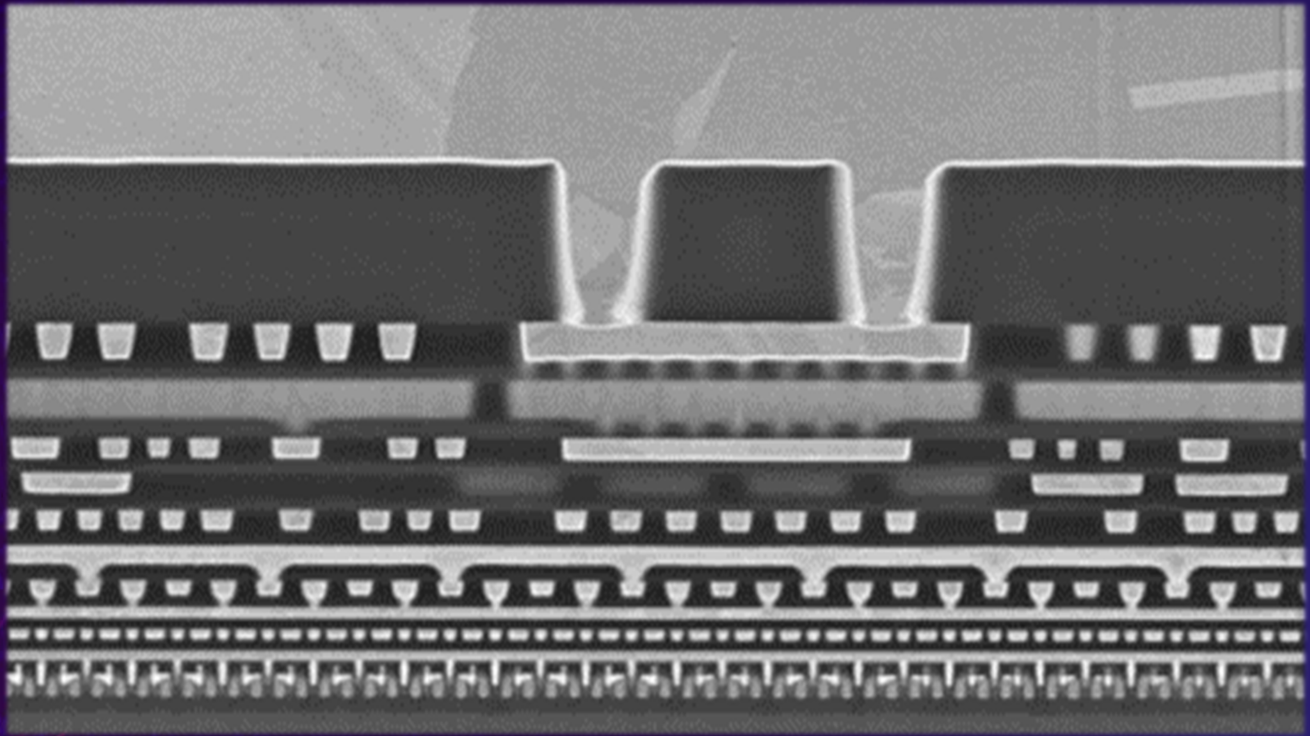
Accelerating innovation in artificial intelligence hardware



Source: IBM

Enable confidence in machine learning for mission relevant problems

Enabling Confidence (EC) program



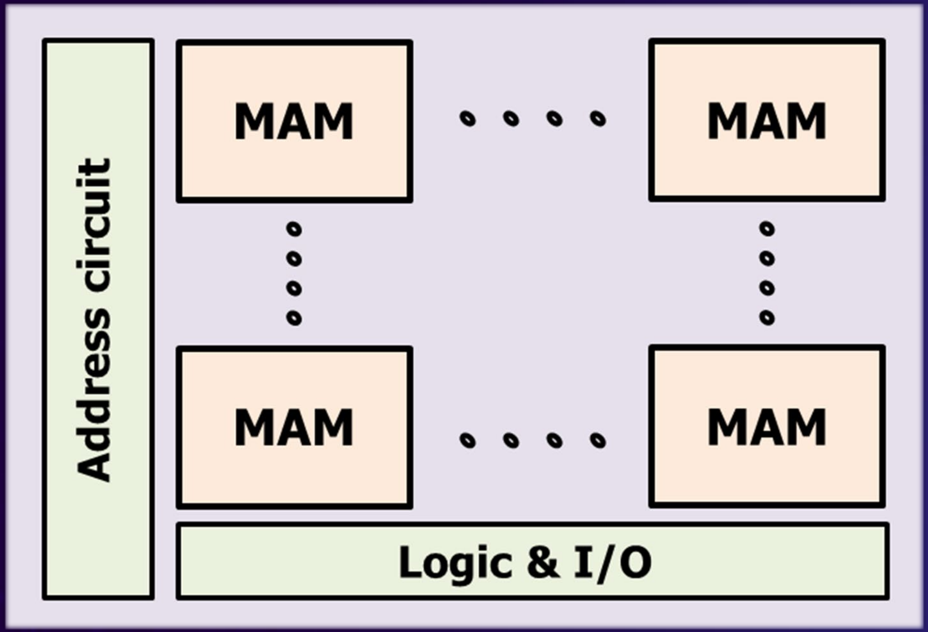
New materials for compute-in-memory

Foundations Required for Novel Compute (FRANC) program

Source: tripwire.com

Applying bio-inspired AI at the pixel level

In-Pixel Intelligent Processing (IP2) program



Source: DARPA

Fast, compact, power-efficient, and scalable compute-in-memory accelerator

Optimum Processing Technology Inside Memory Array (OPTIMA) program

Securing communications

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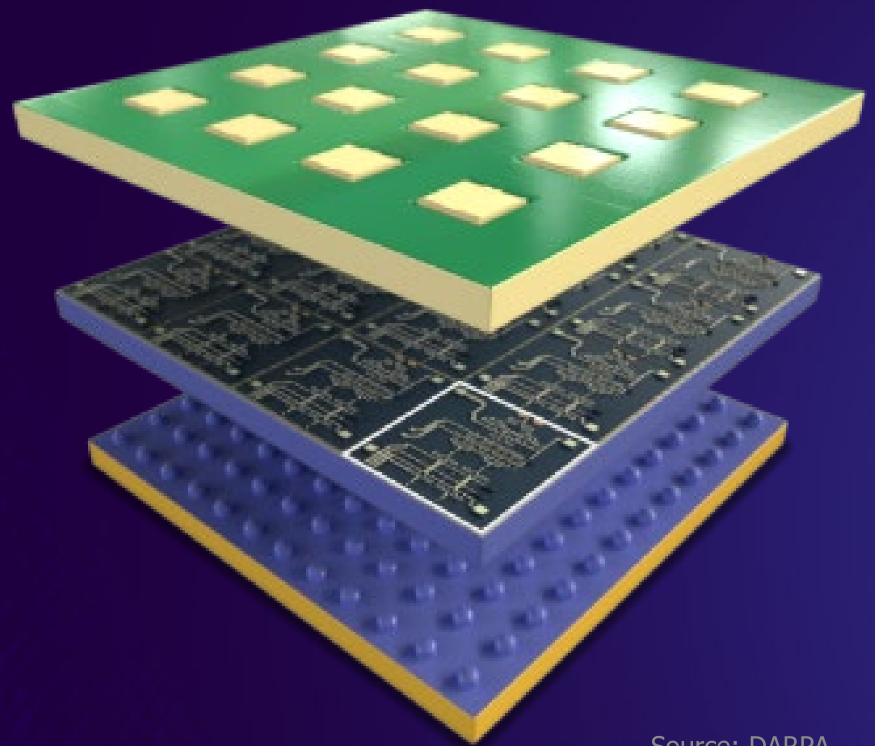
Source: DARPA

Compact radio frequency filters for AESA resilience to interference

COmpact Front-end Filters at the ElEment-level (COFFEE) program

AESA: Active electronically scanned array



Source: DARPA

High-frequency millimeter wave arrays achieved by 3D heterogeneous integration

Electronics for G-band Arrays (ELGAR) program

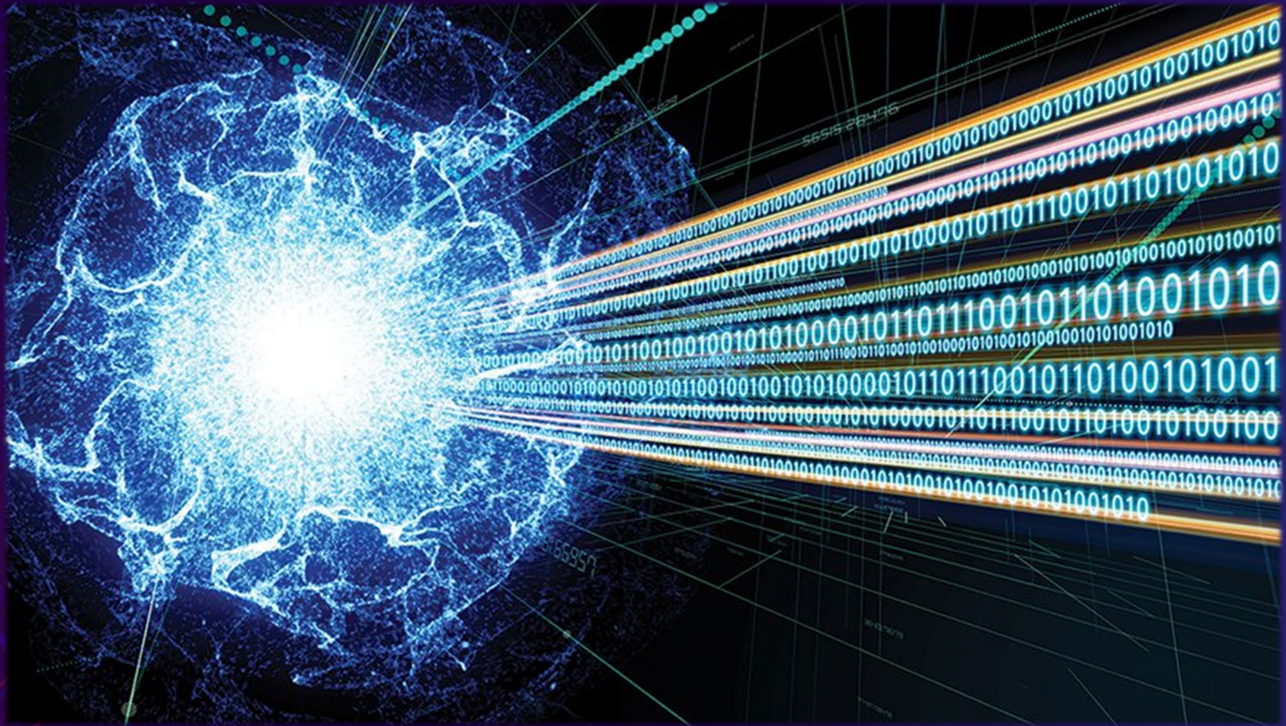
Source: DARPA

Extremely low-noise radio frequency synthesizer achieved with photonics

Generating Radio Frequency with Photonic Oscillators for Low Noise (GRYPHON) program

Element-level millimeter wave, multi-beam digital phased arrays

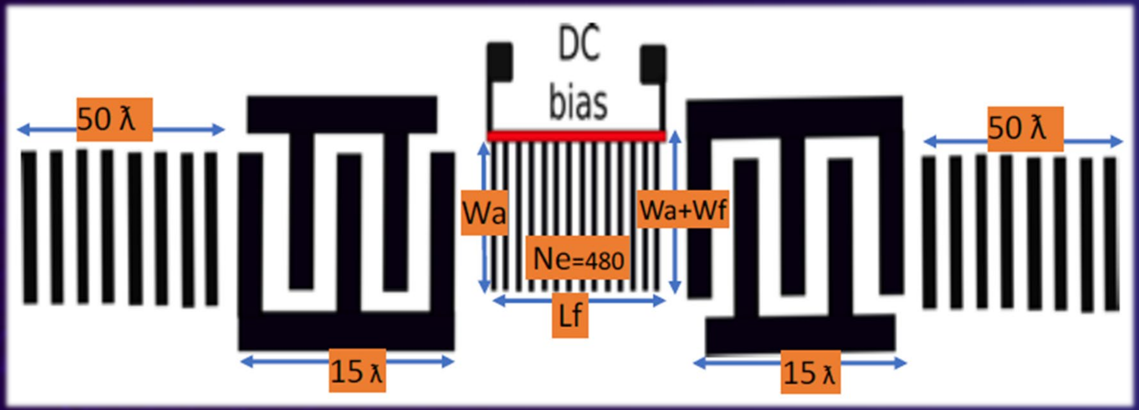
Millimeter Wave Digital Arrays (MIDAS) program



Source: army.mil

Radio frequency sensing using quantum states of atoms

Quantum Apertures (QA) program



Traveling-wave amplification in solid state structures

Traveling-wave Energy Enhancement Devices (TWEED) program

Source: DARPA

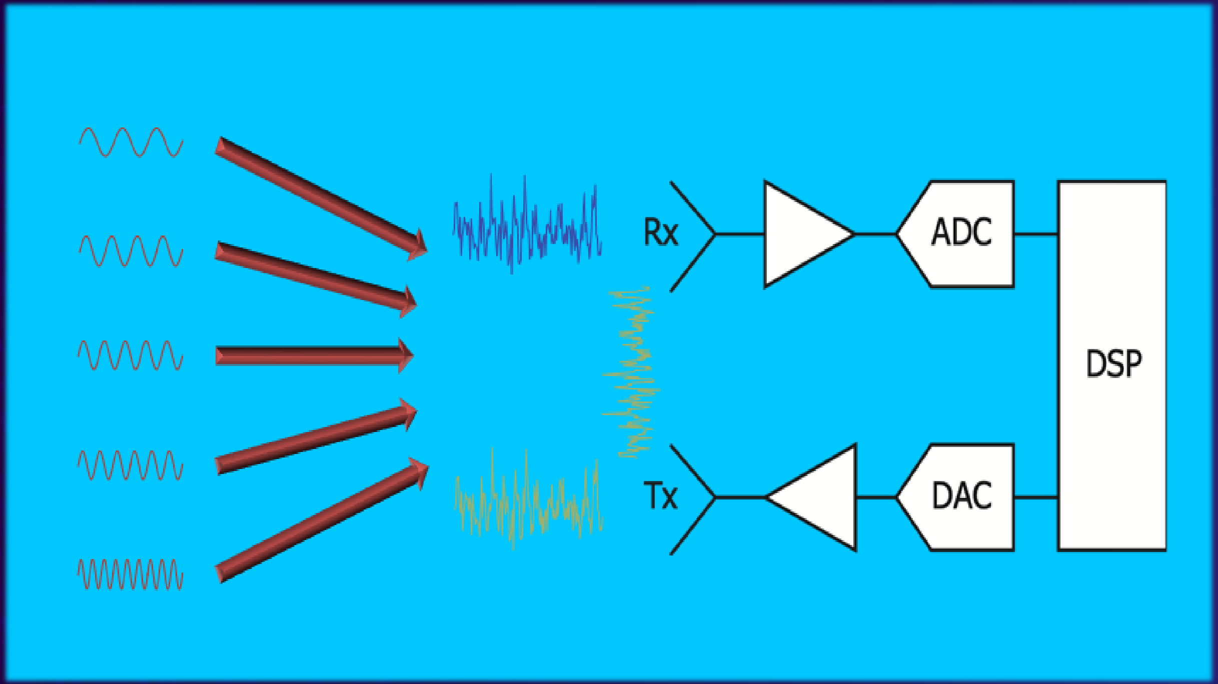
Optical apertures that receive signals from any direction

Steerable Optical Aperture Receivers (SOAR) program

Source: DARPA

Secure comms through spectral, temporal, and spatial diversity

Wideband Secure and Protected Emitter and Receiver (WiSPER) program



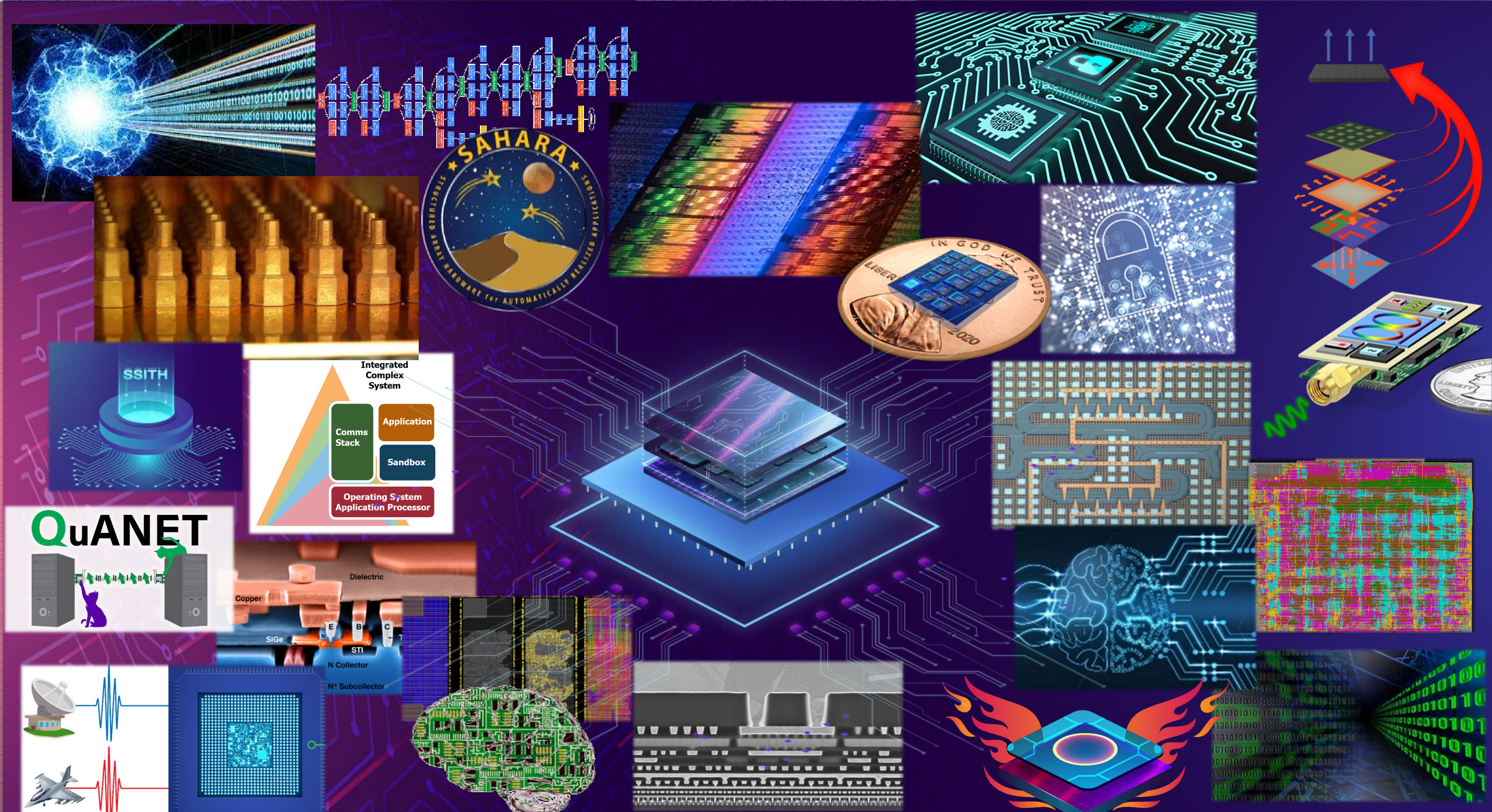
Source: DARPA

Adaptive embedded control for jamming and co-site mitigation

Wideband Adaptive Radio Frequency Protection (WARP) program

Source: DARPA

Source: DARPA



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