# Challenges and Opportunities in 3DIC Test

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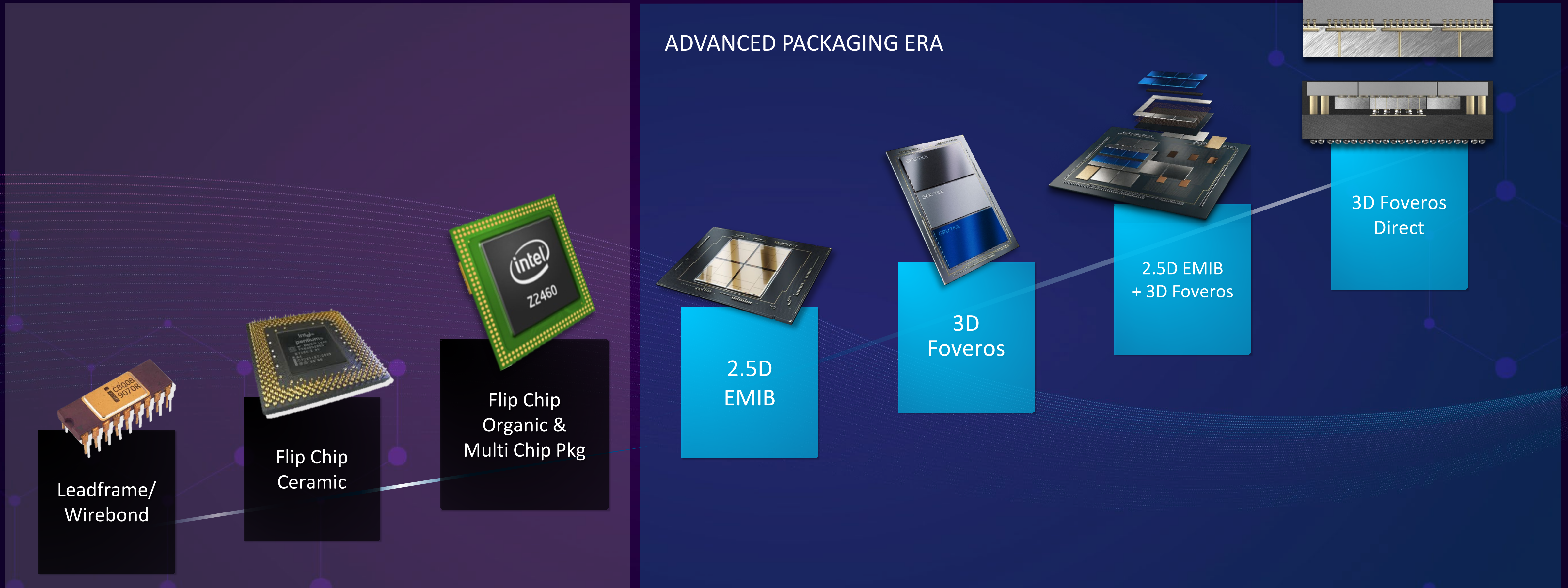
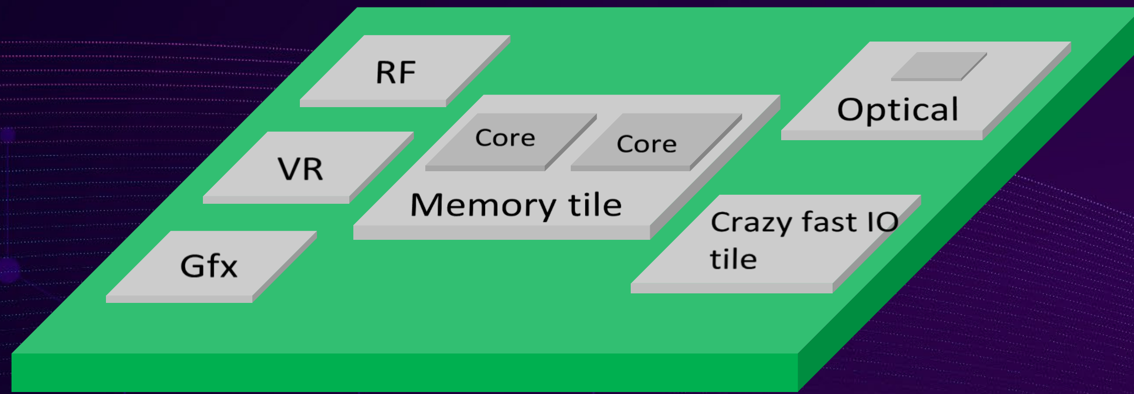



**3DIC (done correctly) will enable higher performance at a lower cost**

3DIC is here to stay…

…but if you can’t test it, you don’t have a product

# 3DIC Test Challenges: Test Cost



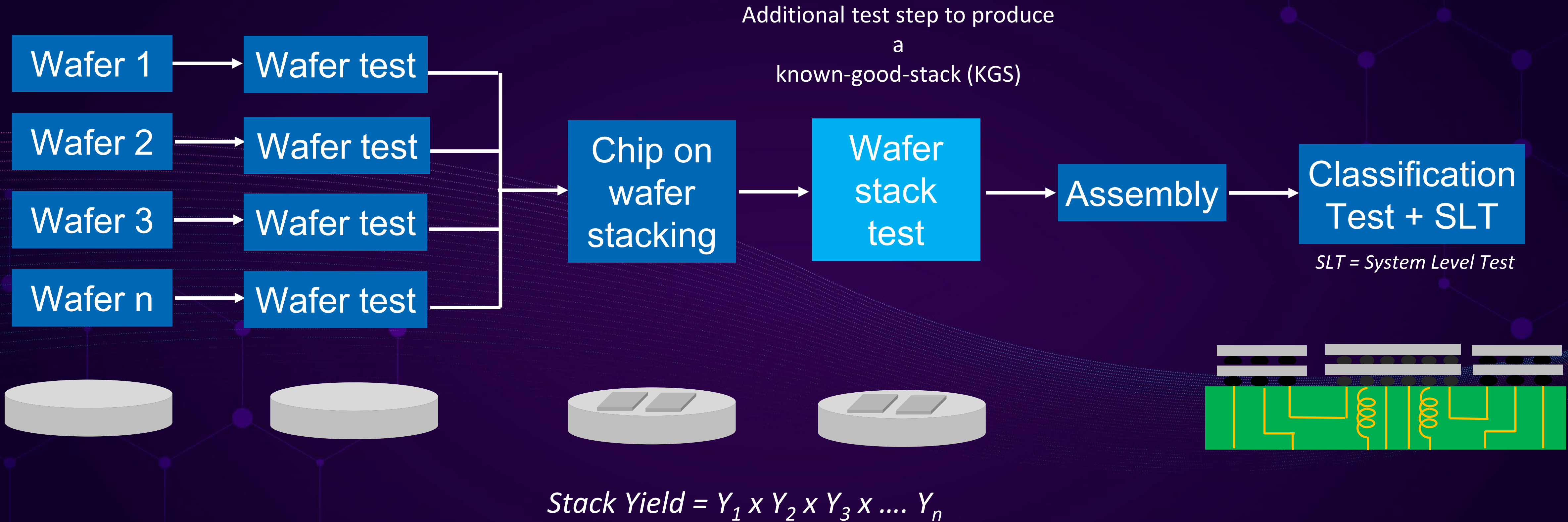

*Test strategy?*

- *Multiple* sockets on specialized ATE* to test each IP separately?
- *Single* socket on a big iron ATE that can test everything?
- Higher reliance on system level test with long test times?

**As 3DIC devices begin to resemble a system, new strategies and solutions are needed to test these products in a cost-effective manner**

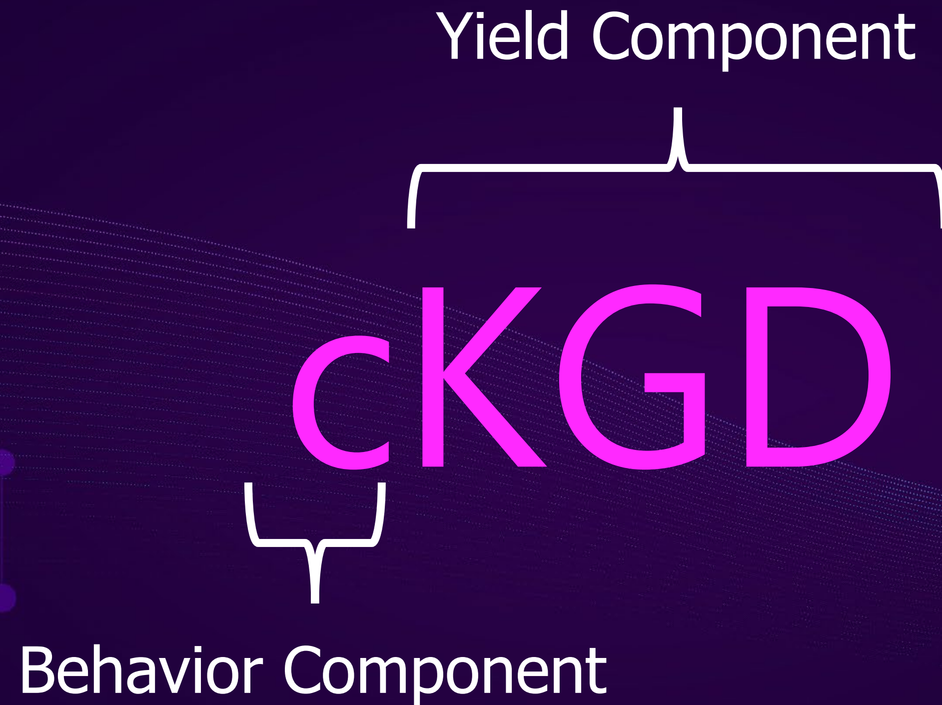
**ATE = Automated Test Equipment*

# 3DIC Test Challenges: cKGD



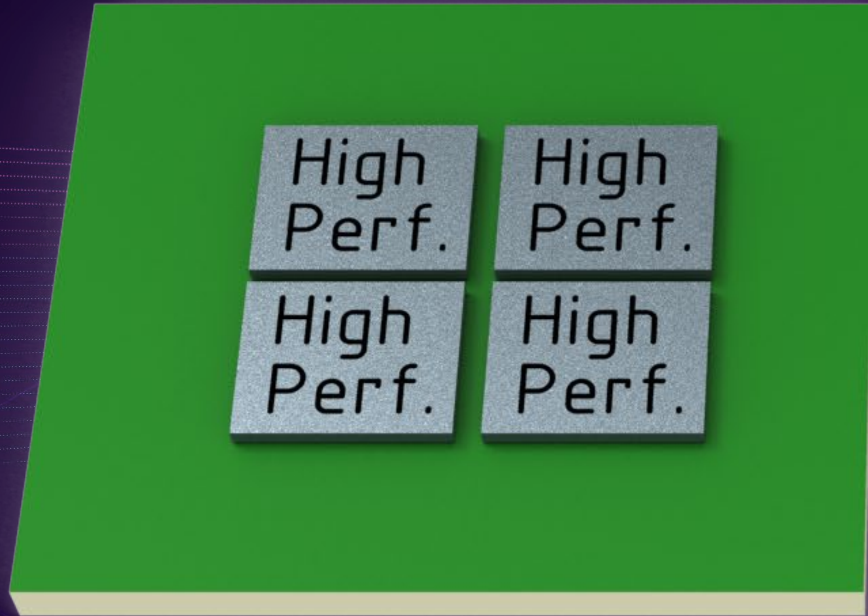

**Characterized Known-Good-Die (cKGD) out of wafer test is critical to making disaggregation and heterogeneous integration successful**

# What is cKGD?

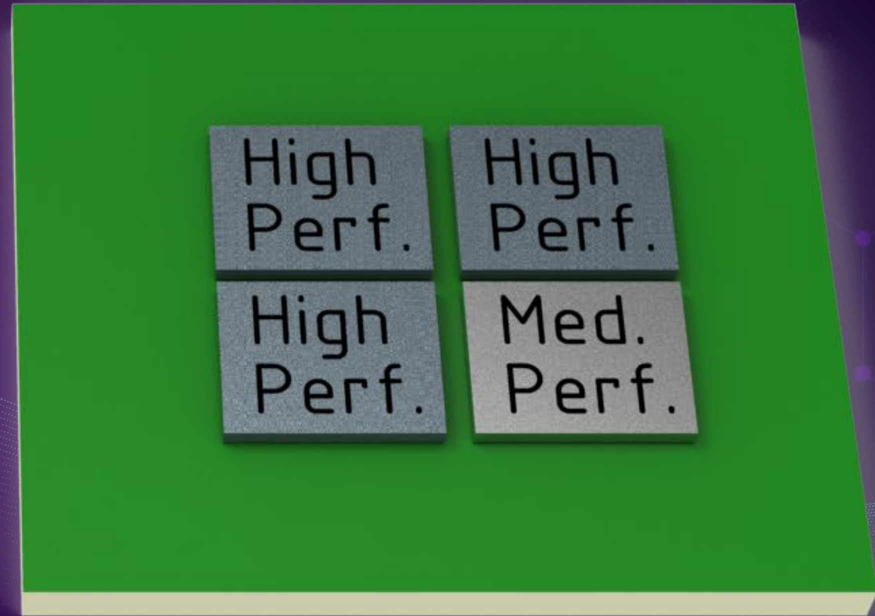



**Wafer test needs to not only catch defects, but also provide an accurate assessment of device behavior for optimal packaging decisions**

# Importance of Characterization




Shipped as high performing part

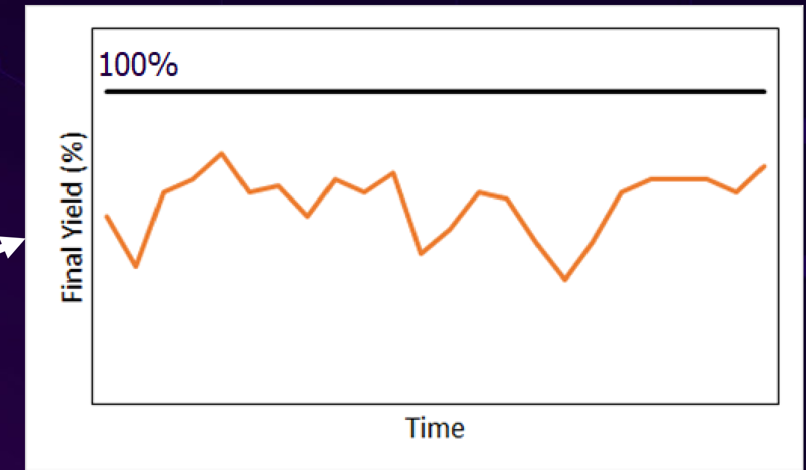



Shipped as medium performing part

**Characterization of device behavior/performance and intelligent pairing is needed to maximize performance**

# cKGD Challenges

Typical final yield for a 3DIC




Despite best efforts to produce KGD out of wafer test, there are still a significant number of defects that are being caught at package test

cKGD

**Silent Data Corruptions at Scale**

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ABSTRACT

Silent Data Corruption (SDC) can have negative impact on large-scale infrastructure services. SDCs are not captured by error reporting mechanisms within a Central Processing Unit (CPU) and hence are not traceable at the hardware level. However, the data corruptions propagate across the stack and manifest as application-level problems. These types of errors can result in data loss and can require months of debug engineering time.

In this paper, we describe common defect types observed in silicon manufacturing that leads to SDCs. We discuss a real-world

machine learning inferences, ranking and recommendation systems. However, it is our observation that computations are not always *accurate*. In some cases, the CPU can perform computations incorrectly. For example, when you perform 2x3, the CPU may give a result of 5 instead of 6 silently under certain microarchitectural conditions, without an indication of the miscomputation in system event or error logs. As a result, a service utilizing the CPU is potentially unaware of the computational accuracy and keeps consuming the incorrect values in the application. This paper predominantly focuses on scenarios where datacenter CPUs exhibit such silent data

**Cores that don't count**

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Abstract

We are accustomed to thinking of computers as fail-stop, especially the cores that execute instructions, and most system software implicitly relies on that assumption. During most of the VLSI era, processors that passed manufacturing tests and were operated within specifications have insulated us from this fiction. As fabrication pushes towards smaller feature sizes and more elaborate computational structures, and as increasingly specialized instruction-silicon pairings are intro-

*MI, USA*. ACM, New York, NY, USA, 8 pages. https://doi.org/10.1145/3458336.3465297

1 Introduction

Imagine you are running a massive-scale data-analysis pipeline in production, and one day it starts to give you wrong answers – somewhere in the pipeline, a class of computations are yielding corrupt results. Investigation fingers a surprising cause: an innocuous change to a low-level library. The change itself was

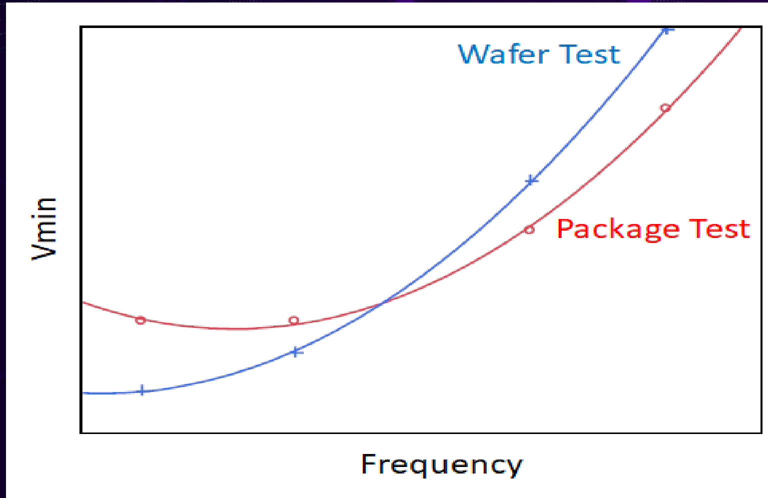
Even package level test has challenges catching all defects due to differences in the test vs use environment

**Defects are getting harder to catch and test methods are not keeping pace**

# cKGD Challenges

| | Wafer Test | Package Test |
|---|---|---|
| Thermal | Cold/warm, passive cooling | Hot, active cooling |
| Electrical | No package, limited connectivity | Package, full connectivity |
| Mechanical | No package, flat die | Package, warped die |

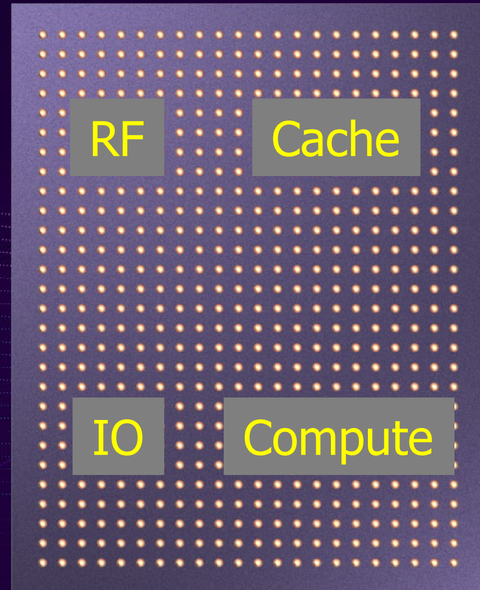
cKGD



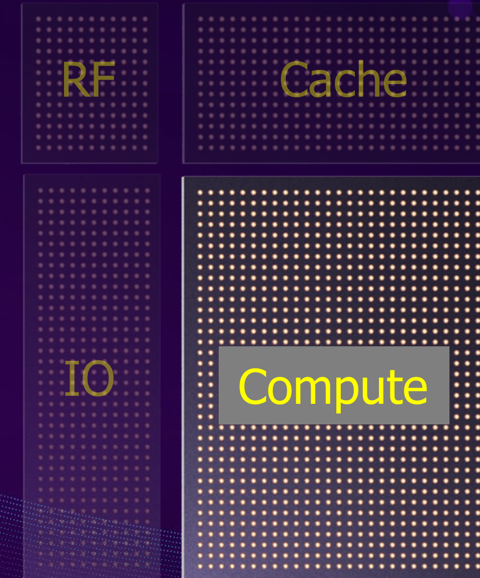

Device performance shifts due to differences in the wafer test vs backend test environment

**Differences in wafer test vs backend test environment present challenges in properly characterizing die**

# Characterization Challenges




All functional blocks are present during wafer test




Functional blocks are distributed and not present during wafer test

**Need methods for effective testing and characterization of disaggregated chiplets that don’t have all the functional blocks available during wafer test**

# Summary

- 3DIC is here to stay, but if you can't test it, you don't have a product
- Generating a characterized known good die (cKGD) is key to a successful 3DIC production strategy
- More testing is not the answer – there is a need for better coverage, resiliency, and repair

**CALL TO ACTION: need more funding and focus to drive innovation in design, DFT, and test methods to solve the challenges with 3DIC test in a cost-effective manner**