ERI Summit 2019

ELECTRONICS RESURGENCE INITIATIVE

Collaboratively innovating the 4th wave of electronics development

Hosted by DARPA's
Microsystems Technology Office

Detroit, MI
July 15-17, 2019

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To the Electronics Resurgence Initiative Community –

Welcome to the 2019 Electronics Resurgence Initiative (ERI) Summit.

Two years ago, DARPA's Microsystems Technology Office (MTO) launched ERI as a bold response to critical emerging trends. These included the rapid increase in the cost and complexity of advanced microelectronics design and manufacture, which has challenged Gordon Moore's economic premise that technology would lower costs and shorten turnaround times. Another trend is the limited availability of leading-edge electronics for the DoD, a result of cost-driven foundry consolidation. Meanwhile, non-market foreign forces are working to shift the electronics innovation engine overseas, challenging U.S. economic and security advantages. In addition, the nation is gaining a new appreciation for electronics security—a longtime defense concern—following publicized challenges to our digital backbone in areas as diverse as automobiles, cybersecurity, and voting.

In ERI, we have envisioned a unified national response, marked by research collaborations between DARPA, the defense community, academia, and the commercial sector.

There is strong historical precedent to suggest the viability of this approach. Each wave of modern electronics development has benefitted from the combination of defense-funded academic research and commercial sector investment. In the 1980s, when geometric scaling started to make low-volume integrated circuit fabrication unaffordable, DARPA's investment in the Metal Oxide Silicon Implementation Service (MOSIS) opened the door to rapid, low-cost chip manufacture, laying the foundation for the nation's world-leading fabless design industry. In the 1990's, a combination of defense, academic, and commercial partners pioneered 193 nm lithography, which has become the industry critical fabrication process over the past two decades. Then, as Dennard scaling ended in the 2000's, the semiconductor industry adopted Fin Field Effect Transistors (FinFETs), another DARPA-funded innovation that drove low power computing and kicked off an era of 3D devices.

Today, I believe the nation stands ready to innovate a 4th wave of electronics progress. The state of the industry indicates that the 4th wave will be characterized by three-dimensional heterogeneous integration. Through integration, innovators will add new materials and devices to the silicon foundation, enabling intelligence and specialized functions precisely designed to meet the diversifying needs of the commercial and defense sectors. 3D heterogeneous integration will demand new architectures and design tools, developed to manage the complexity of working in three dimensions while enabling rapid system upgrades and integrating security as a primary design concern. The 4th wave, however, is neither inevitable nor inevitably beneficial to the United States. Results from the nascent Electronics Resurgence Initiative point to U.S. leadership opportunities; the ERI Summit will highlight several successes. Even so, our collective challenge will be to ensure that benefits differentially accrue to the U.S. commercial and defense base, which is aggressively investing in continued progress.

The need for this advancement is clear. Both the defense and commercial sectors face a world defined by the rapid rise of devices operating at "the edge," by the glut of information those devices will collect, and by the growing cyber-driven threats those devices will encounter. To overcome the challenges of increased cost and new non-market foreign forces, 4th wave innovations must successfully transition into the domestic industrial base. To meet our national security needs, 4thwave technologies must enable more capable systems that process data locally, extract actionable information, and make decisions at the edge. To address new security concerns, 4th wave technologies must integrate security considerations into microsystem design in a way that is both effective and easy to implement.

The 2019 ERI Summit is designed to advance these objectives. For the first two days, leaders from across the electronics community will share their visions for the future and the challenges to be met, followed by solution-oriented and technical updates from ERI performers. The third day of the Summit will give attendees the opportunity to gain further insight into several ongoing ERI programs and to provide input into the future of DARPA investment. I look forward to sharing our progress with you and to shaping the 4th wave of electronics innovation, together.

Dr. Mark Rosker
Director, Microsystems Technology Office
Defense Advanced Research Projects Agency

DARPA Electronics Resurgence Initiative

Announced in June 2017, the Defense Advanced Research Projects Agency (DARPA) Electronics Resurgence Initiative (ERI) is a five-year, upwards of $1.5 billion investment in the future of domestic, U.S. government, and defense electronics systems. ERI is forging forward-looking collaborations to enable microelectronics progress through circuit specialization and to ensure secure DoD access to next-generation electronics technologies.

ERI currently encompasses 20 programs—organized into four thrusts—managed by 12 program managers. The 3D heterogeneous integration thrust is enabling tight incorporation of differing circuit components, including through the development of the first state of the art electrical interface standard supported by an open source reference design. The novel materials and devices thrust is delivering new materials technologies to the domestic manufacturing base, demonstrating the first commercial manufacture of resistive RAM devices integrated with carbon nanotube transistors in a silicon compatible process. The design and security thrust is accelerating delivery of specialized circuitry and creating new opportunities for the safe use of open-source IP, recently showing that unknown chip design flaws can be rapidly located. The specialization thrust is optimizing systems for commercial and defense functions, such as driving towards ASIC-level performance in runtime programmable processors. Building on the tradition of successful government-industry partnerships, these and other ERI programs will enable the United States to collaboratively innovate a 4th wave of microelectronics progress and to create a more specialized, secure, and heavily automated electronics industry that meets national defense and commercial needs.

Dr. Mark Rosker
Director, MTO

Dr. Jay Lewis
Deputy Director, MTO

Mr. Richard-Duane Chambers
ERI Special Assistant

Program Managers

Dr. Young-Kai Chen
Foundations Required for Novel Compute (FRANC)
Technologies for Mixed-mode Ultra Scaled Integrated Circuits (T-MUSIC)

Dr. Benjamin Griffin
Near Zero Power RF and Sensor Operations (N-ZERO)

Dr. Timothy Hancock
Millimeter Wave Digital Arrays (MIDAS)

Dr. Gordon Keeler
Modular Optical Apertures Building Blocks (MOABB)
Photonics in the Package for Extreme Scalability (PIPES)

Mr. Serge Leef
Automatic Implementation of Secure Silicon (AISS)

Mr. Andreas Olofsson
Posh Open Source Hardware (POSH)
Intelligent Design of Electronic Assets (IDEA)
Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)

Dr. Ken Plaks
Obfuscated Manufacturing for GPS (OMG)

Dr. Tom Rondeau
Domain-Specific System on Chip (DSSOC)

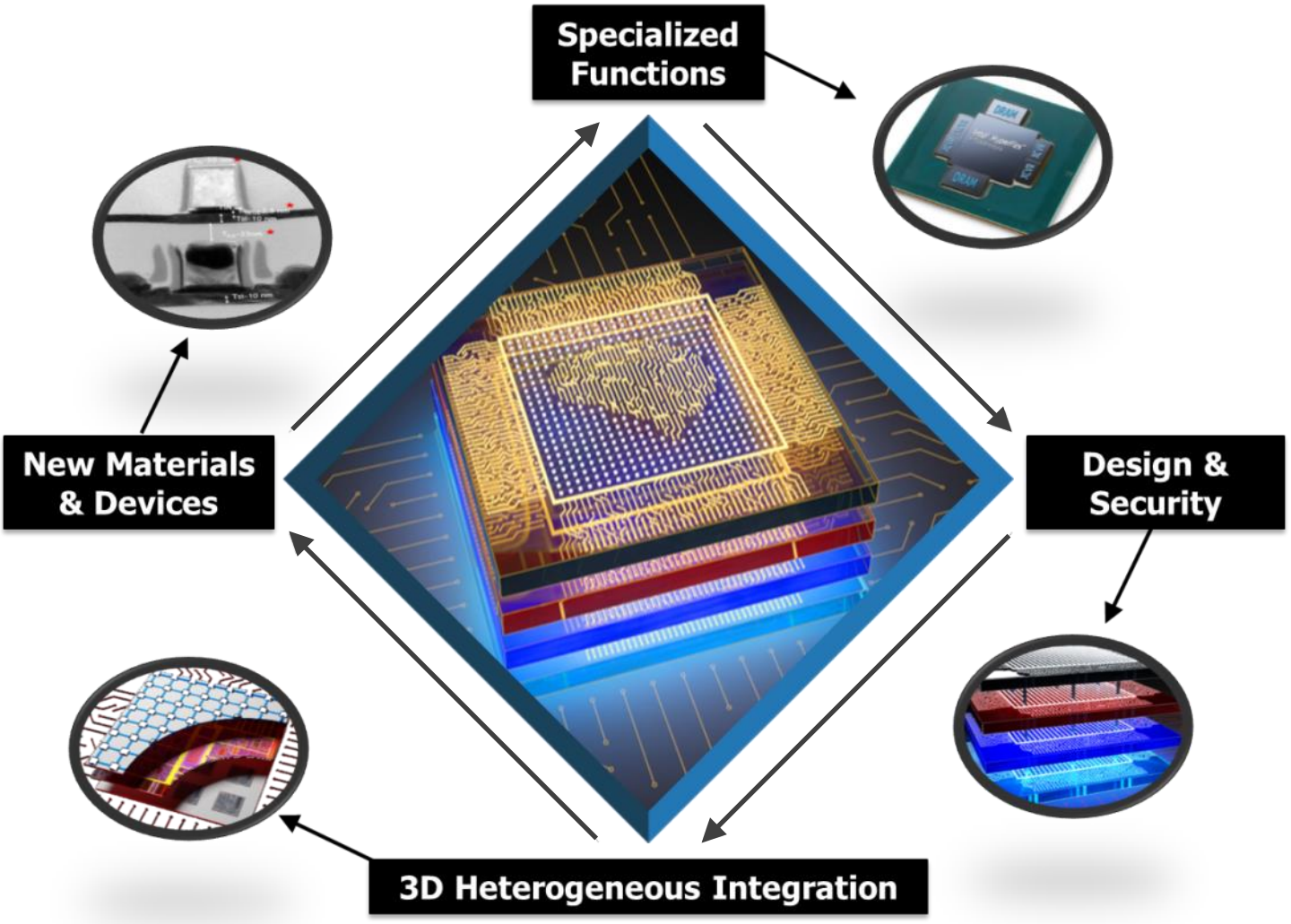
Dr. Linton Salmon
Three Dimensional Monolithic System-on-a-Chip (3DSoC)
System Security Integration Through Hardware and Firmware (SSITH)
Circuit Realization at Faster Timescales (CRAFT)
Joint University Microelectronics Program (JUMP)

Dr. Hava Siegelmann
Lifelong Learning Machines (L2M)

Mr. Wade Shen
Hierarchical Identify Verify Exploit (HIVE)
Software Defined Hardware (SDH)

Mr. Paul Tilghman
Digital RF Battlespace Emulator (DRBE)

Mr. Walter Weiss
Guaranteed Architecture for Physical Security (GAPS)



3D Heterogeneous Integration

3D heterogeneous integration enables a shift from board and chip-level integration to fine heterogeneous integration

CHIPS: Chips made from the best DoD & commercial IP

MIDAS: Digital millimeter wave phased array tiles

3DSoC: 3D chips for high-performance processing

PIPES: Package-level optical signaling on CMOS

New Materials & Devices

New materials and devices enable a shift from familiar to beyond-CMOS materials

JUMP*: Largest university effort of its kind

FRANC: CHIPS that improve due to new materials

T-MUSIC: Novel mixed-mode devices on CMOS

Specialized Functions

Specialized functions programs enable a shift from microsystems with hand-engineered, pre-set functions to circuits with flexible, defense-specific specialization

HIVE: Chips that traverse large sparse graphs

L2M: Artificial intelligence models that learn from experience

N-ZERO: Chips for ultra-low power operation

DSSoC: Chips that adapt within defined DoD problems

SDH: Chips that adapt to dynamic DoD data streams

DRBE: Real-time emulation of the RF battlespace

RTML: Machine learning hardware that adapts in real time

Design & Security

Design and security programs enable a shift from standard EDA tools to next-generation EDA and designs with built-in security

CRAFT: Chips as easy to create as writing software

SSITH: Chips with inherent security

IDEA: Electronic design automation that learns

POSH: Trustable chips composed of understandable parts

AISS: Security-conscious design for integrated circuits

GAPS: Architectures for provable privacy and security

*JUMP applies to all ERI thrusts.

Monday, July 15, 2019 - The Fillmore & Little Caesars Arena

7:00 AM *Registration / Continental Breakfast / Limited Poster Review*
Located in all Lobby areas

ERI Morning Plenary

9:00 AM ***Welcome and Introductory Remarks***
Dr. Mark Rosker, Director, DARPA Microsystems Technology Office (MTO)

9:20 AM ***The Origins of ERI***
Dr. William Chappell, CTO, Microsoft Azure Global

9:40 AM  ***Opening Plenary Speaker***
Dr. Lisa Su, CEO, AMD

10:20 AM  ***Information Technology Keynote Speaker***
Dr. John Kelly III, Executive Vice President, IBM

10:40 AM *Morning Break*
Refreshments located in all Lobby areas

Whole-of-Government / Multilateral Response

11:00 AM ***An Industry Perspective on Government Action***
Mr. John Neuffer, President, Semiconductor Industry Association

11:10 AM ***The Rest of the Story: Assurance and other DoD Investments***
Dr. Lisa Porter, Deputy Under Secretary of Defense for Research and Engineering

11:30 AM ***Microelectronics Innovation at the Department of Energy***
Dr. Chris Fall, Director of the Office of Science, Department of Energy

11:45 AM ***Real Time Machine Learning (RTML) - DARPA / NSF Collaboration***
Mr. Andreas Olofsson, Program Manager, DARPA MTO
Dr. Sankar Basu, Program Director, National Science Foundation

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12:00 PM *Lunch*
Lunch located in all Lobby areas

National Challenges and Promising Research Responses

1:20 PM ***Making ERI Matter***
Dr. Jay Lewis, Deputy Director, DARPA MTO

1:40 PM ***Secure Systems: Voting***
Dr. Joe Kiniry, Principal Scientist, Galois

Future Technology: System Security Integration through Hardware and Firmware (SSITH)
Dr. Todd Austin, Professor of Electrical Engineering and Computer Science, University of Michigan

2:10 PM ***Space Applications***
Dr. Jesse Mee, Deputy Program Manager, Space Electronics Technology, Air Force Research Laboratory

Future Technology: Domain Specific System on Chip (DSSoC)
Dr. Mark Horowitz, Professor of Electrical Engineering and Computer Science, Stanford University

2:40 PM ***Future of the Cloud***
Mr. Mark Ryland, Director, Office of the CISO, Amazon Web Services (AWS)

Future Technology: Software Defined Hardware (SDH)
Dr. David Wentzlaff, Associate Professor of Electrical Engineering, Princeton University

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3:10 PM ***Afternoon Break***
Refreshments located in all Lobby areas

The Intersection Of Automotive, Electronics, and Automation

3:30 PM ***Automotive Applications***
Dr. Tim Talty, Technical Fellow, General Motors

3:50 PM ***Enabling Robotics and Autonomy within the Army***
Dr. Robert Sadowski, Robotics Senior Research Scientist, U.S. Army Tank Automotive Research, Development and Engineering Center

4:10 PM ***Future Technology: Lifelong Learning Machines***
Dr. Praveen Pilly, Senior Researcher, HRL Laboratories

Innovation

4:30 PM ***From Labs to Impact***
Dr. Rich Uhlig, Managing Director, Intel Labs

4:45 PM ***Revitalizing Hard Tech Innovation***
Dr. Ilan Gur, Executive Director, Cyclotron Road

5:00 PM ***More Moore: Thinking Outside the (Traditional Hardware) Box***
Dr. Partha Ranganathan, Distinguished Engineer, Google

Evening Reception

5:15 PM ***Transition to Biergarten at Little Caesars Arena (3 block walk)***
Summit staff will assist in directing attendees from The Fillmore to Little Caesars Arena

5:30 PM ***Reception at Little Ceasars Arena - Biergarten***
Remarks by Dr. Mark Rosker, Director, DARPA MTO

7:00 PM ***Reception Concludes***

Dinner Options: The following restaurants inside of Little Caesars Arena will be open after the reception: Kid Rock's Made in Detroit, Mike's Pizza Bar, Sports & Social Detroit

Tuesday, July 16, 2019 - Cobo Center

7:00 AM *Registration / Breakfast / Poster Session*
Located in the Ballroom Prefunction Space and Grand Ballroom A

8:20 AM

Opening Plenary Speaker
Mr. Steve Mollenkopf, CEO, Qualcomm Incorporated

9:00 AM ***Hierarchical Identify Verify Exploit (HIVE)***
Mr. Wade Shen, Program Manager, DARPA I2O / MTO
Mr. Peter Wang, Co-Founder & CTO, Anaconda, Inc.

9:20 AM ***Software Defined Hardware (SDH)***
Mr. Wade Shen, Program Manager, DARPA I2O / MTO
Dr. Saman Amarasinghe, Professor of Electrical Engineering and Computer Science, MIT

9:50 AM ***Domain-Specific System on Chip (DSSoC)***
Dr. Tom Rondeau, Program Manager, DARPA MTO
Dr. Sarita Adve, Professor of Computer Science, University of Illinois at Urbana-Champaign

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10:20 AM *Morning Break*
Refreshments located in the Ballroom Prefunction Space

10:40 AM

Foundry Keynote Speaker: GlobalFoundries and a Differentiation Strategy
Dr. Thomas Caulfield, CEO, GlobalFoundries

11:20 AM ***Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)***
Mr. Andreas Olofsson, Program Manager, DARPA MTO
Mr. Sergey Shumarayev, Senior Principal Engineer, Intel

11:40 AM ***Three Dimensional Monolithic System-on-a-Chip (3DSoC)***
Dr. Linton Salmon, Program Manager, DARPA MTO
Dr. Max Shulaker, Assistant Professor of Electrical Engineering and Computer Science, MIT

12:10 PM ***Framework for Novel Compute (FRANC)***
Dr. Young-Kai Chen, Program Manager, DARPA MTO
Dr. Naresh Shanbhag, Professor of Electrical Engineering,
University of Illinois at Urbana-Champaign

12:40 PM *Lunch / Poster Session*
Lunch located in the Ballroom Prefunction Space and Grand Ballroom A

2:20 PM ***Circuit Realization at Faster Timescales (CRAFT)***
Dr. Linton Salmon, Program Manager, DARPA MTO
Dr. Brucek Khailany, Director of ASIC and VLSI Research, NVIDIA

2:40 PM ***Intelligent Design of Electronic Assets (IDEA) & Posh Open Source Hardware (POSH)***

Mr. Andreas Olofsson, Program Manager, DARPA MTO
Mr. Edgar Iglesias, Principal Software Engineer, Xilinx
Dr. Eric Keiter, Technical Staff, Sandia National Laboratories
Dr. Andrew Kahng, Professor of CSE and ECE, University of California San Diego
Dr. Clark Barrett, Associate Professor of Computer Science, Stanford University

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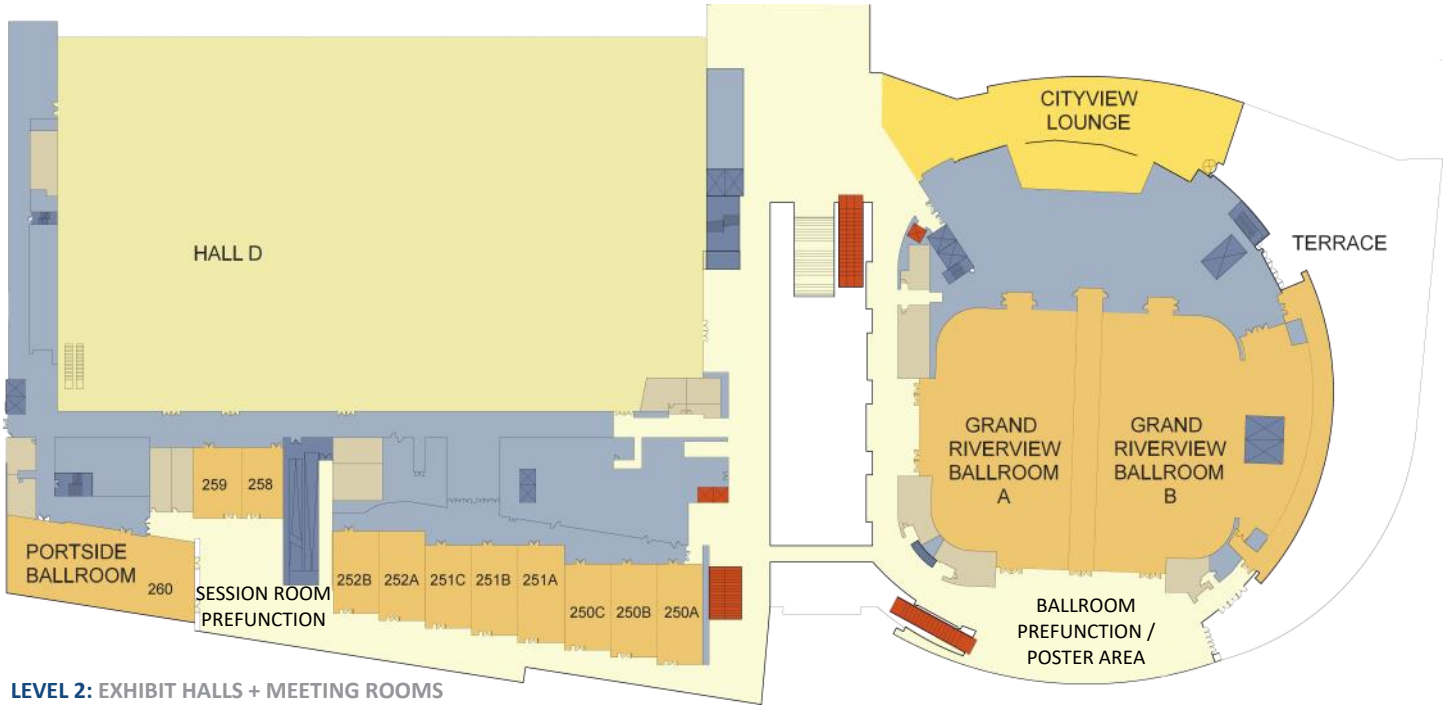
3:40 PM ***Afternoon Break***

Refreshments located in the Ballroom Prefunction Space

4:00 PM ***ERI Programs Panel - Phase II Overview and Emerging Concepts***

Dr. Mark Rosker, Director, DARPA MTO
Mr. Richard-Duane Chambers, ERI Special Assistant
Dr. Young-Kai Chen, Program Manager, DARPA MTO
Dr. Timothy Hancock, Program Manager, DARPA MTO
Dr. Gordon Keeler, Program Manager, DARPA MTO
Mr. Serge Leef, Program Manager, DARPA MTO
Mr. Andreas Olofsson, Program Manager, DARPA MTO
Mr. Paul Tilghman, Program Manager, DARPA MTO
Mr. Walter Weiss, Program Manager, DARPA I2O / MTO

5:30 PM ***Adjourn***



LEVEL 2: EXHIBIT HALLS + MEETING ROOMS

Directions From People Mover: The People Mover (Detroit's public transit) enters The Cobo Center at Level 4. Upon arriving, take both of the escalators down to the main concourse on Level 2 and follow posted signs.

Wednesday, July 17, 2019 - Cobo Center

Community engagement is critical to shaping the future of ERI. Ongoing Efforts sessions offer further information on existing ERI programs. Emerging Concepts sessions focus on topics not currently part of ERI. Enhancing Collaboration sessions equip the community to engage with DARPA and to transition technology.

7:00 AM — ***Registration / Breakfast / Poster Session***
Located in the Ballroom Prefunction Space and Grand Ballroom A

8:30 AM - 10:30 AM
Room 258

Ongoing Efforts: Guaranteed Architectures for Physical Security (GAPS)
Mr. Walter Weiss
In this session, the GAPS team will lead a discussion with interested parties on the first draft Integration Control Documents (ICDs) that describe how GAPS-compatible hardware and software will interact.

8:30 AM - 12:30 PM
Room 250B

Emerging Concepts: Heterogeneous Integration for RF & Mixed Signal Systems
Dr. Tim Hancock
This workshop will focus on the problems facing the commercial and DoD communities in the area of heterogeneous integration and packaging, including challenges associated with dense digital integration, high-bandwidth RF integration, thermal management, and mixing silicon technology with compound semiconductors.

8:30 AM - 12:30 PM
Room 251B

Ongoing Efforts: Trust through Technology: Addressing Security and Manufacturing Challenges in DoD Systems
Dr. Ken Plaks
The workshop will discuss DARPA efforts to, by leveraging technological solutions, create trusted-by-design components that are compatible with the modern fabless semiconductor foundry model.

8:30 AM - 5:30 PM
Room 260

Ongoing Efforts: IDEA & POSH: ERI Design Integration Exercise
Mr. Andreas Olofsson
This Integration Exercise will provide users with a chance to evaluate the one year release of "no human in the loop" physical layout and system generators from the IDEA program and open source IP and verification technology in development under the POSH program.

8:30 AM - 5:30 PM
Room 252A

Ongoing Efforts: Lifelong Learning Machines (L2M)
Dr. Hava Siegelmann
The workshop will highlight the status of the L2M program, with presentations from selected L2M performers, with additional interactive sessions on where L2M concepts are headed. The workshop will also include a "Centers Group" discussion devoted to the topic of translating biological learning concepts to machines.

8:30 AM - 5:30 PM
Room 250C

Emerging Concepts: Edge Intelligence
Dr. Ali Keshavarzi
Through interaction with thought leaders and researchers, this interdisciplinary workshop will cover all scales – materials, devices, circuits, design, architectures, and implementations – to expand the vision of EI and explore the means to achieve it.

8:30 AM - 5:30 PM
Room 259

Emerging Concepts: Distributed Systems Simulation & Optimization
Mr. Serge Leef
In this workshop, we will discuss data models and abstraction levels suitable for fast and sufficiently detailed simulation of distributed systems, and approaches to optimize and secure them.

9:30 AM - 12:00 PM ***Ongoing Efforts: Atomic Clock with Enhanced Stability (ACES)***
Room 252B *Dr. John Burke*
The ACES Program Review Meeting will review and share project progress and accomplishments and provide an opportunity to discuss plans and options for the next 12-month period, especially the integration of electronics into the final prototype.

10:30 AM - 10:45 AM ***Morning Break***
Refreshments located in the Ballroom Prefunction Space

12:30 PM - 1:30 PM ***Lunch***
Located in the Ballroom Prefunction Space and Grand Ballroom A

1:30 PM - 5:30 PM ***Enhancing Collaboration: Emerging from the Lab – A Researcher's Guide for Funding Technology from Science to Solution***
Room 258 *Mr. David Henshall*
This discussion will include key insights into common pitfalls, the critical role of timing, and finding the right type of investor. The workshop will also talk about how industry uses tech scouting to identify, acquire, and scale critical technologies through licensing and partnerships, and what elements determine success and failure.

1:30 PM - 5:30 PM ***Emerging Concepts: Security – From Chip to Board***
Room 251B *Mr. Keith Rebello*
This workshop will feature a series of presentations examining state-of-the-art solutions for securing the hardware supply chain. A panel discussion will then explore the limitations and challenges of current safeguards and suggest new approaches for addressing threats to commercial-off-the-shelf hardware.

3:30 PM - 3:45 PM ***Afternoon Break***
Refreshments located in the Prefunction outside meeting rooms

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3:45 PM - 4:45 PM ***Enhancing Collaboration: DARPA/MTO Collaboration 101***
Room 251C *Dr. Mark Rosker and Dr. Jay Lewis*
Intended primarily for those who are new to working with DARPA, this session will equip attendees with a better understanding of DARPA's history and mission, the critical role of the Program Manager, and how new ideas turn into DARPA programs.

5:30 PM ***Adjourn***

Room	Morning (8:30 AM – 12:30 PM)	Afternoon (1:30 PM – 5:30 PM)
251B	Trust through Technology...	Security—From Chip to Board
258	Guaranteed Architectures for Physical Security (GAPS)	Emerging from the Lab ...Funding Technology...
250B	Heterogeneous Integration for RF & Mixed Signal Systems	
252B	Atomic Clock ... (ACES, 9:30 AM – 12:00 PM)	
251C		DARPA / MTO Collaboration 101 (3:45 PM – 4:45 PM)
259	Distributed Systems Simulation & Optimization	
252A	Lifelong Learning Machines (L2M)	
260	IDEA & POSH: ERI Design Integration Exercise	
250C	Edge Intelligence	

For room map, please see page 8.

Poster Session Layout

Design & Security	Performer(s)	Program
Guaranteed Architecture for Physical Security	Northrop Grumman	GAPS
ALIGN: Analog Layout, Intelligently Generated from Netlists	U Minnesota, Texas A&M, Intel	IDEA
GUIDE: Generative User Intent-driven Design of Electronics	Northrop Grumman Mission Systems, JITX	IDEA
IDEAL: An Intelligent Design Environment for Asynchronous Logic	Yale, UT Austin, Texas State	IDEA
LSOracle: A Learning Based Oracle for Automatic Logic Optimization	U Utah	IDEA
Analog Mixed Signal (AMS) Open-source IP Ecosystem	USC, MOSIS, GlobalFoundries	POSH
CIFER: Coherent Interconnect and FPGA Enabling Reuse ORDER: Open-Source Rooted Design Experts with Repute	Princeton, Cornell, U Washington	POSH IDEA
OpenFPGA: A Framework Enabling Rapid Prototype of Customizable FPGAs	U Utah	POSH
The BlackParrot RISC-V Multicore	U Washington, Boston U	POSH
System Security Integration Through Hardware and Firmware (SSITH)	DARPA	SSITH

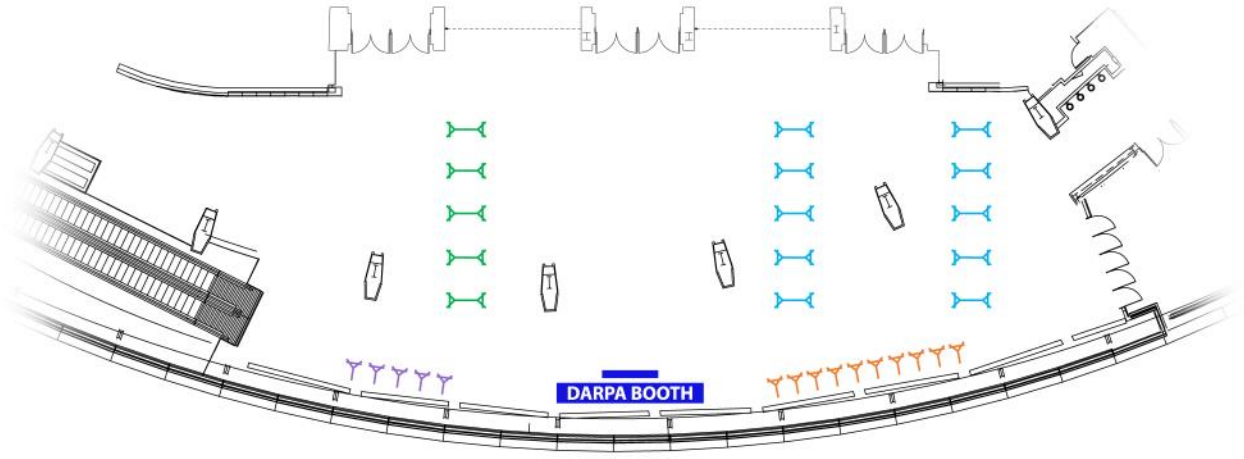
3D Heterogeneous Integration	Performer(s)	Program
3D Monolithic System on a Chip	MIT, Stanford, SkyWater Technology Foundry, NanoIntegris (Raymor), Georgia Tech, Duke	3DSoC
Heterogeneous Systems-on-Wafers	UCLA	CHIPS
Modular System Design in 2.5D	U Michigan	CHIPS
Millimeter Wave Digital Arrays (MIDAS)	DARPA	MIDAS
Integrating Advanced Interconnect Bus with TeraPHY	Ayar Labs, Inc.	PIPES

Materials & Devices	Performer(s)	Program
Functional Fiber Electronics (FFE)	MIT Lincoln Laboratory	FFE
A Synaptic Switch for Neuromorphic Compute	Applied Materials, Symetrix, U British Columbia, ARM, U Colorado-Boulder	FRANC
Compute-Near-Memory Architecture	Micron Technology, Inc.	FRANC
MRAM-based Deep In-Memory Architectures	Raytheon Missile Systems, GlobalFoundries, Princeton, UIUC	FRANC
Scalable, Energy-Efficient, and High-Throughput All-Memristor Neuromorphic Processor	HRL Laboratories	FRANC
Spintronic Stochastic Dataflow Computing	UCLA	FRANC
Compact, Light-Weight, Low-Cost Laser Radar	ASR Systems, Columbia, Voyant Photonics	MOABB
Integrated Optical Phased Arrays for LiDAR	Analog Photonics	MOABB
Vision Cued LIDAR for Autonomous Navigation	Teledyne Scientific Company	MOABB
Memristive Crossbar Arrays for Brain-inspired Computing	U Massachusetts Amherst	Young Faculty Award

Specialized Functions	Performer(s)	Program
Development of Next Gen Processors	ASU	DSSoC
Run-Time Configurable Accelerator (RCA)	Raytheon, Raytheon BBN, System View, Xilinx	DSSoC
Hierarchical Identify Verify Exploit (HIVE): 1000X Faster Graph Analytics	DARPA	HIVE
A Scalable Pipeline for Designing Reconfigurable Organisms	Tufts, U Vermont, ASU	L2M
Dynamic Architectures via Introspection and Neuromodulation	Argonne National Laboratory, Rochester Institute of Technology, Sandia National Laboratories	L2M
Lifelong Learning Across Synapses, Circuits, and Brain Areas	Baylor College of Medicine, Columbia, NYU	L2M
Lifelong Learning of Perception & Action in Autonomous Systems	UPenn, U Michigan, Brown, UT Austin, USC	L2M
Robot Self-Modeling	Columbia	L2M
Solutions to Catastrophic Forgetting	HRL Laboratories	L2M
M0N0: an Ultra-low Power Microcontroller	Arm Research	N-ZERO
Near Zero Power RF and Sensor Operations (N-ZERO)	DARPA	N-ZERO
Spectrum Collaboration Challenge (SC2)	DARPA	SC2
DDARING: Dynamic Data-Aware Reconfiguration, INtegration & Generation	Georgia Tech, U Illinois, U Michigan, USC	SDH
HammerBlade: A Supercomputer for ML & Graphs	U Washington, Cornell	SDH
Honeycomb: A Software Defined Data Analytics System with Unprecedented Efficiency	Qualcomm, ESS, OMICS	SDH
Intel SDH PUMA Platform	Intel	SDH
Plasticine: A Universal Data Analytics Accelerator	Stanford	SDH
SDH: Mitchell	Systems & Technology Research, Northeastern, Purdue	SDH
The DECADES Project	Princeton, Columbia	SDH
Transmuter – A Reconfigurable Computer	U Michigan, ASU, U Edinburgh	SDH

Design & Security

Specialized Functions



3D Heterogeneous Integration

Materials & Devices

Notes

ERI