ERI Design: IDEA and POSH

Generative **U**ser-**I**ntent **D**esign of **E**lectronics

GUIDE

Technical Area 2

Open Session

Dr. Jonathan Bachrach, Dr. Duncan Haldane (JITX)

Dan D'Orlando (NGC)

IDEA and POSH Integration Exercise and PI Review

Detroit, MI

July 17, 2019 - July 19, 2019

THE ELECTRONICS RESURGENCE INITIATIVE

Achieving 24 Hour, Intent Driven PCB Design with Open & Modular Software

Teaming

Northrop Grumman (Prime)

Jim Kuszewski - PI
Dan D'Orlando - PM

Design Domain Expert
Transition
Systems Architecture & Applications

JITX (Sub)

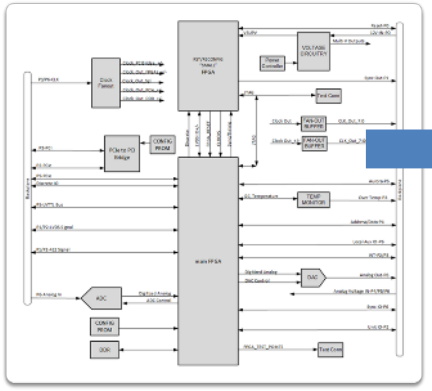
Dr. Jonathan Bachrach - PI
Dr. Duncan Haldane - CEO

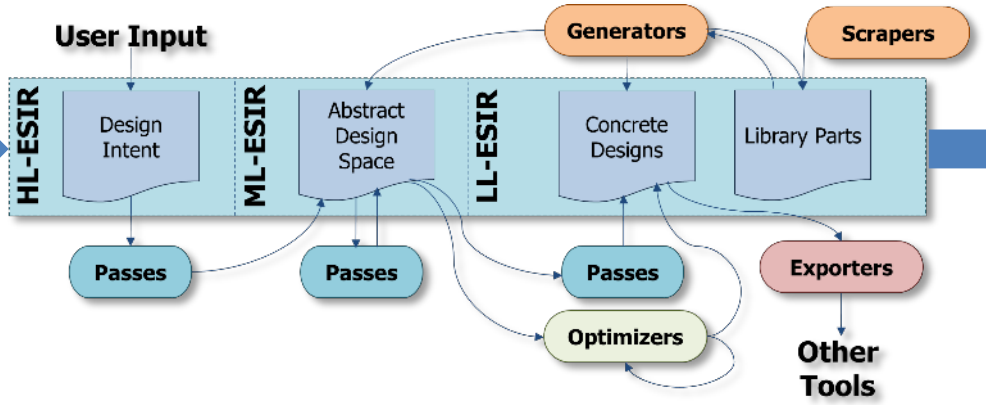
Embedded System Intermediate Representation (ESIR)
Open Parts Database
Intent-driven System Generator
Circuit Optimizer

Goals & TA2 Approach

- Specify what, not how!
- Requirements Simple
- Flexible
- DoD Approved

Capture Intent → Transform to Optimized, Concrete Design Using ESIR → Export Design and Hand-Off to TA1

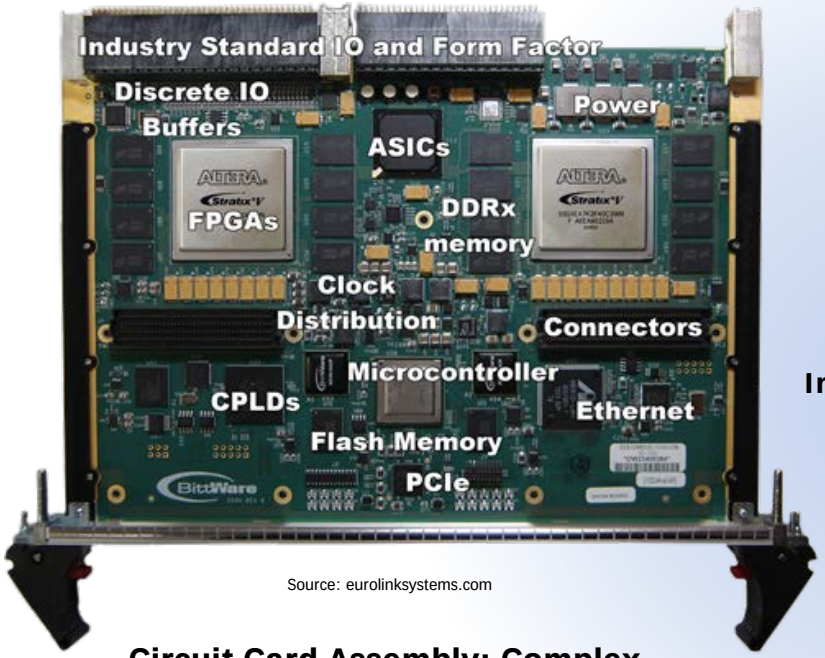





```
;; Keyin Netlist File
;; V4.1.0
;;
%NET
%PRIORITY=1
%PAGE=0
dio    R11-1 C6-1 S1-2 U1-10
ps$3_agnd    R12-1 U4-16
an-3v3    C16-2 U3-10 L0-2 R0-1 U3-15
noname7550    D5-1 R8-2
dio$2    R5-1 C4-1 S0-2 U1-11
noname7542    D2-1 R2-2
dio$5    U1-16 R21-1
ps$3_en    R15-1 U4-2
noname7551    U1-14 U0-2
```

Targeting Complex, Ruggedized Designs for DoD Applications

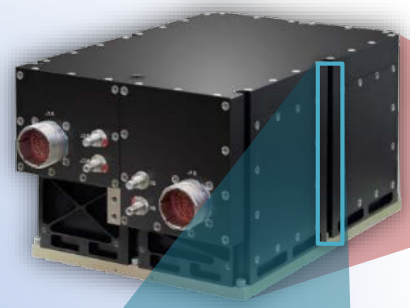
Target Designs



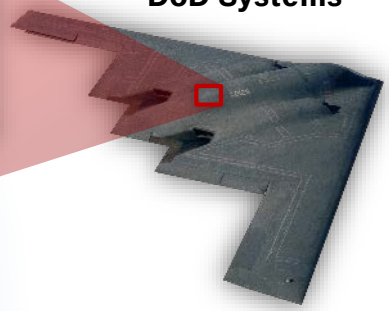
Source: eurolinksystems.com

Circuit Card Assembly: Complex, dense processing functions

Rugged Processing

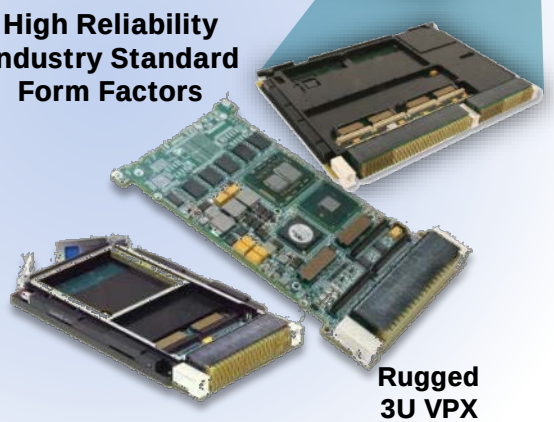


DoD Systems



Source: news.northropgrumman.com

High Reliability Industry Standard Form Factors



Rugged 3U VPX

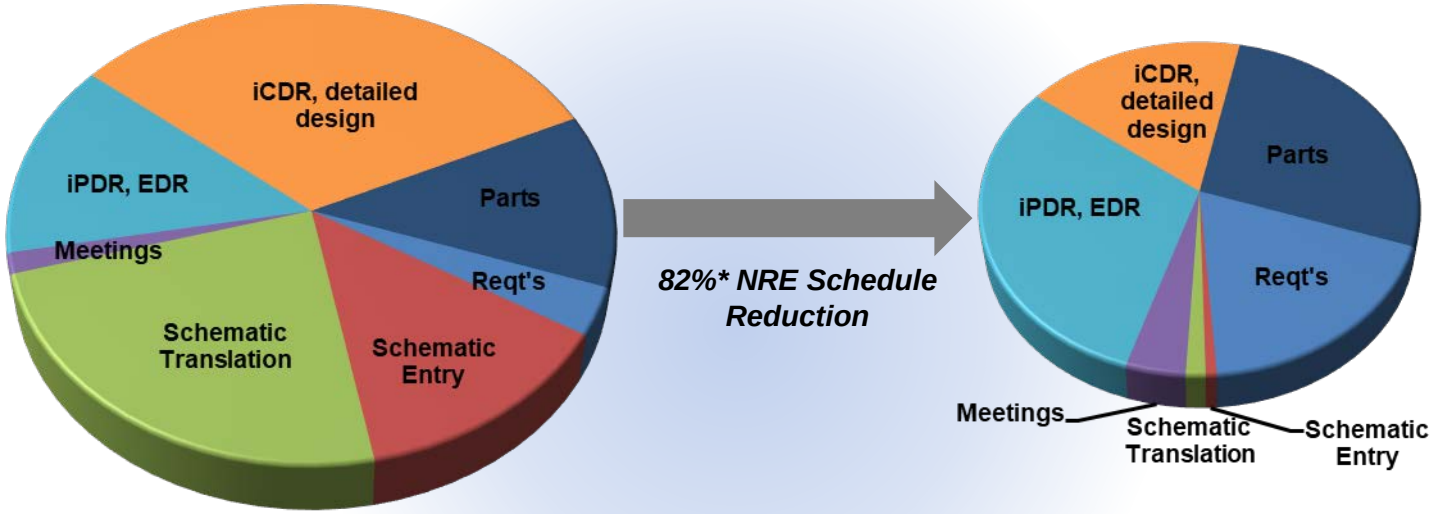
Source: archive.cotsjournalonline.com

Reducing the Hardware Design Cycle

Example Impact Case Study

*Data from Real NGC Designs. NRE savings only estimates. Real data to be collected in future phases.

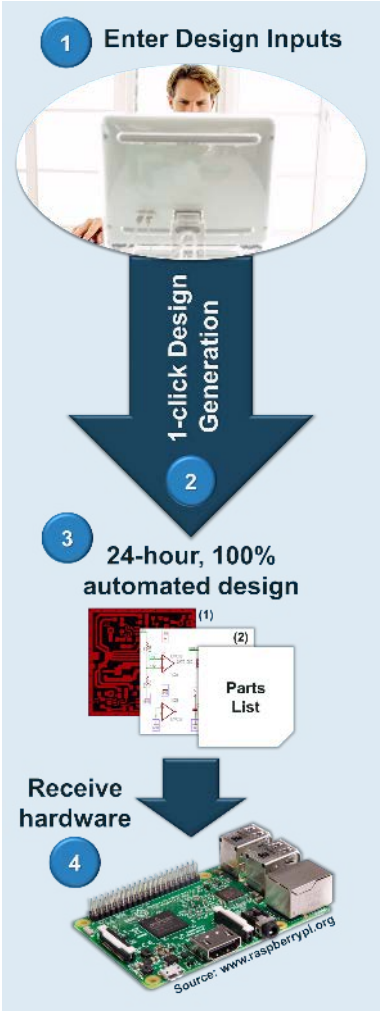
Design A: DoD Airborne Control CCA, Update design with latest technology and modern FPGA, but same functionality at IO level



Other DoD Case Studies		
Design B	DMS update to an older existing design, includes design capture tool update and DMS component replacement and collateral design changes	74% Reduction
Design C	Major update for form factor/IO connector plus significant additional new functions (80% new)	82% Reduction
Design D	Existing Design, minor tweak to requirements	57% Reduction

**Assumptions: Requirements Change/Review - No change; Overhead / Detailed Design / Schematic Capture / Design Entry / EDR - 60% reduction due to automated tools. No reduction for analysis (today); Meetings - Assumed 50% reduction due to less time between things to discuss; Reviews - Assumed 60% less because design is accurate due to automation

End State



Source: 1) scottyspectrumanalyzer.us/slim_PDM.html
2) learn.sparkfun.com

Example Design

USER INPUT

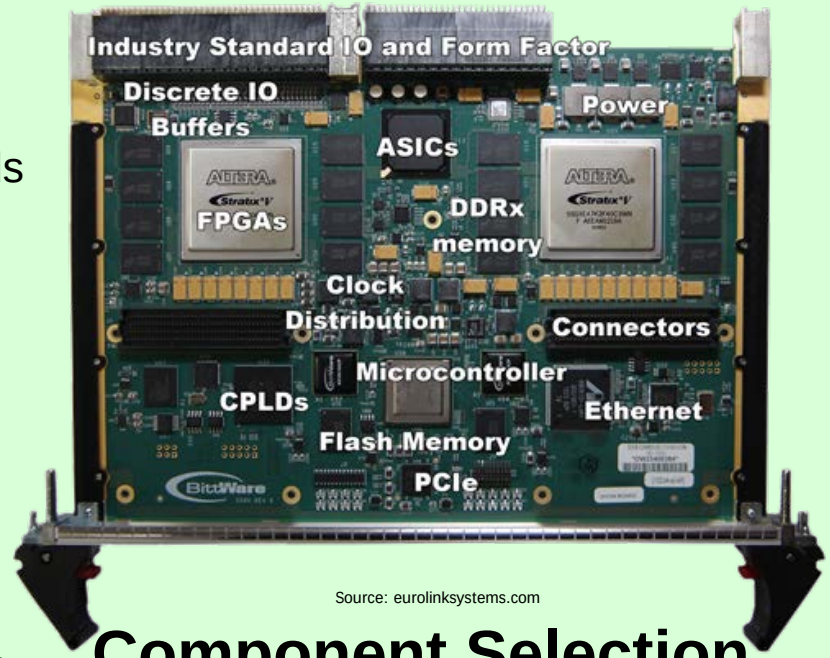
Top-Level Goal: Pipe data from connectors through FPGAs

AUTOMATICALLY DESIGNED

Power

Provide power to all loads

Trim and sequence rails



Source: eurolinksystems.com

I/O Translation

Implement interface ICs to make I/O compatible

Pin Assignments

Select and assign concrete pins to meet I/O goals

Clocks

Design clock trees to cover all requirements

Component Selection

Select components such as DDRx, EEPROM, etc. to meet functional high level intent

Automated Design Using GUIDE Software

1. Capture user intent with a programming language

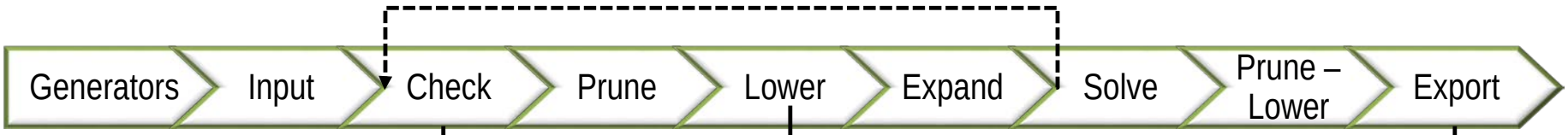
Get benefits of software - flexibility, modularity, abstraction, reusability

```
inst fpga : xilinx-XCKU060-1FFVA1517I-cmp
inst ram : {sdram(`ddr3, `x32, `x4Gb)}
connect (ram.ddr3, fpga.ddr3)
```

User Input

2. Generate concrete design from intent using a compiler

Modular generators and passes for solving design problems attached using ESIR



ELKT

Expand Bundle Nets; Flatten Hierarchy; Groups, Nets Merges; Computes Pin Properties

```
fpgapod18rxnet   U0-AM31 U56-5
levelshifter4t_GND_net   U64-11 U64-12 U64-13 C101-1 C100-1 C131-1 C130-1
fpgapod10rxnet   U54-5 U0-AP30
iface33en   U38-3 U38-2 U64-20
iface39pwr   C69-1 U50-8
backplane_P_2_B3_net   J2-B3 U18-7
fpgapod30rxnet   U58-9 U0-AW35
backplane_P_2_A1_net   J2-A1 U13-6
ifaceluart_tx_net   U19-1 U65-20
...
```

Key-In
Verilog
LEF
DEF

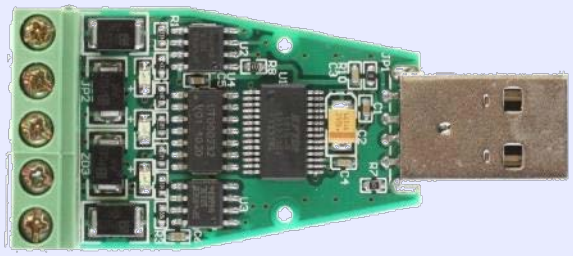
Detailed Output

Live Demo

Demo Designs Show Scalability of Software

Design 1

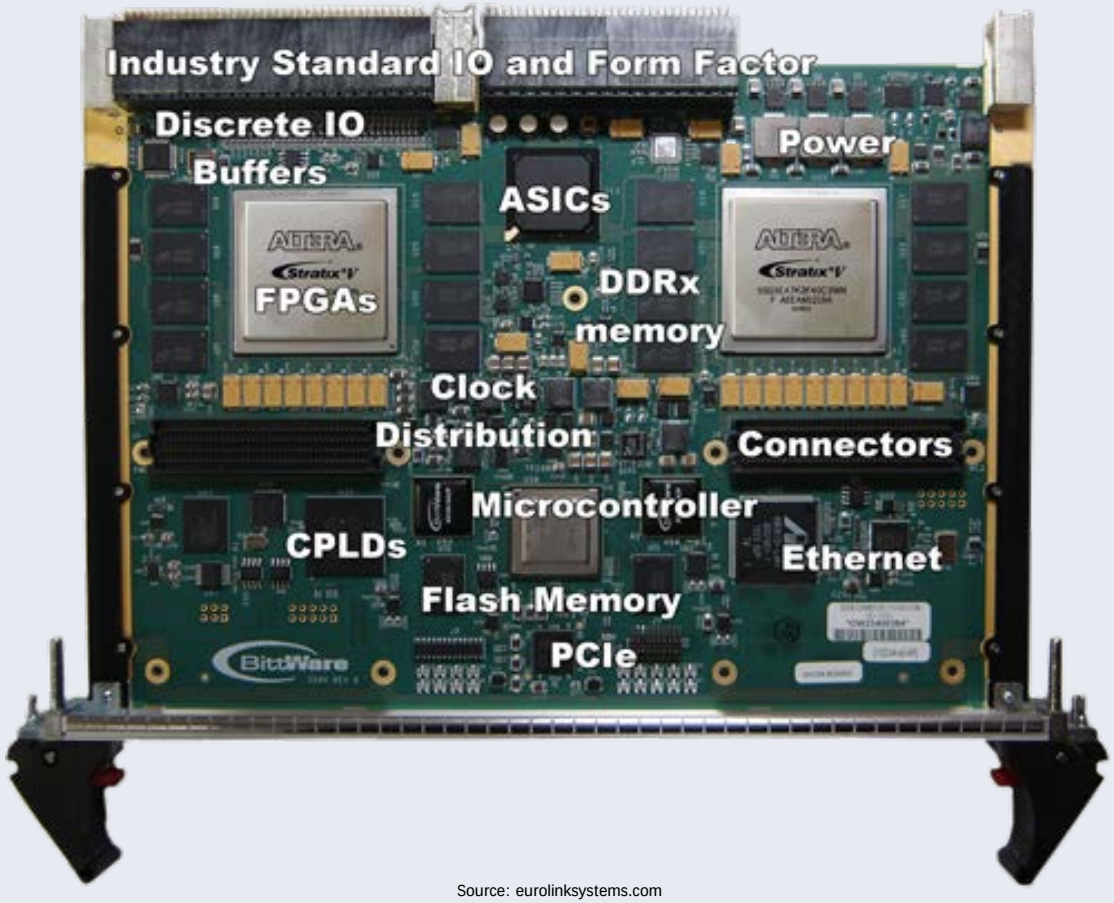
Simple
Microcontroller Based
Limited Functionality



Source: gearmo.com/shop/usb-to-rs485-rs422-converter-ftdi-chip-with-terminals/

Design 2

Complex
FGPA Based
DoD Applicable



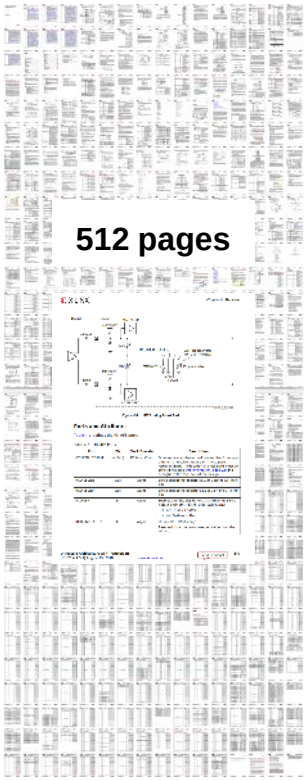
Source: eurolinksystems.com

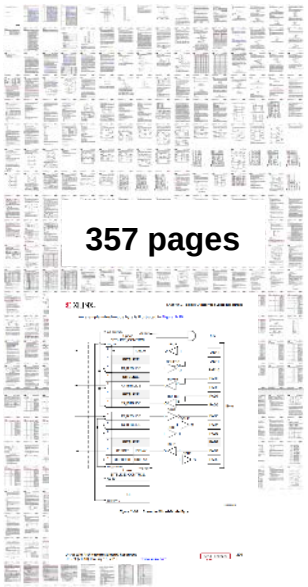
*Images Not Actual Design

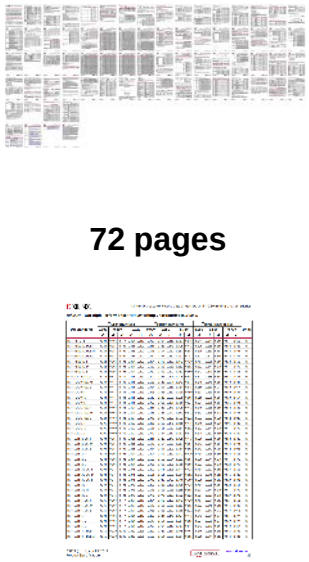
Automated Modeling of Components Through Datasheet Scrapers

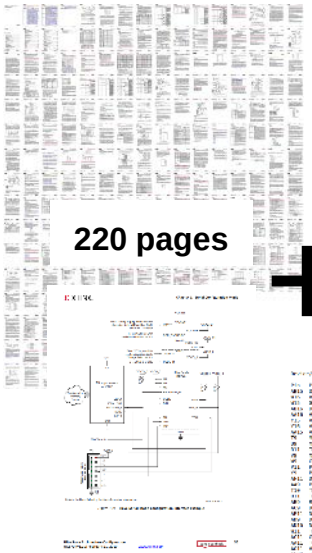
Import complex component information (**FPGA design**) directly into generator system

Generator source material: FPGA datasheets

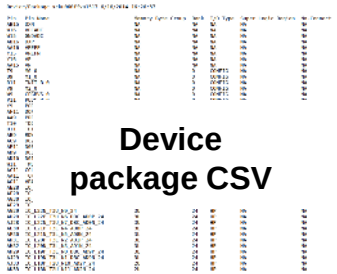








FPGA Constraint Files (e.g. Xilinx XDC)



Source: Manufacturers' websites

Acknowledgements

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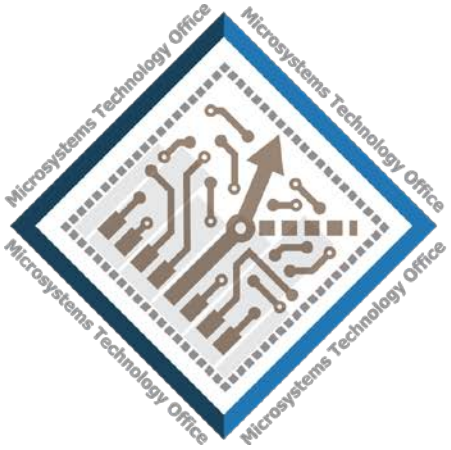
- *Disclaimer: This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions, and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.*



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