ELECTRONICS RESURGENCE INITIATIVE

# ERI Design: IDEA and POSH

## *MAGESTIC:* Machine-Learning for Automatic Generation of Electronic Systems Through Intelligent Collaboration

Cadence Design Systems, NVIDIA and Carnegie Mellon University

IDEA and POSH Integration Exercise
Detroit, MI

July 17 – July 19, 2019

***This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions, and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.***




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# MAGESTIC Program

- Team: Cadence Design Systems, NVIDIA and Carnegie Mellon University
- Goals:
  - No Human in the Loop (NHIL) Design Flow, Silicon Compiler in < 24 hours TAT
  - Research in Analog IC Design through Package and PCB Design
  - Achieve Automated Design Across a Broad Spectrum of Designs in Year 2
- Agenda for Today:
  - Software Demonstration of NHIL Package and PCB Design Progress
  - Focus for NHIL Package and PCB Design Research in Year 2

  Taylor Hogan
  - Software Demonstration of NHIL Analog IC Design Progress
  - Focus for NHIL Analog IC Design Research in Year 2

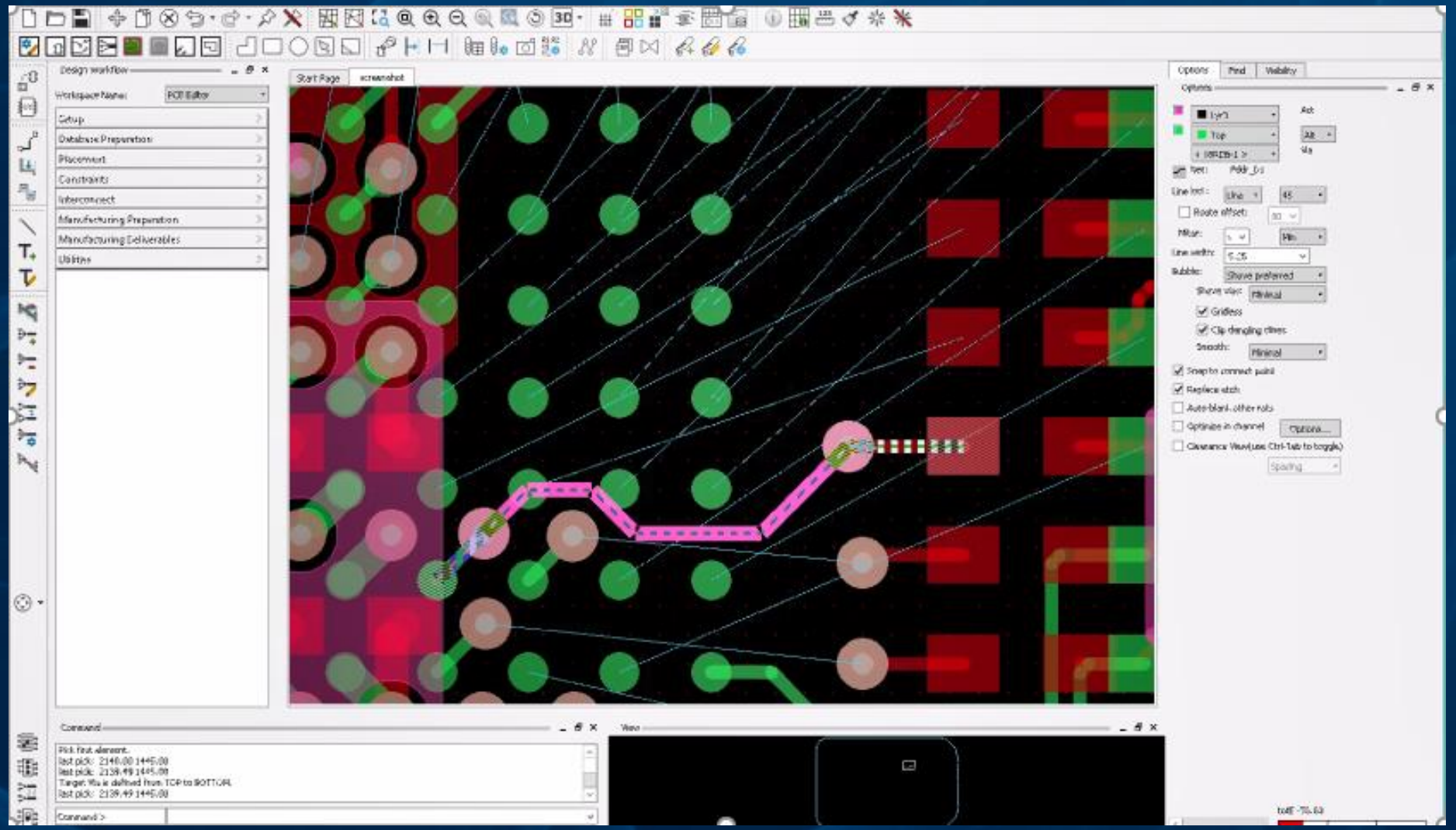
  Elias Fallon
- Visit MAGESTIC Team to see Live Demos of the Design Data Presented Today

# *PCB & Package Synthesis ERI Conference 2019*

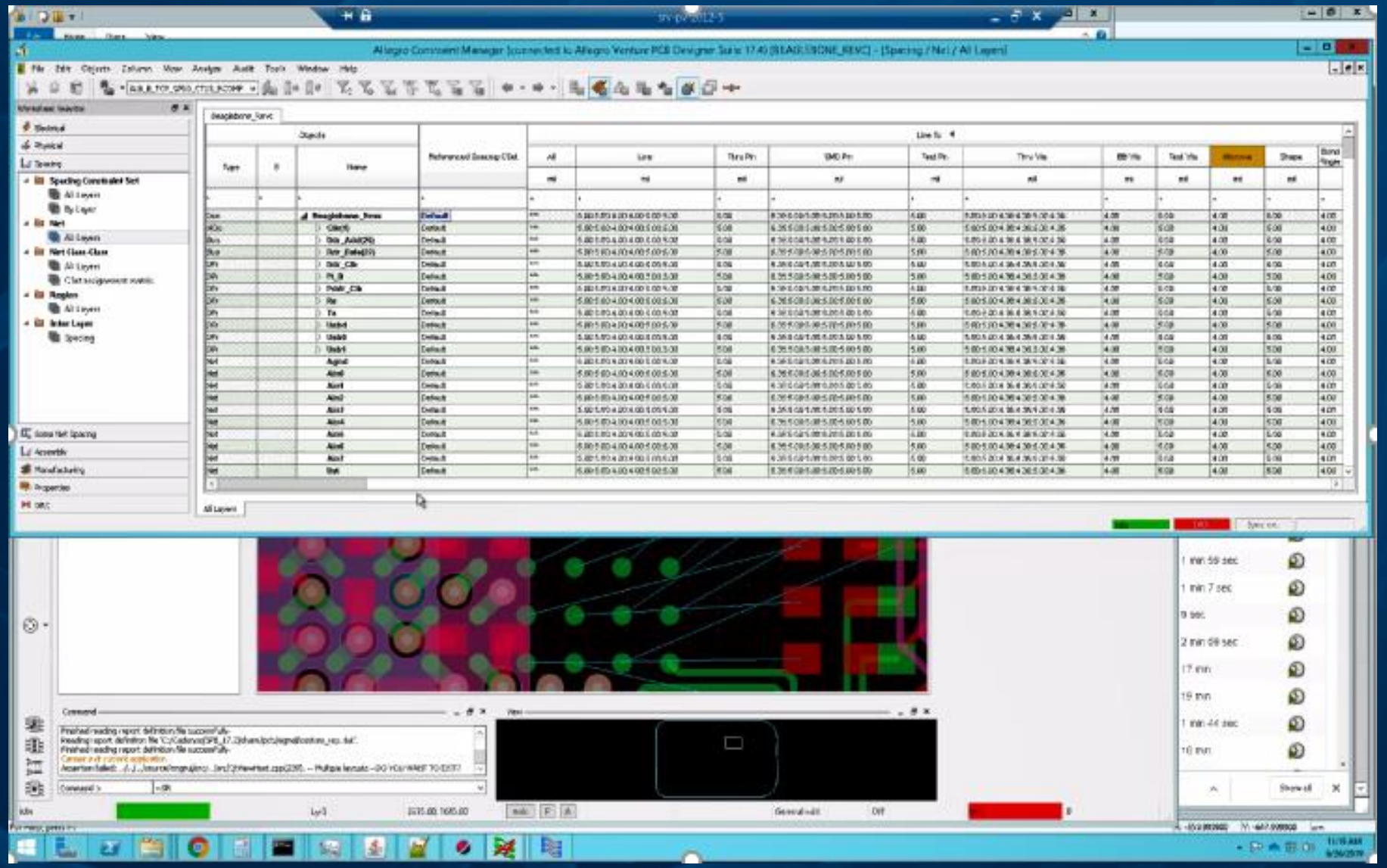
# EDA Ages

- The Dark Age
  - Interactive, NAIL
- The Industrial Age
  - NHIL for Some, Hope
- The Age of Enlightenment
  - NHIL for All, Explorations

# The Dark Ages



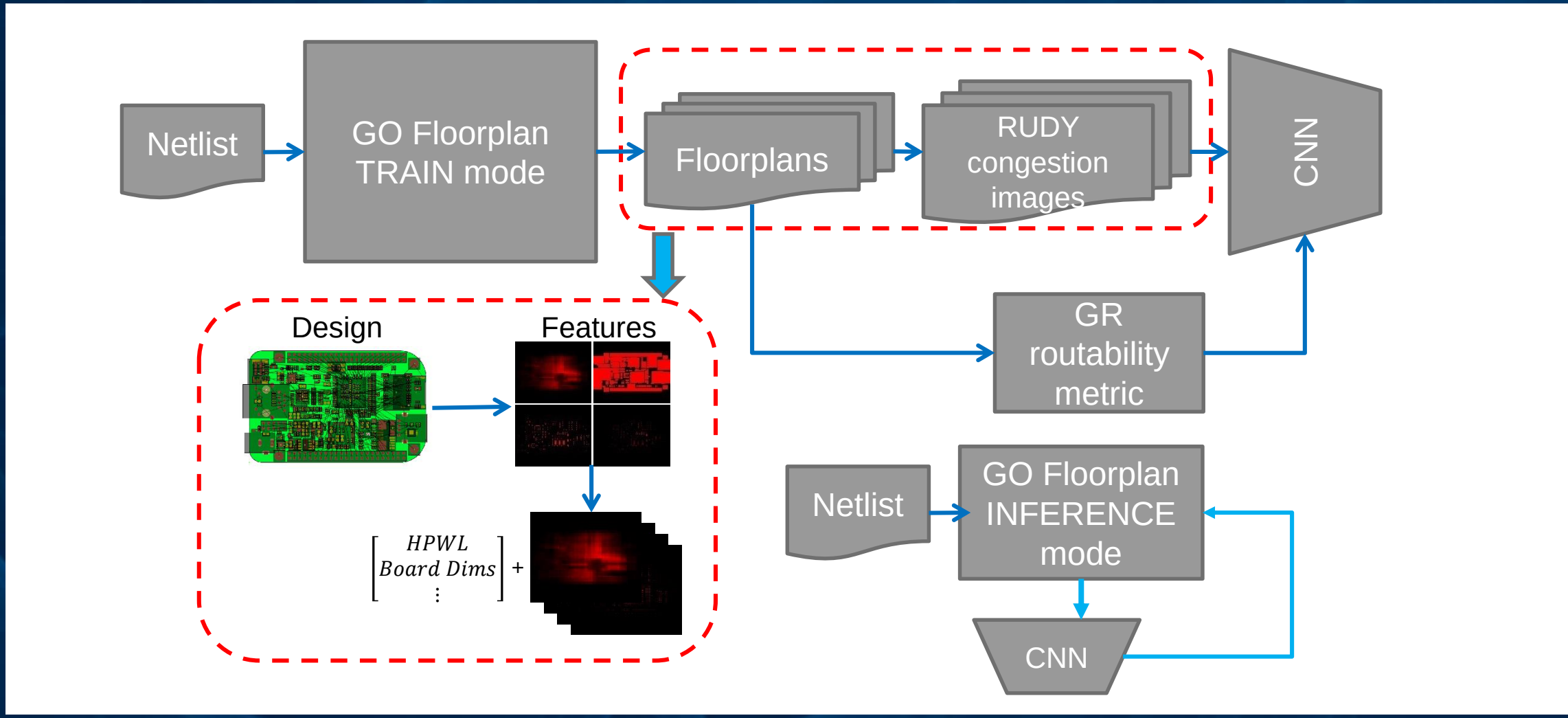
# The Dark Ages Continue



# The Industrial Age

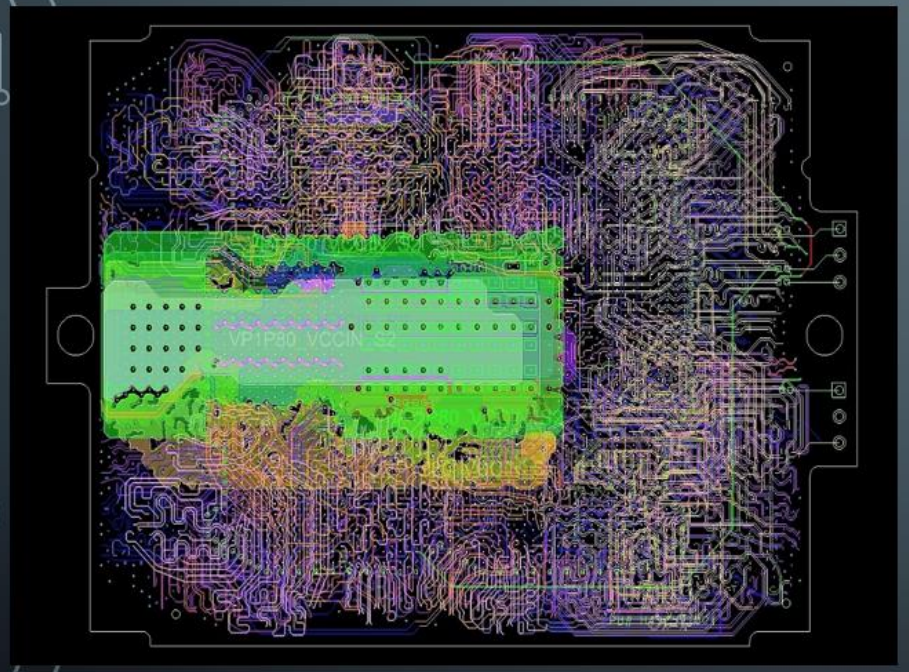
# Industrial Age

## Training Neural Networks to Avoid Intractable Computational Problems

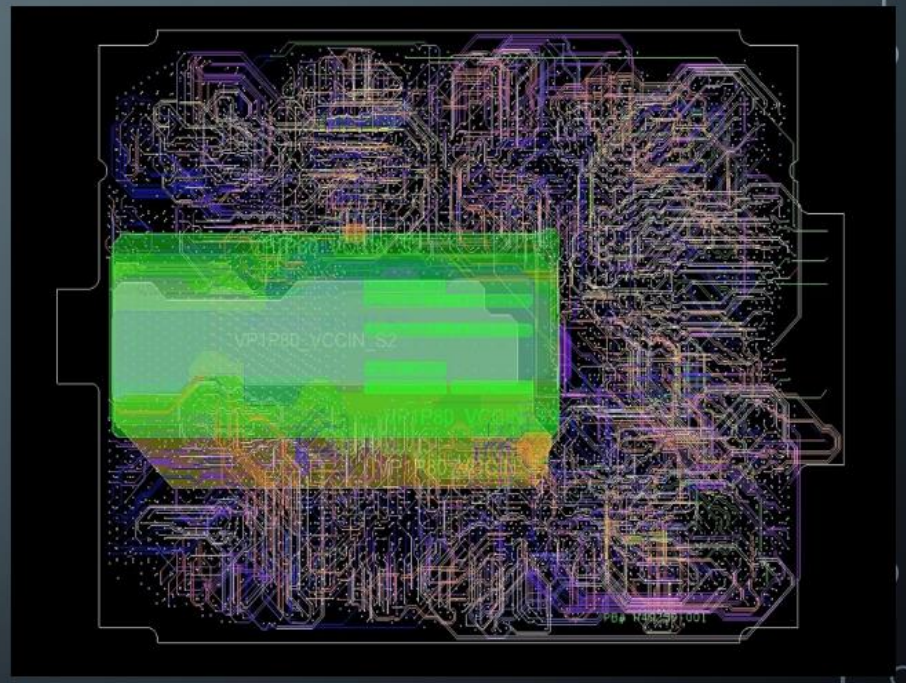


# The Industrial Age … Hope

## Auto Router Comparisons- Test Case 1



Manually routed and tuned N-1 CPU Interposer. Routing time: ~120 hours

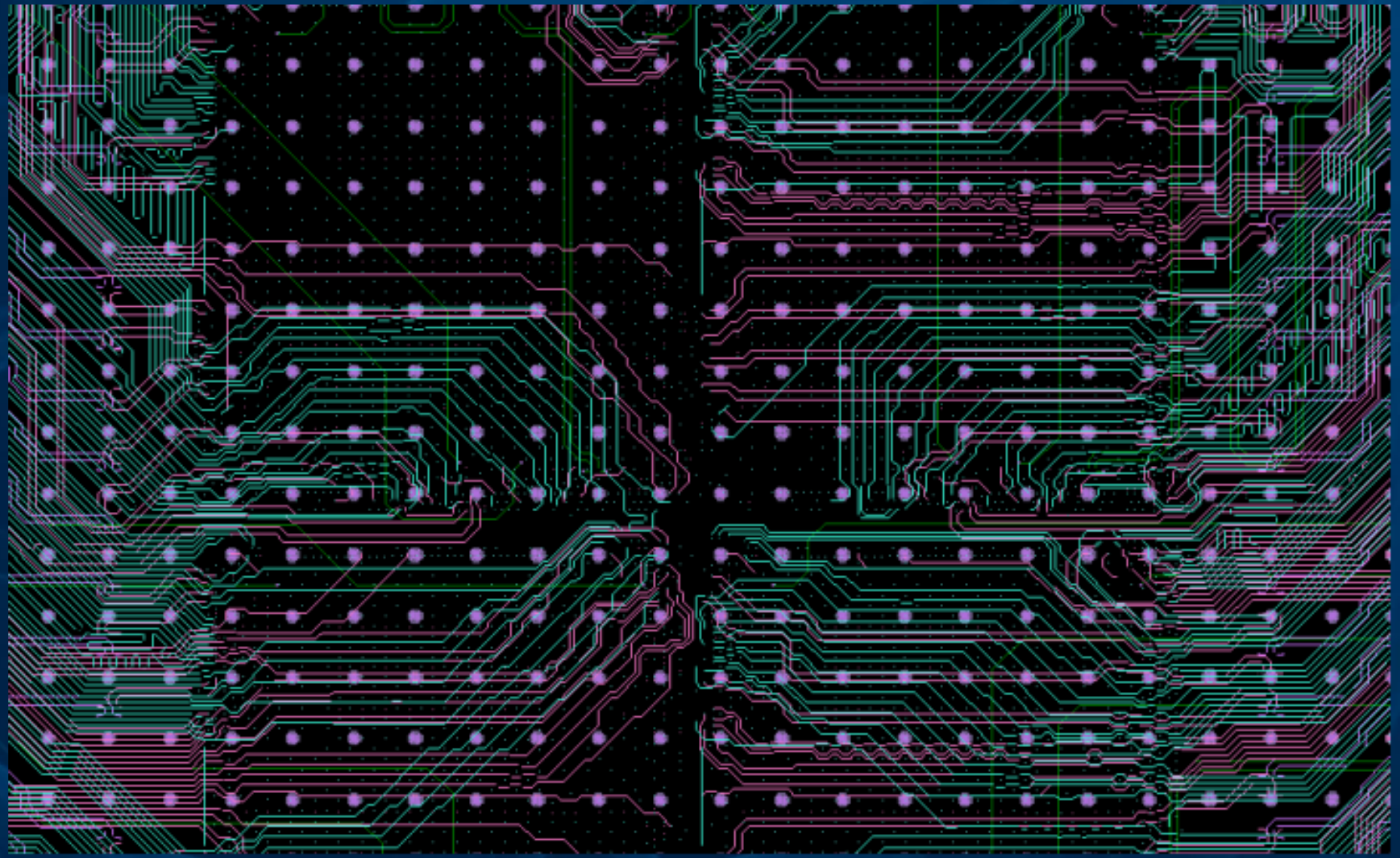


Automatic routings of N-1 CPU interposer using the AI Global router. Routing time: ~ 30 minutes

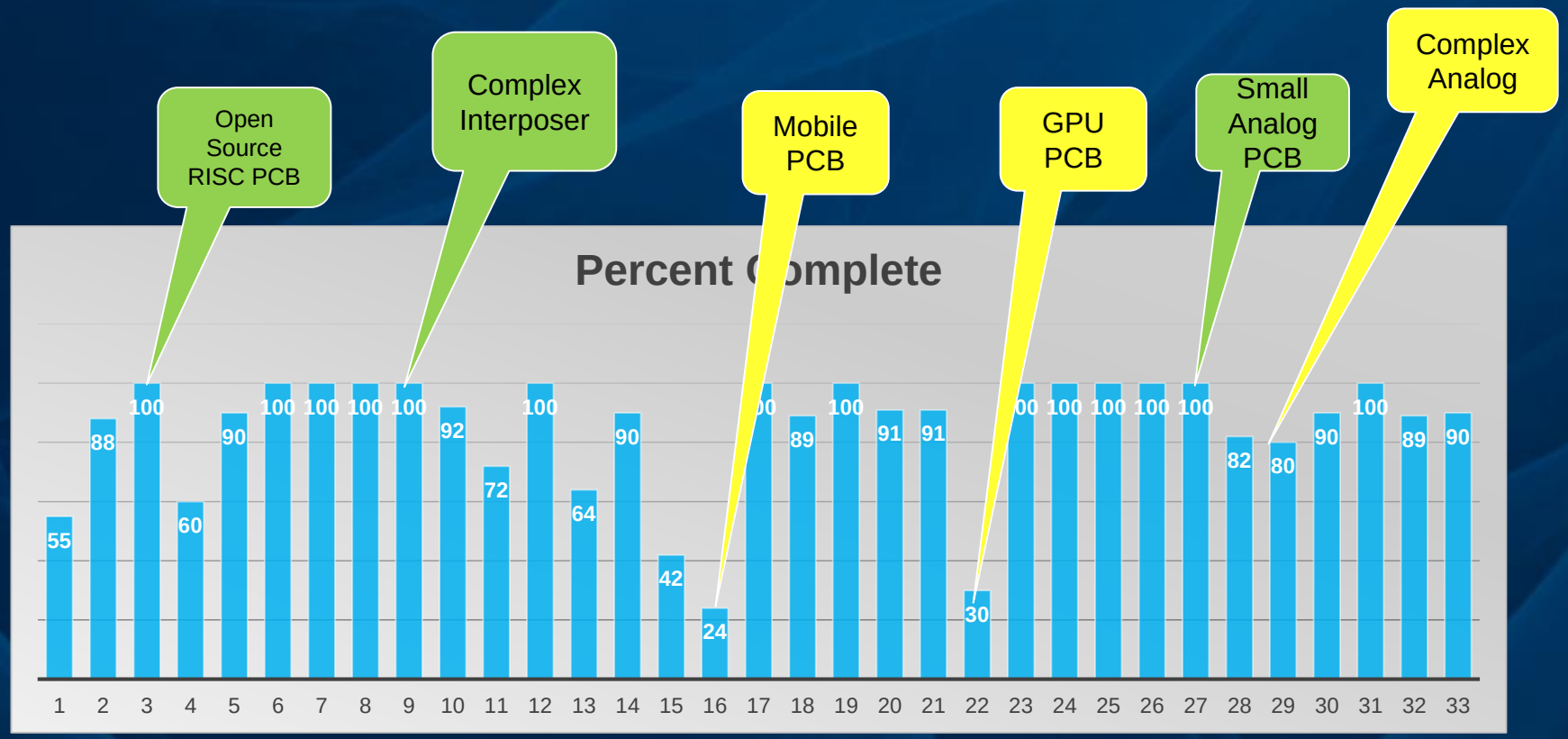
PCB West 2018, September 11-13, 2018, Santa Clara, CA

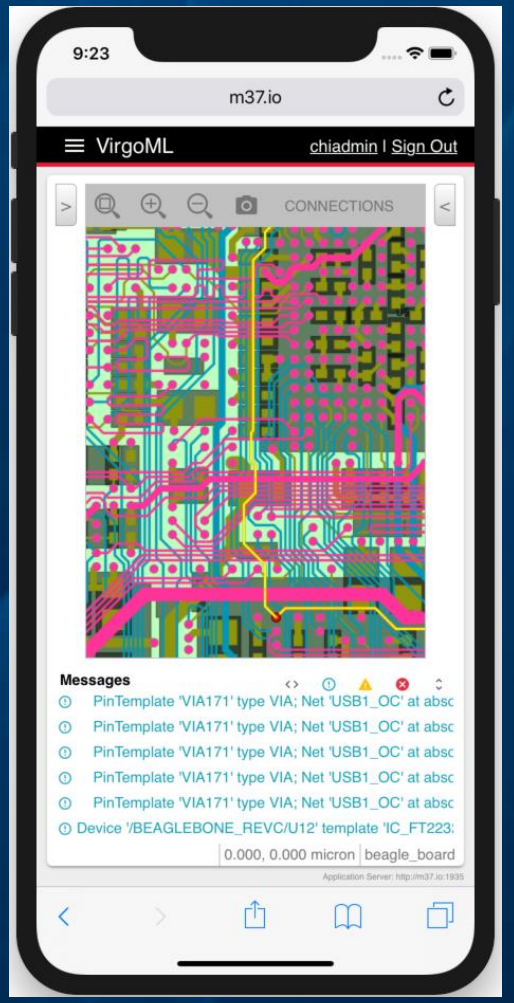
19

# Industrial Age Continues



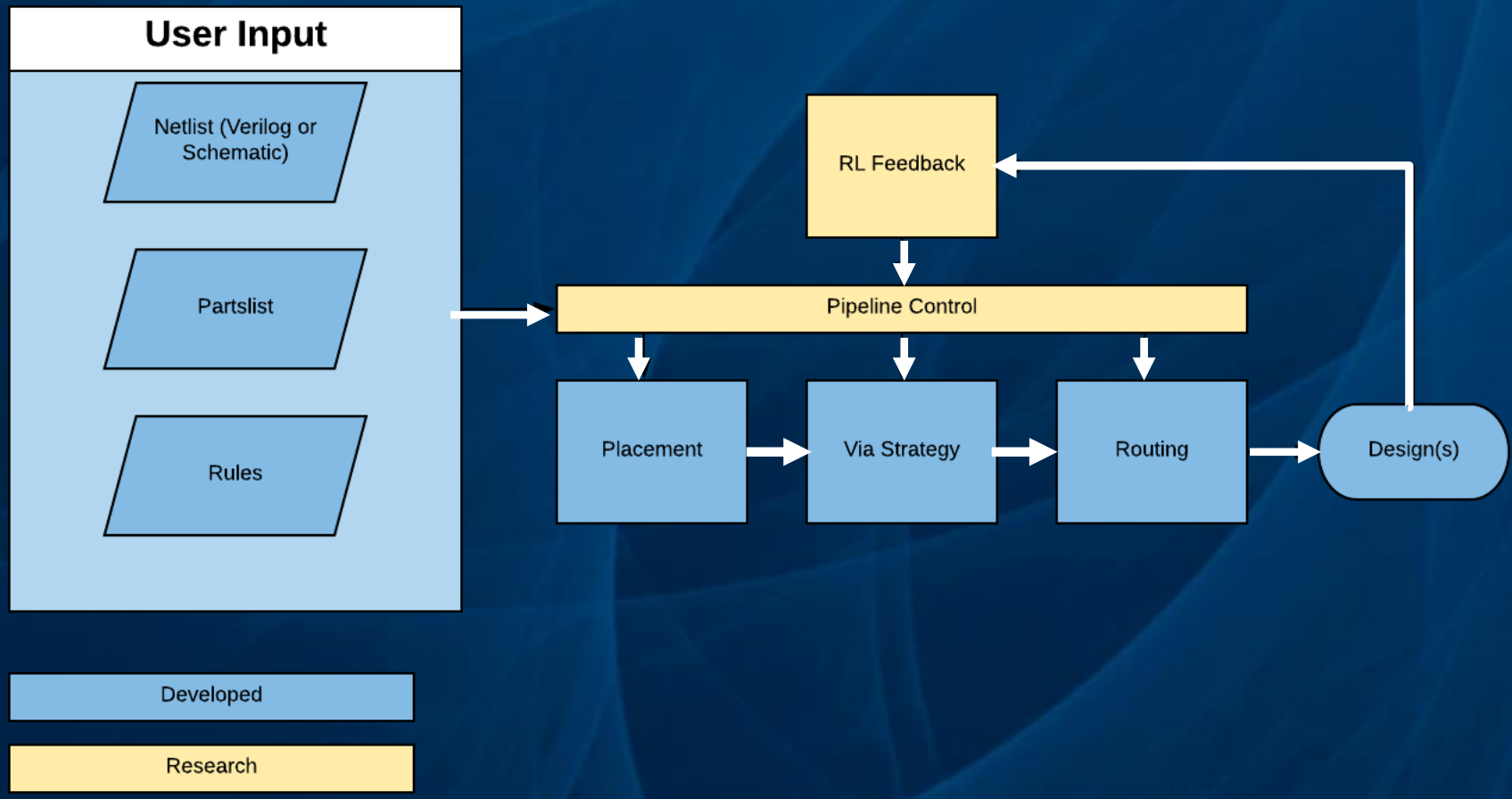
# What Works
# What Does Not Work



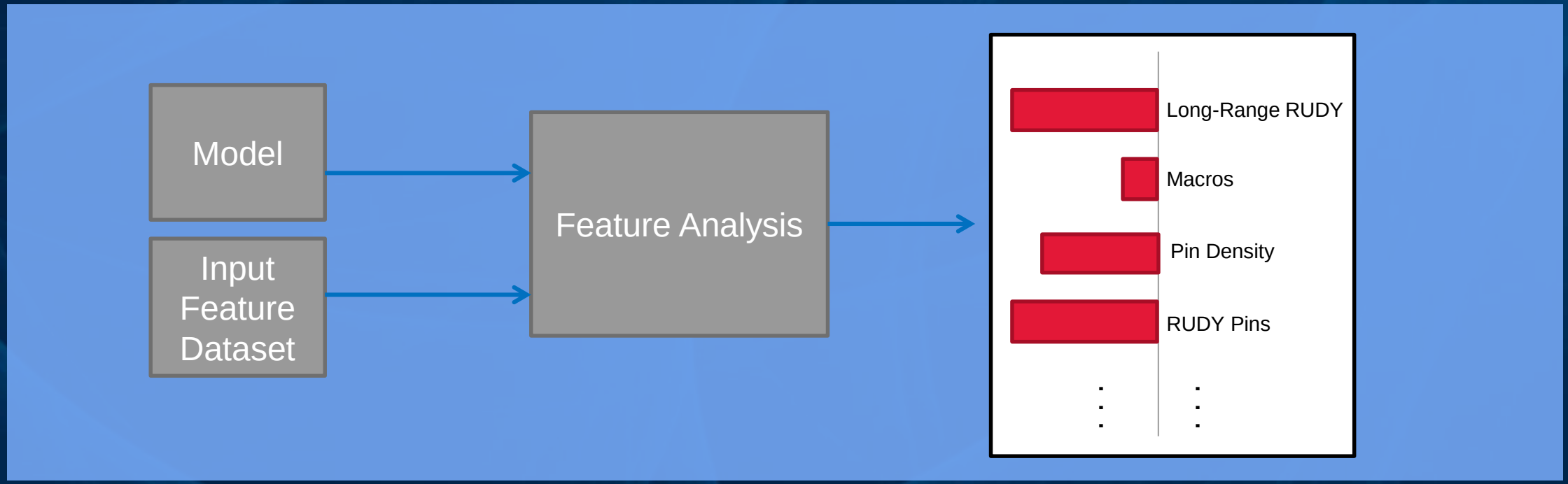
# Achieving NHIL for All





# Age of Enlightenment Feature Sensitivity Analysis

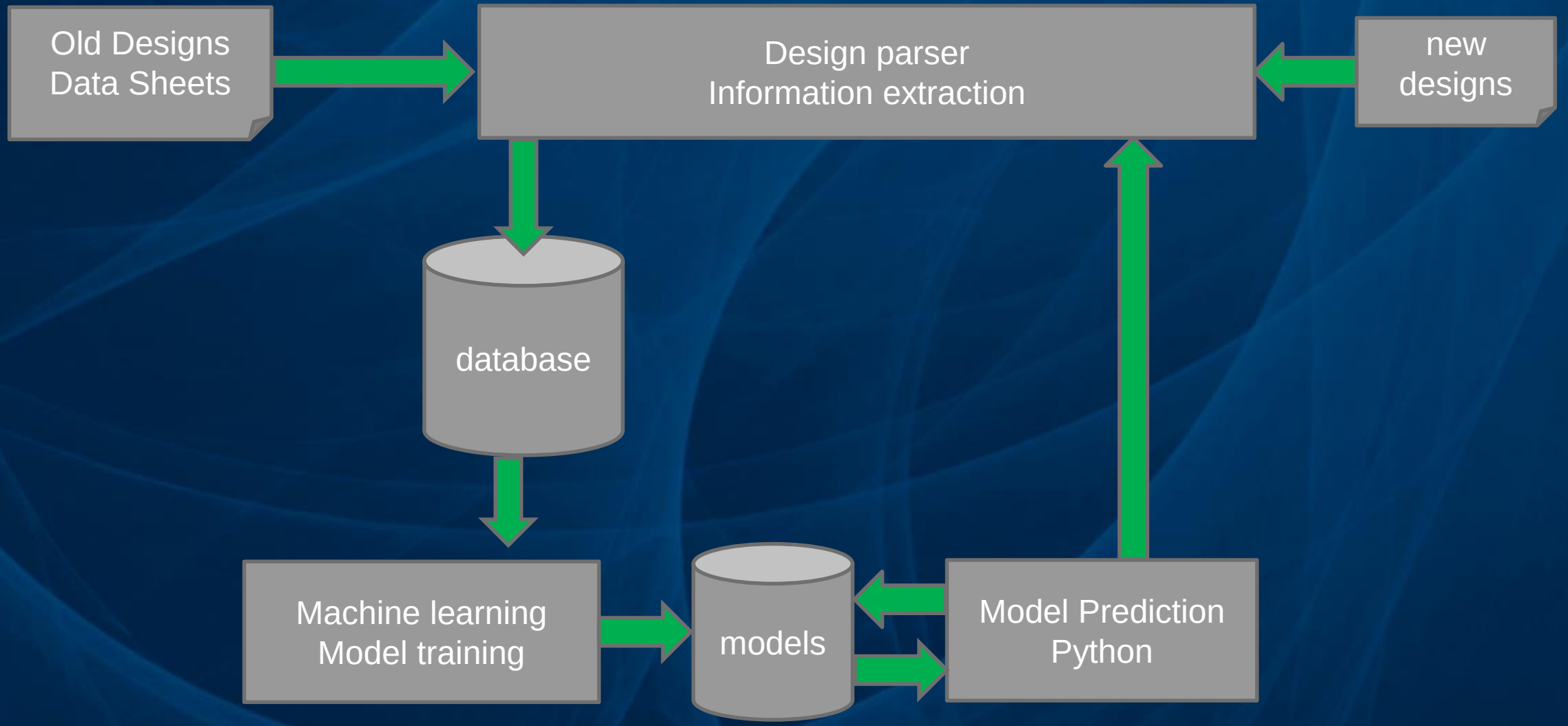
- Development of methods and tools that aid in the interpretability of neural networks by humans
- Explain what features matter



# The Age of Enlightenment

## Data Mining to eliminate typing in the known



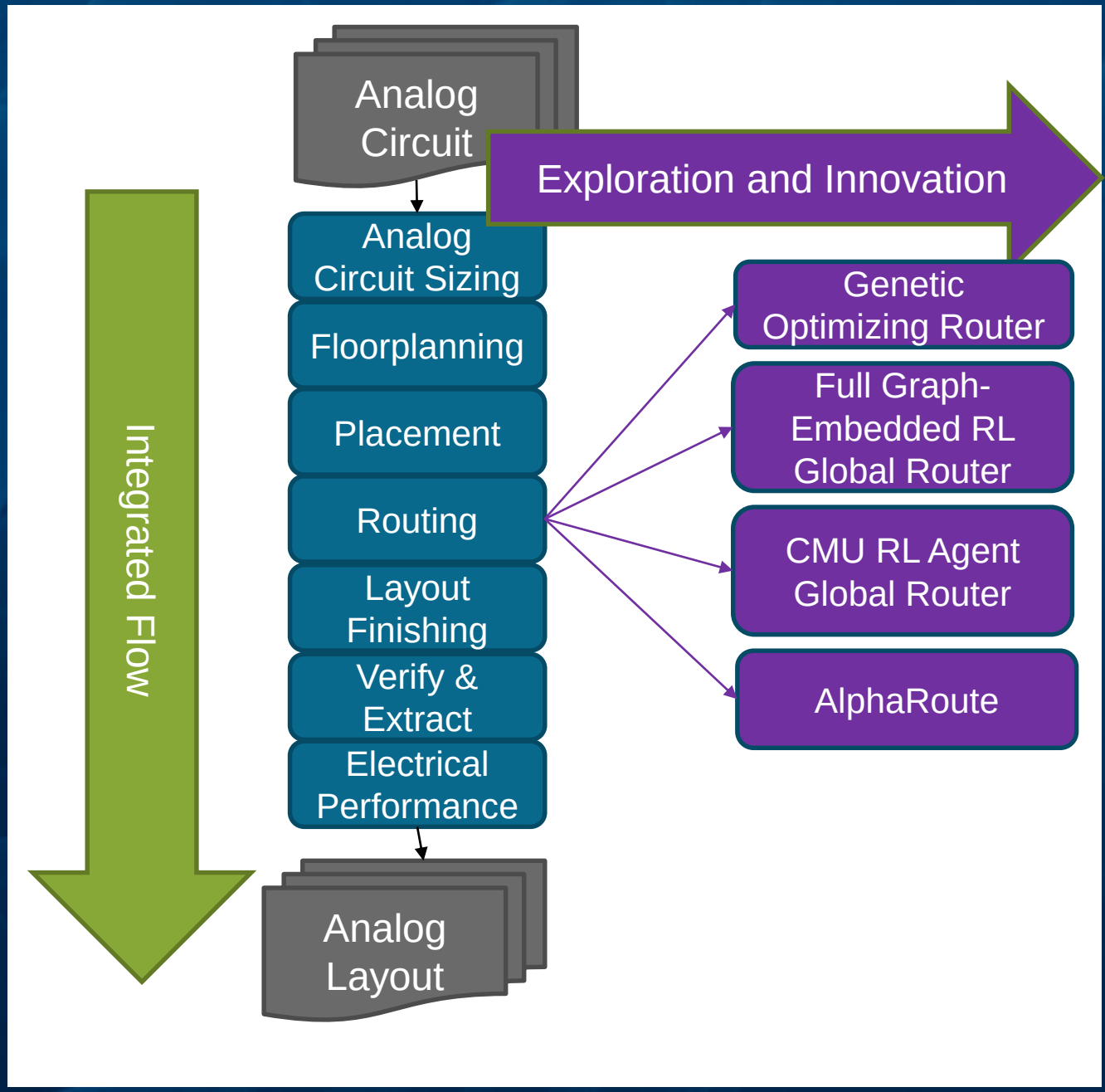


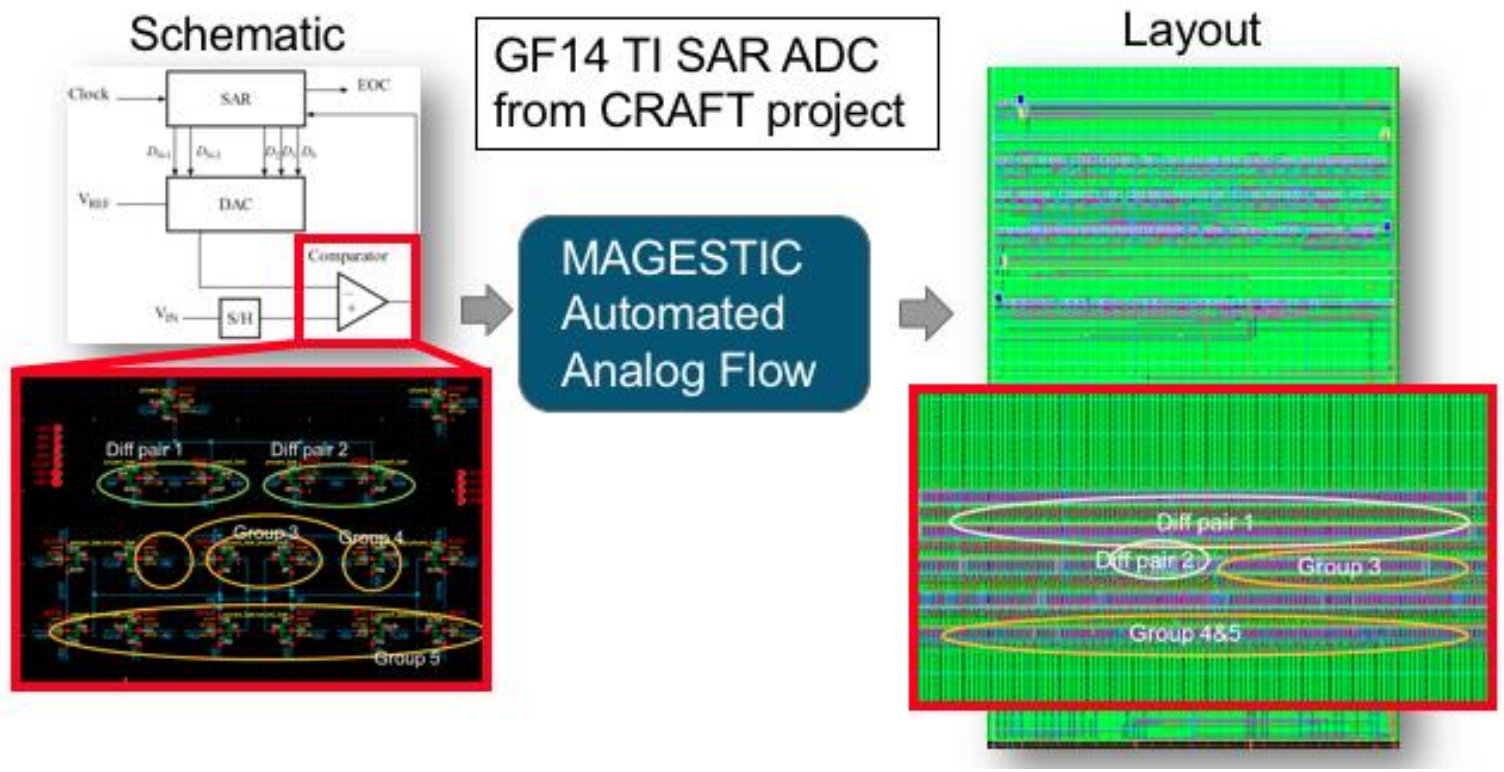
# *Analog IC ERI Conference 2019*

# MAGESTIC Analog

## Research Dimensions

- **Integrated flow**
  - See complex interactions between steps
  - Evaluate overall electrical performance
- **Exploration and Innovation**
  - Creative research into new approaches



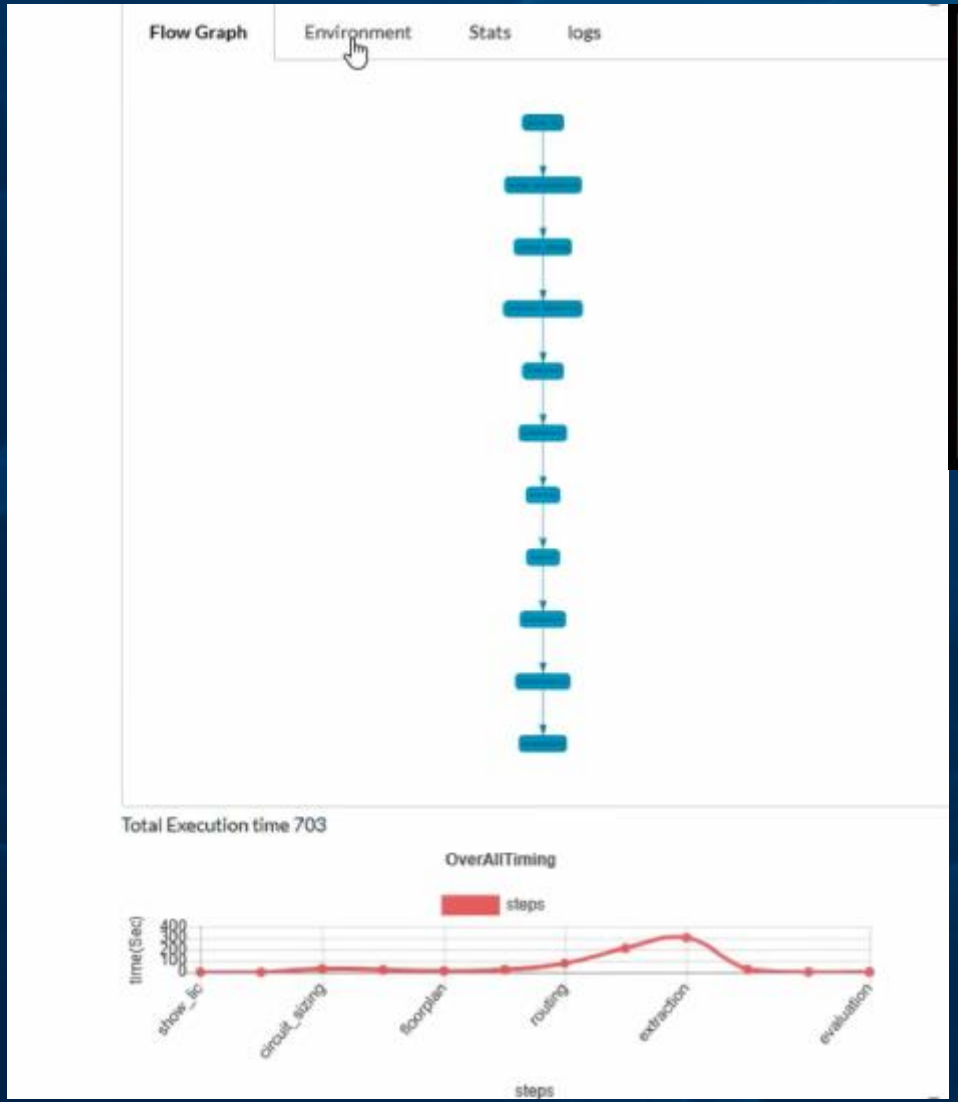



| | Original CRAFT GF14 sub-ADC + Comparator circuit Schematic Only Simulation | CRAFT GF14 sub-ADC + Resized Comparator for yield Schematic Only Simulation | Original CRAFT GF14 sub-ADC (original Comparator) Post-Layout (CRAFT taped-out) Simulation with extracted parasitics | CRAFT GF14 sub-ADC (original Comparator) Post-Layout (MAGESTIC-created) Simulation with extracted parasitics | CRAFT GF14 sub-ADC (resized Comparator) Post-Layout (MAGESTIC-created) Simulation with extracted parasitics |
|---|---|---|---|---|---|
| Comparator Yield (Process Corners/Mismatch) | 62% | 99% | 55% | 51% | 100% |
| Comparator Yield (across Vdd/Temp) | 58% | 99% | 52% | 47% | 100% |
| Effective Number of Bits (ENOB) | 5.87 | 6.64 | 5.47 | 5.70 | 6.15 |

ML based yield improvements

Within design metrics, better yield

Integrated Flow




Analog Circuit

Analog Circuit Sizing

Floorplanning

**Placement**

Routing

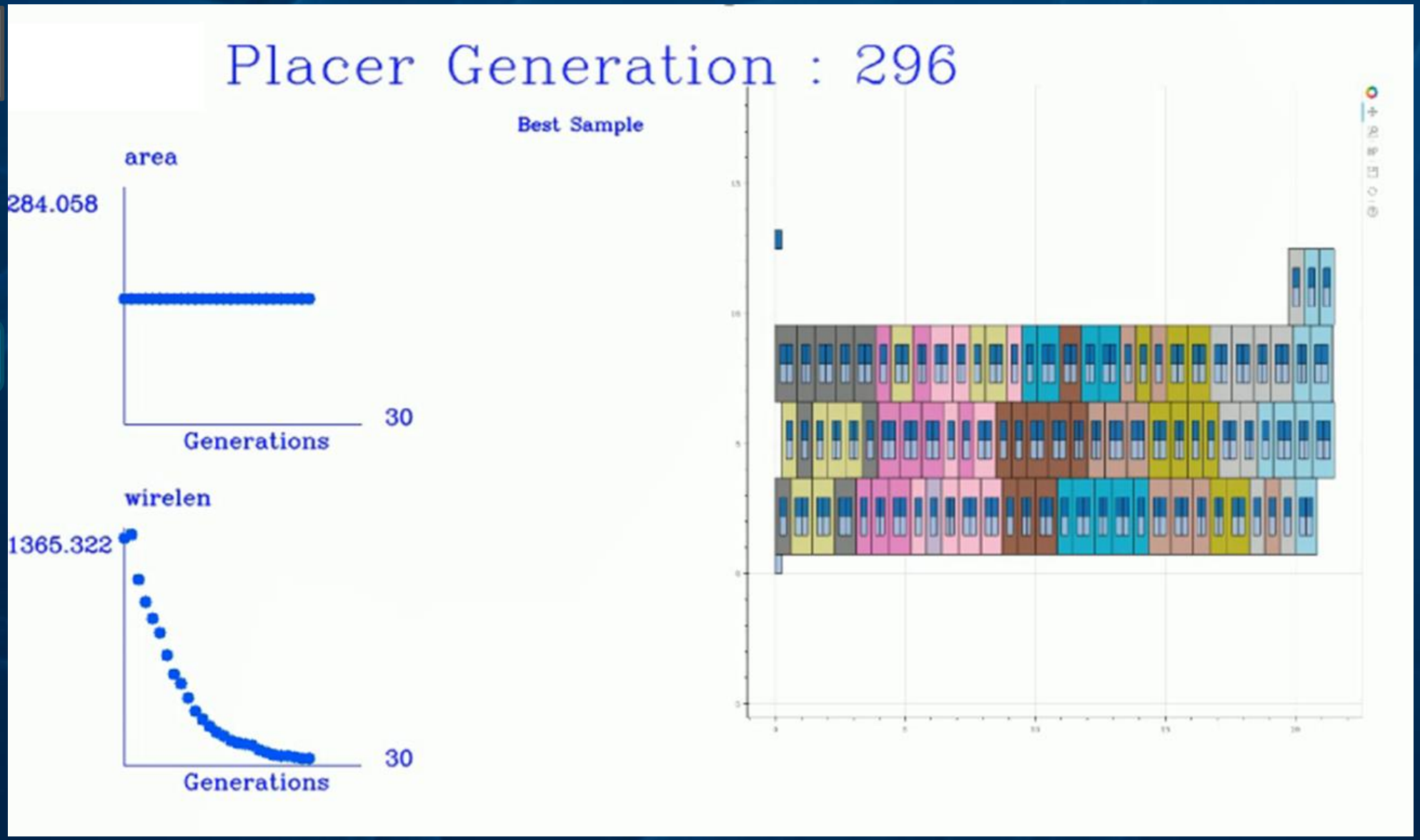
Layout Finishing

Verify & Extract

Electrical Performance

Analog Layout

Integrated Flow





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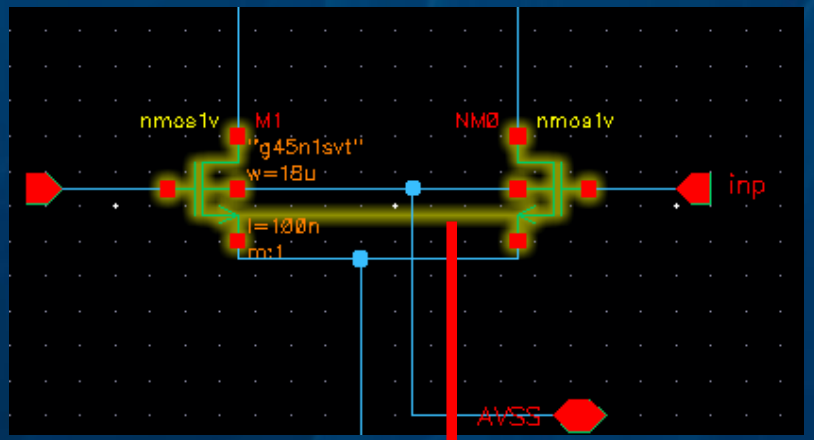
# Layout Group Prediction Problem

- It is common practice for layout designers to group devices that need good matching
  - Grouped devices are placed closely together, and there may be interdigitation




- Grouping decisions are largely made from experience
  - *Even simulation cannot fully predict effects of grouping*
  - Can we learn them from good hand-crafted layouts?

| | |
|---|---|
| M0.1 | M1.1 |
| M1.2 | M0.2 |

- To formulate a machine learning problem, we need to define grouping as a label and predict it from schematic features

Analog Circuit

Analog Circuit Sizing

Floorplanning

Placement

Routing

Layout Finishing

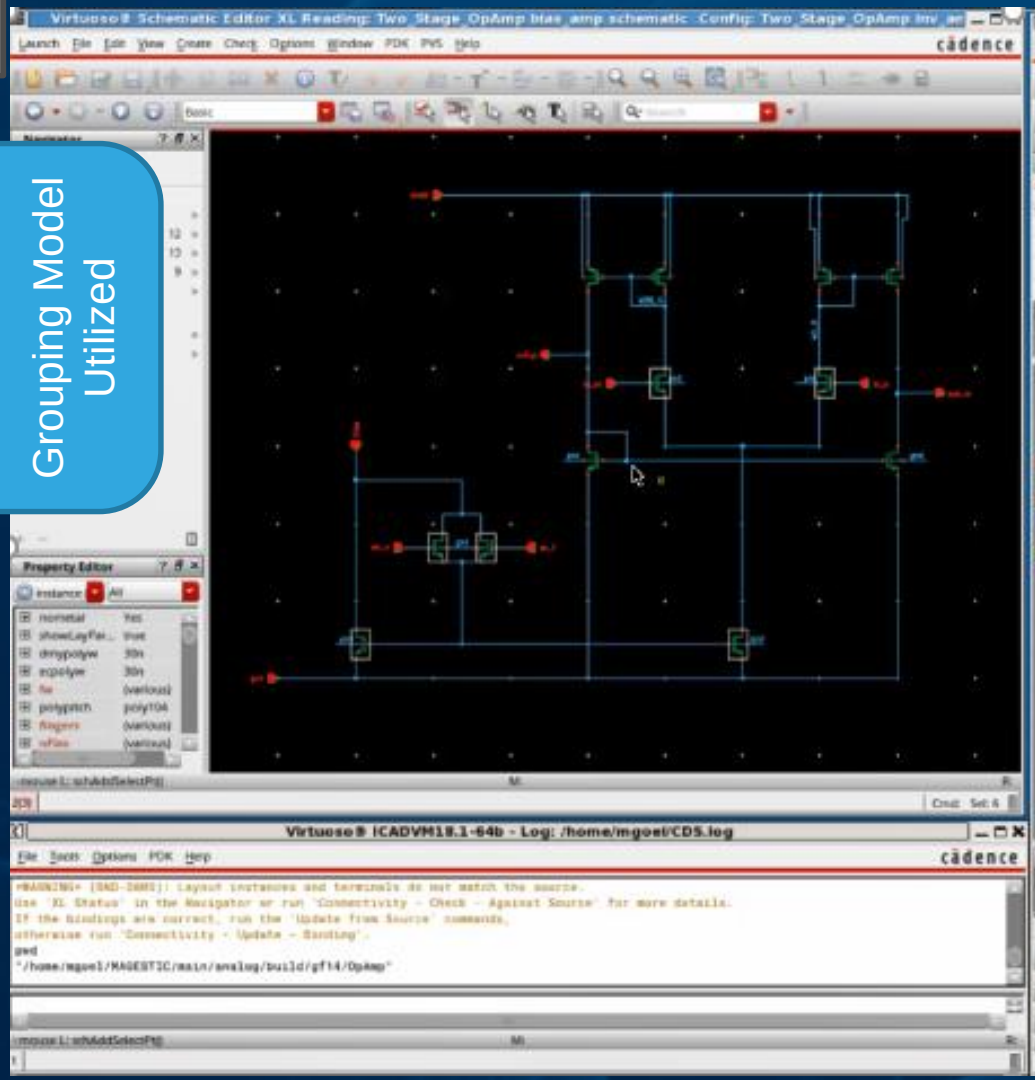
Verify & Extract

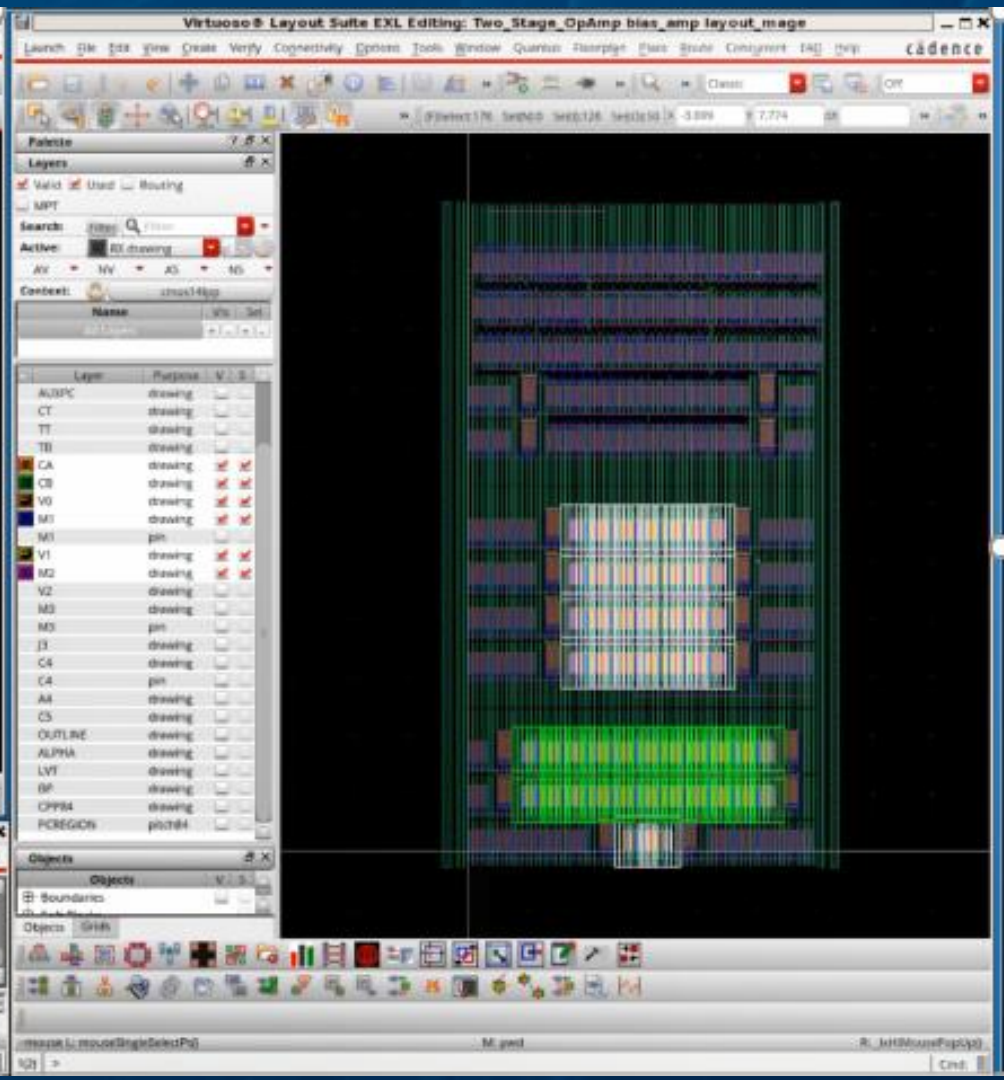
Electrical Performance

Analog Layout

Grouping Model Utilized

Integrated Flow





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# But Wait! There's More!

Exploration and Innovation

***Please stop by during the IDEA Integration Exercise to see a demo or discuss in more detail many of our other exciting projects***

## Parasitic Prediction

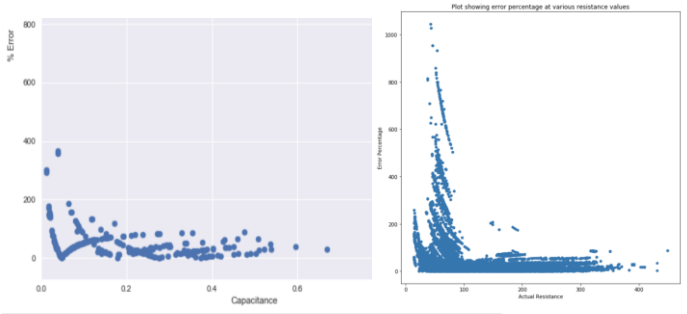
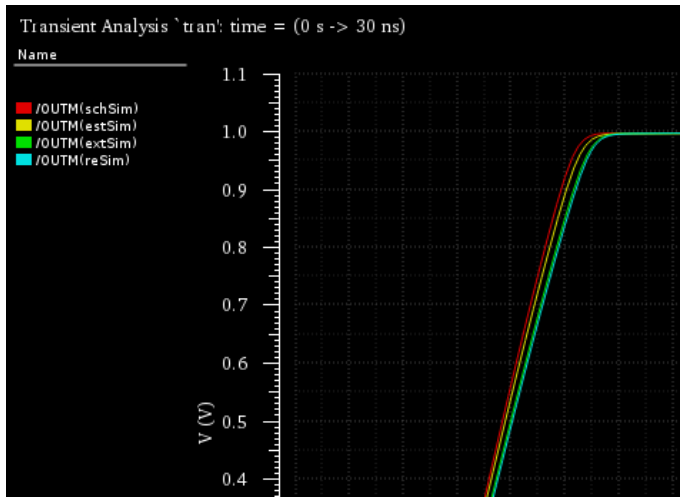
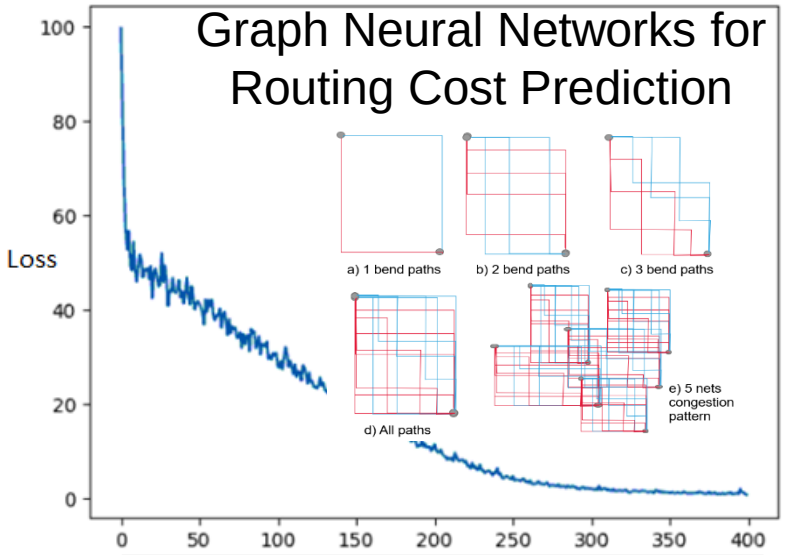
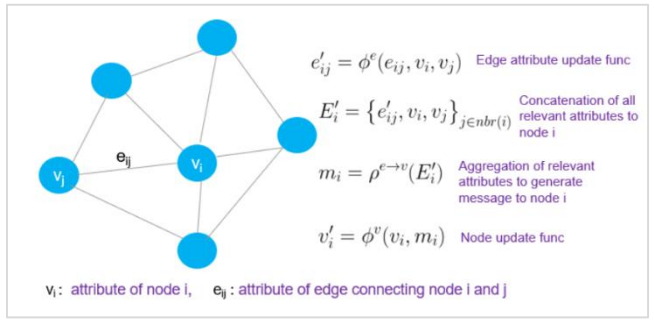



Figure 3.13 Actual Capacitance v/s Error Percentage plots across all nets.

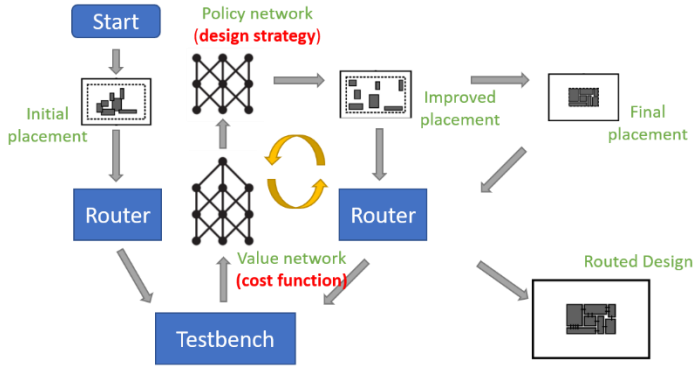


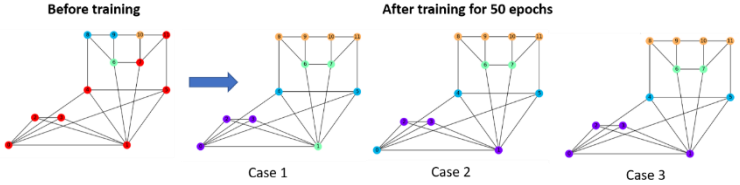

## Graph Neural Networks for Routing Cost Prediction



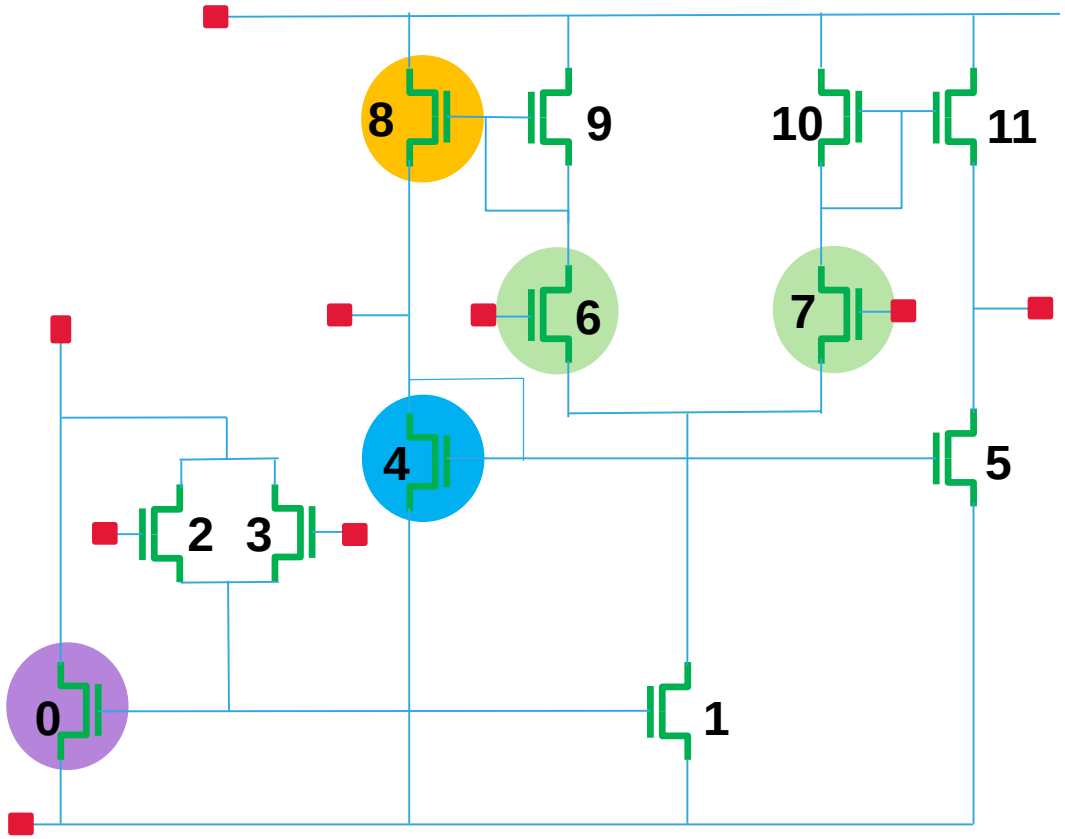

## AlphaRoute / AlphaAnalogDesign Updates



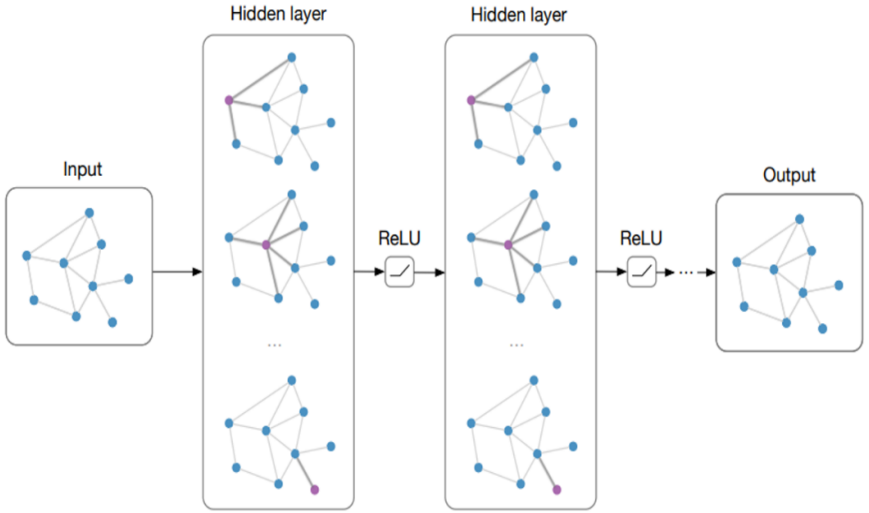



# Grouping Cold Start Problem






**Graph Convolutional Network** (GCN)
Representation of Circuit

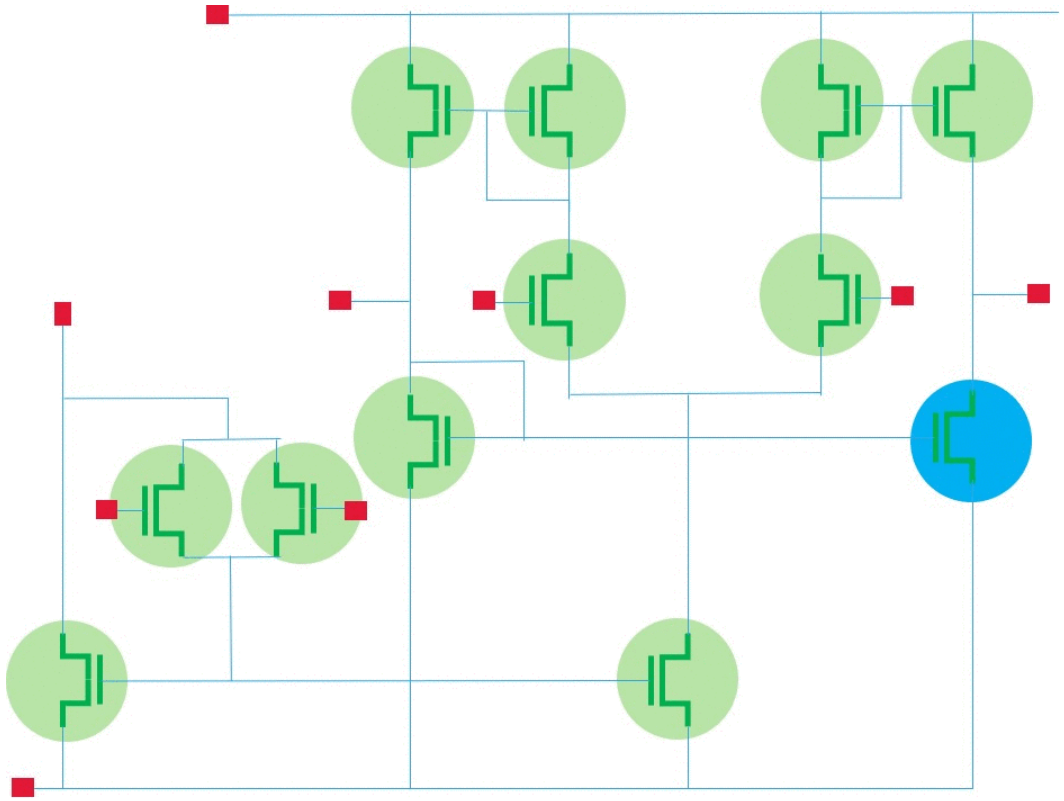



Suppose we are given the following (sparse) labels:

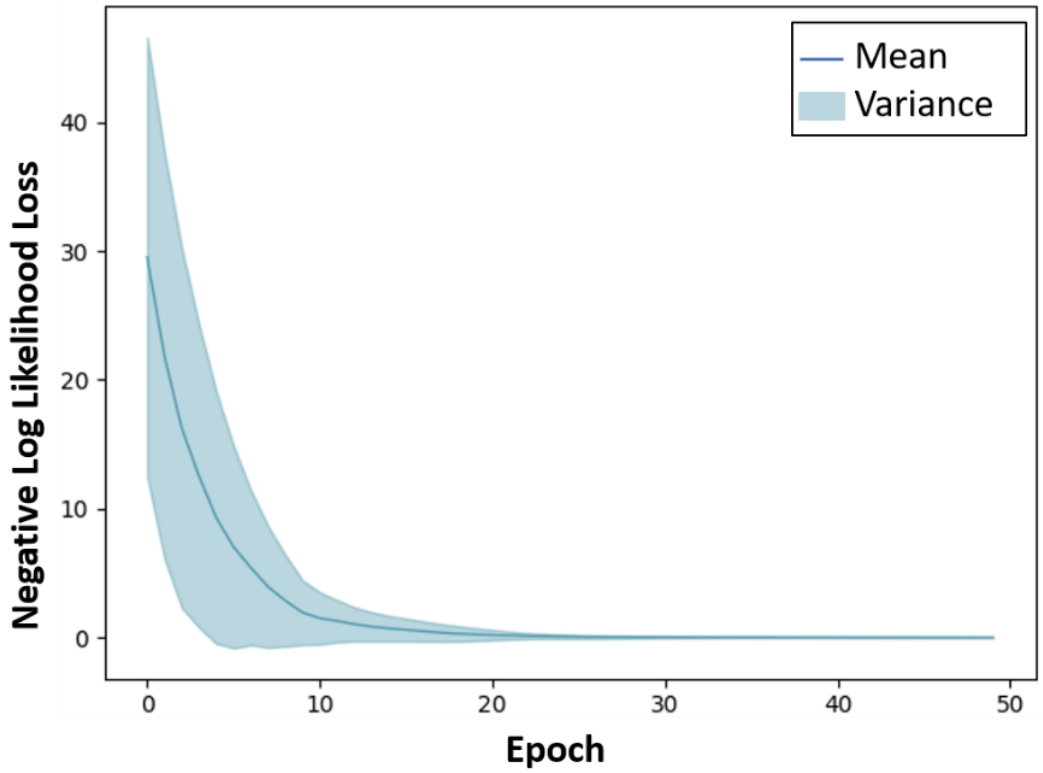
- Transistor 0, 4, 6, and 8 will be in *different* groups
- Transistor 6 & 7 belong to the *same* group

Can we train a reasonable grouping model using the netlist information?

# GCN Training for Grouping Cold Start Model



Epoch 0




The learning curve of 10 runs, each with a maximum of 50 epochs

# Cadence Design Systems, NVIDIA and Carnegie Mellon University

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