## ERI Design: IDEA and POSH Rapid Modeling and Analysis Framework for Full-Chip/Package/Board Layout Automation

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#### IDEA and POSH Integration Exercise and PI Review Detroit, MI

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 Software for rapid and first-principle-accurate full-chip/package/board layout modeling and analysis, to guide layout generation in a fast turnaround time.







Existing Layout Modeling & Analysis

#### Modeling:

 Static-based C, RC, and RLC models fail to capture distributed, 3-D, global effects even at low frequencies; inaccurate at high frequencies; expensive at large scale
 Full-wave-based models are accurate, but expensive in large-scale extraction

#### Analysis:

Extraction is involved even though simulation is the end goal
Inherent difficulty in fast circuit simulation due to extracted parasitics
No embarrassingly parallel solution
Accurate analysis of full-chip/package/board layout can take years, and may be infeasible

#### Proposed Layout Modeling & Analysis

#### Modeling:

 ✓ RLC-compatible and computation-free representation of the layout has firstprinciples accuracy
 ✓ Algorithm breakthroughs allow fullchip/package/board parasitic extraction done in a few hours

#### Analysis:

- ✓ Extraction is bypassed
- ✓ Computation-free decomposition of the full-wave solution into RC- and RL-/full-wave components; optimal-complexity direct solutions for finding each
- $\checkmark$  Embarrassingly parallel solution
- ✓ Full-chip/package/board layout in one day





Subtask 1. Rapid Extraction-Free Full-Chip/Package/Board Layout and Circuit Simulator

Prevailing flow



**Circuit Simulation** 

### Problems:

- At which frequency to switch between these models?
  - Physical layout has never changed from this frequency to the other frequency, it is the model that has changed.
  - What is the true broadband model of the layout?
- Even at LF, how to connect RC with L elements, etc. to capture 3D effects, and distributed effects correctly?
- Static solvers are inaccurate at high frequencies
- If using a full-wave solver for all frequencies, it is not efficient either for statics-dominated circuits
- When layout is large, extraction is computationally expensive; the large number of extracted circuit elements further makes fast circuit simulation difficult



## Proposed flow: Layout is our spice netlist

```
.tran 5.0ps 20ns

.param

+ vdd_val = '1.2'

.....

.layout

xxxx.gds

.....

.probe v(data_in) v(data_in_agg) v(data_in_agg2)...
```

Output: Voltage and current anywhere in the layout in FD and TD



#### Subtask 2. Parasitic Extraction at Full-Chip/Package/Board Scale

#### **Intel CPU**





#### Facebook Wedge 100 board

- The input of our parasitic extraction tool can be a GDS file, describing the geometrical and material information of the layout.
- The output is Z-, S-, and any network parameters at the ports/pins of interest in the layout



Input: Layout file in .gds, etc.

Output:

.spef .Network parameters such as Z-, Y-, Sparameters .cir .sp



Subtask 3. Power and Signal Integrity Analysis



We will provide a rapid power analysis and signaling analysis to ensure power and signal integrity of the layout.



# Demo of Layout Analyzer — gds2Para

## Li Xue, Michael Hayashi, and Dan Jiao

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OpenSource at GitHub:

https://github.com/purdue-onchip/gds2Para



## **Parasitics Extraction Flowchart**





## **GitHub Repository Activity**

or jump to	Pull requests Issues Marketplace Expl	ore	
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## Visit <a href="https://github.com/purdue-onchip/gds2Para">https://github.com/purdue-onchip/gds2Para</a>



## **Example 1: Test-chip Interconnect**



## Cross-sectional view of a test-chip interconnect



## Example 1: Agree well with measured data





## **Example 2: Scan D Flip-Flop Layout**



Top view of the structure in layer 9, 10, and 11 Total number of unknowns: 3,616,773



## **Example 2: Scan D Flip-Flop Layout**

Current source:

Gaussian derivative with  $\tau = 10^{-11} s$ 

Proposed method

 $\Delta t = 10^{-12} \, \mathrm{s}$ 

It takes 34.02 s

Traditional method

 $\Delta t = 10^{-17} \text{ s}$ It takes 6.9 × 10<sup>6</sup> s



## Example 4: Facebook Wedge 100



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#### • Dan Jiao's team



#### Dan Jiao

- Professor and IEEE Fellow
- Specialized in computational electromagnetics, microwave and integrated circuits CAD
- PhD, UIUC, 2001
- 2001-2005, Intel's circuit modeling group, responsible for BKM tools for interconnect, package, and board modeling and simulation
- 2005-present, Purdue ECE, perform research crosscutting EM and circuits



#### Three graduate students

- Li Xue
- Miaomiao Ma
- Michael Hayashi





Miaomiao Ma (Fast solvers)

## Michael Hayashi



(I/O, power and signal integrity analysis)

## Li Xue (Layout modeling and analysis)