ORDER: Open-Source Rooted Design Experts with Repute

Integration Meeting July 2019
Princeton University and
University of Washington
SoC Design Advisor Team

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Earliest research on Dark Silicon, Tiled Multicore, ASIC Clouds RISC-V manycore
OpenCelerity and BaseJump open source projects
ORDER Project Overview

• Fulfill role of SoC Design Advisors to help DARPA create a pushbutton CAD technology that accelerates the rate of progress by making chip design easier
• Independent team of hardware design experts with a strong track record in open source and open collaboration, and design in advanced process nodes
• Provide requirements, feedback, designs, and real world design experience to TA-1 toolflow teams
• Build and Fabricate Chips, Boards, and SiP Package using IDEA tools
Building Open Source SoCs with IDEA Tools

We are excited to use your tools!
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Image Credit: DARPA IDEA BAA
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Outline

- **Benchmarks**
  - OpenPiton Design Benchmark
    - Demo
  - BSG Pipeclean Testsuite
  - UW Idea Analog Test Cases

- **Tools and Formats**
  - IDEA Dimensionless Format (IDF)
  - SV to Verilog
    - Demo
Enabling IDEA Through Convenient Benchmarks

World’s first release of hundreds of high-quality, open-source, self-contained (Pickled into single file) hardware designs.

• Creation of “Pickling” flow to generate hundreds of easy to ingest HW designs.
• Release of high quality, complex, open-source HW designs supporting IDEA tool developers.
  – OpenPiton Design Benchmark
  – IDEA Analog Test Cases
  – BSG Pipeclean Suite

Challenges Addressed:
• HW designs require users to use complex build flows/infrastructure. Our “Pickled” designs enable CAD tool designers to only look at one file.
• CAD tool designers are in dire need for high-quality, non-trivial, open-source designs. We provide hundreds.
OpenPiton Design Benchmark

- Based on the OpenPiton open-source research processor
- 24 different modules
  - Variety of sizes, functionalities, core counts
- 636 “pickled” Verilog designs
  - Instantiation of modules with different configuration parameters
- Includes floorplan and .sdc files for multiple configurations
- Built “pickling” tool (Tursi) using FuseSoC

https://github.com/PrincetonUniversity/OpenPiton
https://github.com/PrincetonUniversity/OPDB
OpenPiton Design Benchmark Open Source Tools Demo

1. Create single “pickled” file of dynamic node module using Tursi (FuseSoC + Icarus Verilog)
2. Synthesize “pickled” file with a given library using Yosys
3. Compile playback driver module and synthesized pickle file into an executable using Icarus Verilog
4. Simulation with test stimuli
IDEA Analog Test Cases

https://github.com/uwidea/UW-IDEA_AnalogTestCases

- Collating pre-existing, developed for other projects, and developed for ORDER analog test cases into test suite
- Hierarchical schematics
- CDL files describe circuit (SPICE Netlist)
- Documentation and simulation results to enable others to match results
- Working to extend to larger test suite
- Exercising IDEA tools from: Purdue, Sandia, UMinn, UT-Austin
BSG Pipeclean Benchmark Suite

https://github.com/bespoke-silicon-group/bsg_pipeclean_suite

small_comb: 8 bit multiplier
medium_comb: 32-bit multiplier
large_comb: 128-bit multiplier

black_parrot_be_only_2019_03_11: Back end (be) of early version of black parrot
black_parrot_fe_only_2019_03_11: Front end (fe) of early version of black parrot
black_parrot_2019_03_28: Entire Black Parrot RISC-V core with reduced size crossbars
  Less challenging routing problem
black_parrot_2019_03_11: Entire Black Parrot RISC-V core with full crossbars
  More challenging routing problem

All of these designs work with commercial tools; use IDF dimensionless format
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Refining the IDF (IDEA Dimensionless Format)

New technology allowing open-source collaborators to share physical design descriptions of chips “in the clear” without violating NDAs.

- IDEA Dimensionless Format (IDF)
  - Simple, coherent coarse floorplan spec allowing open-sourced physical design constraints.
  - Dimensionless = All units are PDK agnostic revealing no sensitive info (NDA safe)
  - IDF-to-DEF converter for turnkey integration into existing CAD tool infrastructure and EDA vendor compatibility.
    - 30.7s to go from IDF file to floorplan in IC Compiler for TSMC 40nm.
- Challenge: IDF excels at moving between similar PDKS but moving between dissimilar PDKs (process node, SRAM compiler) will require the intelligence of a tool like OpenROAD to adjust.

https://github.com/bespoke-silicon-group/bsg_idf_tools

IDF specified in collaboration with UW (Taylor), Princeton, Michigan, Andreas, and Greater IDEA Team from San Diego Meeting
Providing A Pathway for SystemVerilog to Open Source

First open source conversion infrastructure to allow academics to export modern HW designs in SystemVerilog for use with open-source tools.

- **SystemVerilog to Verilog RTL Converter (bsg_sv2v)**
  - Converts cutting edge hardware designs written in SystemVerilog (SV) to a single Verilog 2005 compliant RTL file for maximum compatibility with currently available open-source CAD tools.
  - Extensible framework for post-converted optimizations.
    - Reg-Redux: For a CPU frontend, improved VCS sim speed by 2.3x and LoC by 2.8x over un-optimized pickled netlist.

- **Challenge:** Tools may differ in their interpretation of SystemVerilog. We use Design Compiler as our parser since all academics have it, and it is the industry standard, and post-process the output to regenerate Verilog.

**Open-source CAD Tools**

- Verilator
- Icarus Verilog
- YOSYS
- Design Compiler

**Commercial CAD Tools**

- VCS

https://github.com/bespoke-silicon-group/bsg_sv2v

UW (Taylor)
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- OpenPiton Design Benchmark - https://github.com/PrincetonUniversity/OPDB
- UW IDEA Analog Test Cases - https://github.com/uwidea/UW-IDEA_AnalogTestCases
- System Verilog to Verilog Flow https://github.com/bespoke-silicon-group/bsg_sv2v
- OpenPiton GitHub - https://github.com/PrincetonUniversity/openpiton
- Open Celerity - http://opencelerity.org
- BaseJump - http://bjump.org
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