ERI Design: USC POSH

Automated Analog Mixed Signal (AMS) IP generator for CMOS technologies

FA8650-18-2-7853

Under contract June 25, 2018. Phase IA completed June 24, 2019

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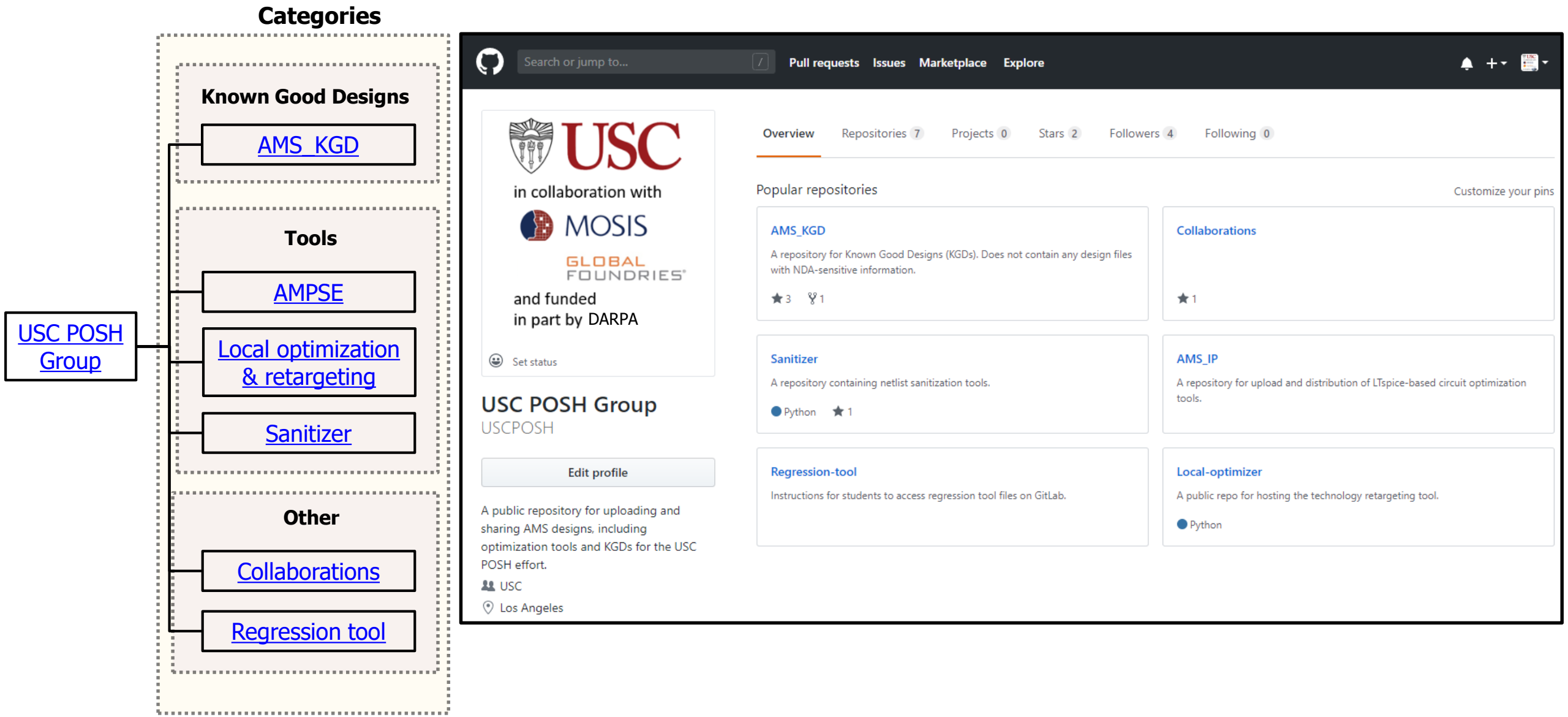
University of Southern California

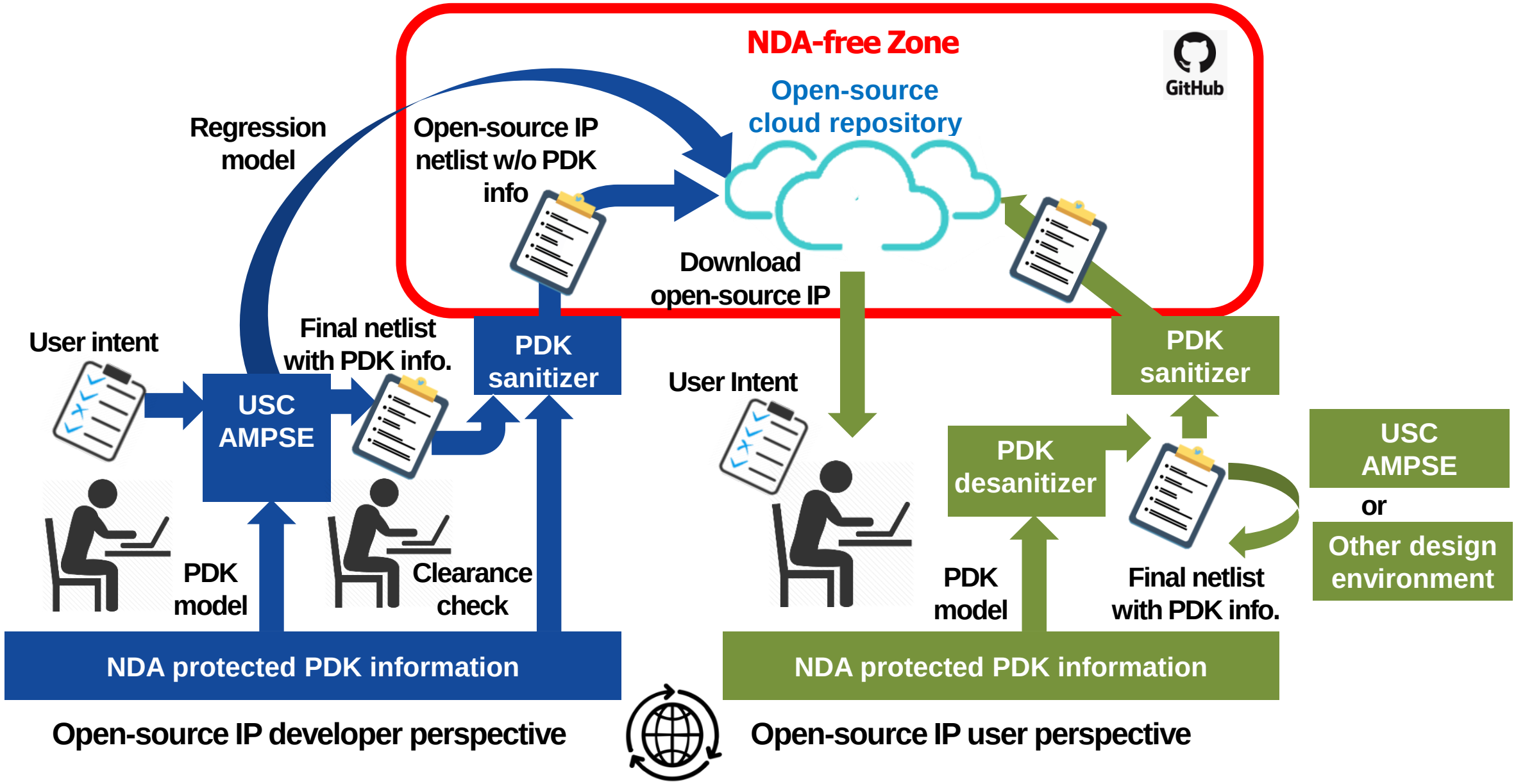
ERI Detroit meeting

3.40pm, Wednesday July 17, 2019

Public open-source USC POSH repository, https://github.com/USCPOSH



Traversing NDA-protected and NDA-free zones



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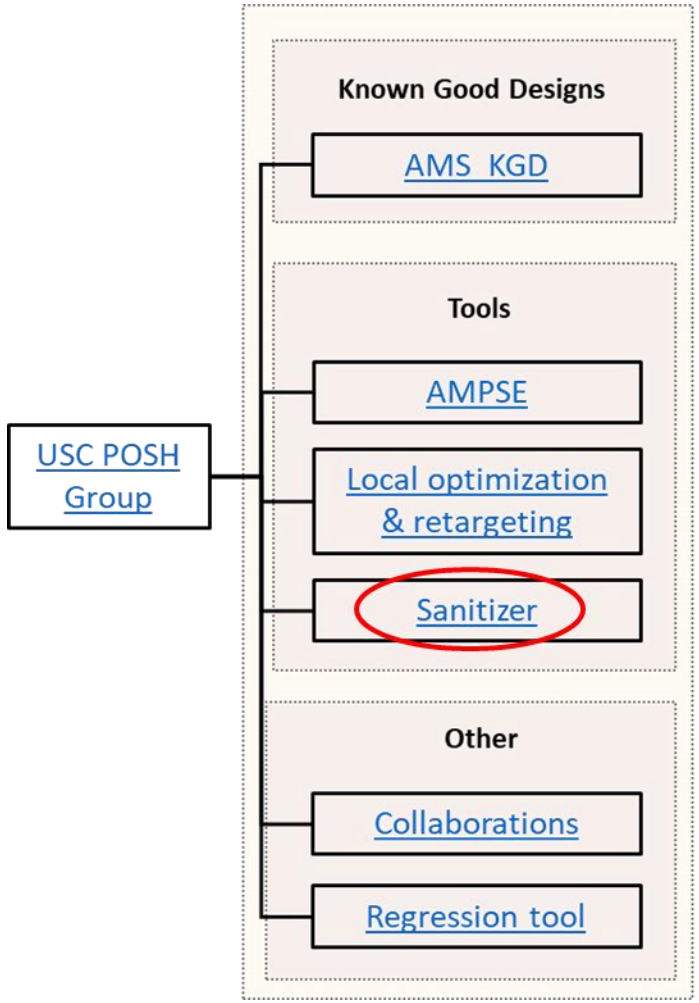

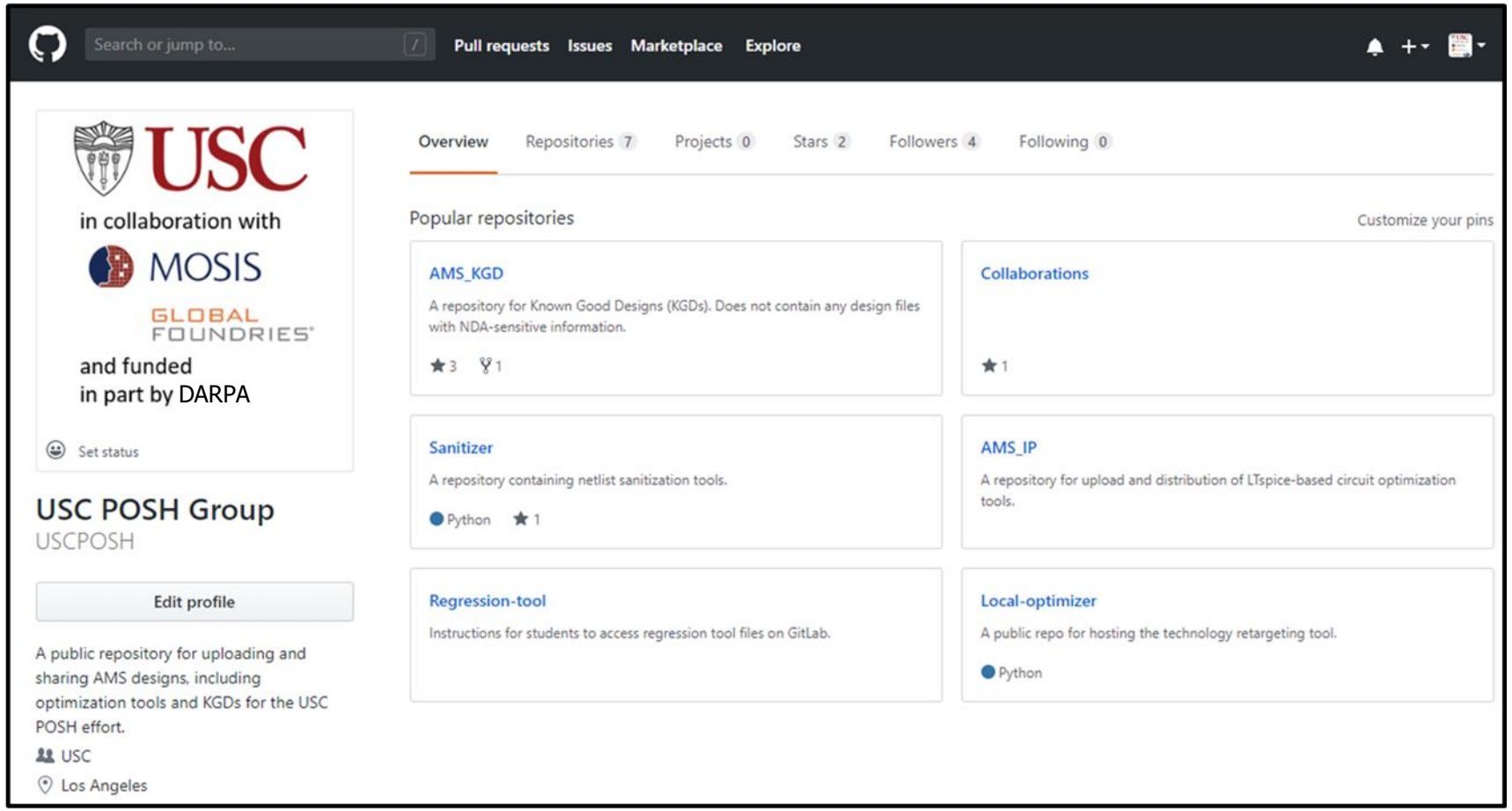

Traversing NDA-protected and NDA-free zones with sanitization

Sanitization

Netlist with PDK information (GF65)

```
subckt INV65_v1 IN OUT VDD VSS
    M1 (OUT IN VDD VDD) p### l=lppp w=wppp*mp m=1 nf=mp\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************
    M0 (OUT IN VSS VSS) n### l=linnn w=winnn*mn m=1 nf=mn\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************
ends INV65_v1
// End of subcircuit definition.
```

Eliminating PDK information (NMOS / PMOS)

Sanitized Netlist

```
subckt INV65_v1 IN OUT VDD VSS
    M1 ( OUT IN VDD VDD ) p### l=lppp w=wppp*mp m=1 nf=mp
    M0 ( OUT IN VSS VSS ) n### l=linnn w=winnn*mn m=1 nf=mn
ends INV65_v1
```

Desanitization

Sanitized Netlist

```
subckt INV65_v1 IN OUT VDD VSS
    M1 ( OUT IN VDD VDD ) p### l=lppp w=wppp*mp m=1 nf=mp
    M0 ( OUT IN VSS VSS ) n### l=linnn w=winnn*mn m=1 nf=mn
ends INV65_v1
```

Adding PDK information necessary for accurate simulations

Netlist with PDK information

```
subckt INV65_v1 IN OUT VDD VSS
    M1 (OUT IN VDD VDD) p### l=lppp w=wppp*mp m=1 nf=mp\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************
    M0 (OUT IN VSS VSS) n### l=linnn w=winnn*mn m=1 nf=mn\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
        ********************************************************************************\
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        ********************************************************************************
ends INV65_v1
// End of subcircuit definition.
```

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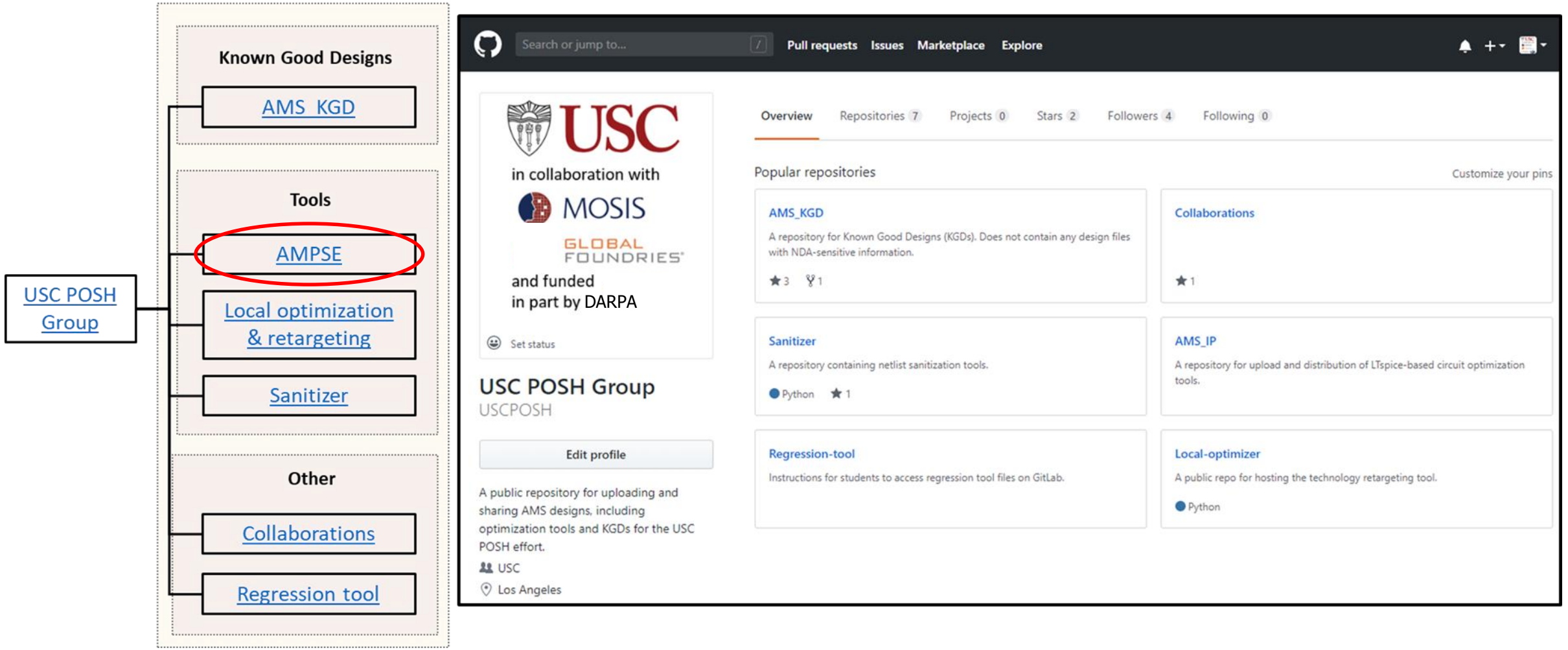
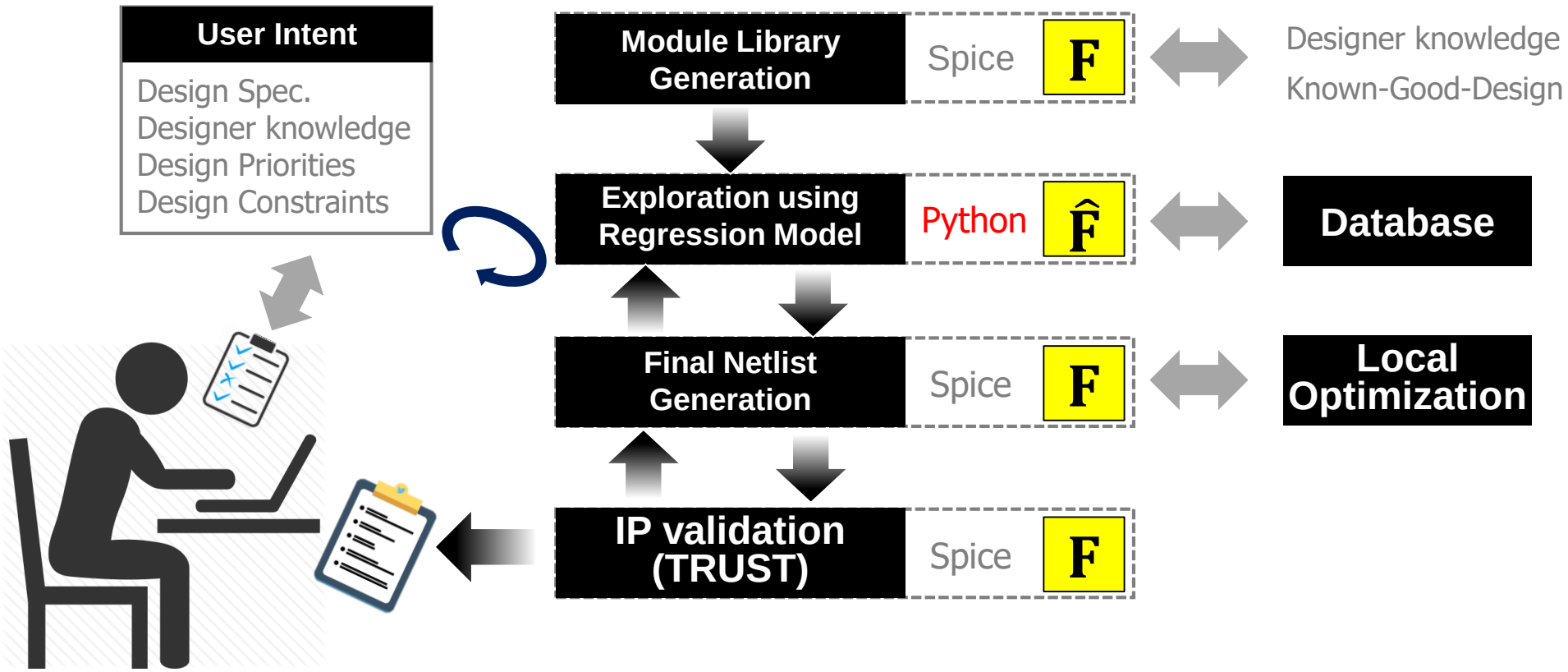
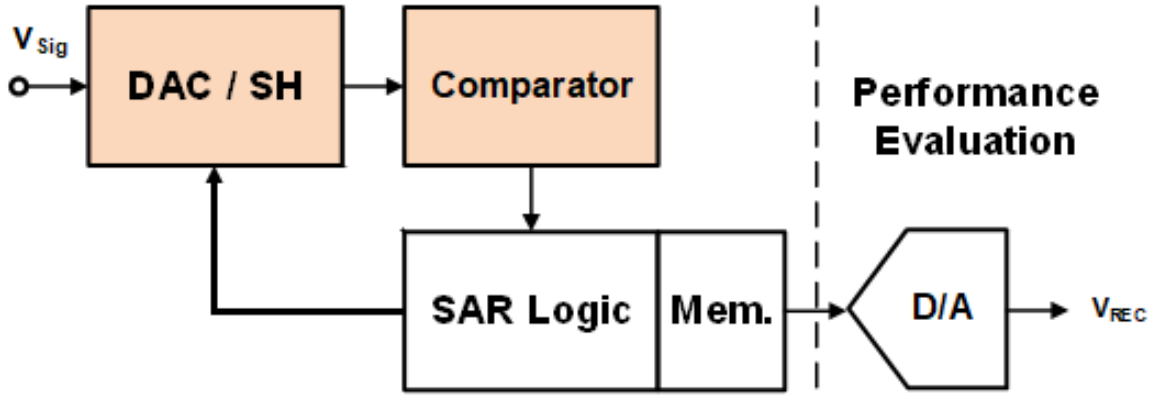


Analog Mixed-signal Parameter Search Engine (AMPSE) Design Flow



Expand AMS Design Space beyond single specification/technology for open-source (including Xyce) ecosystem

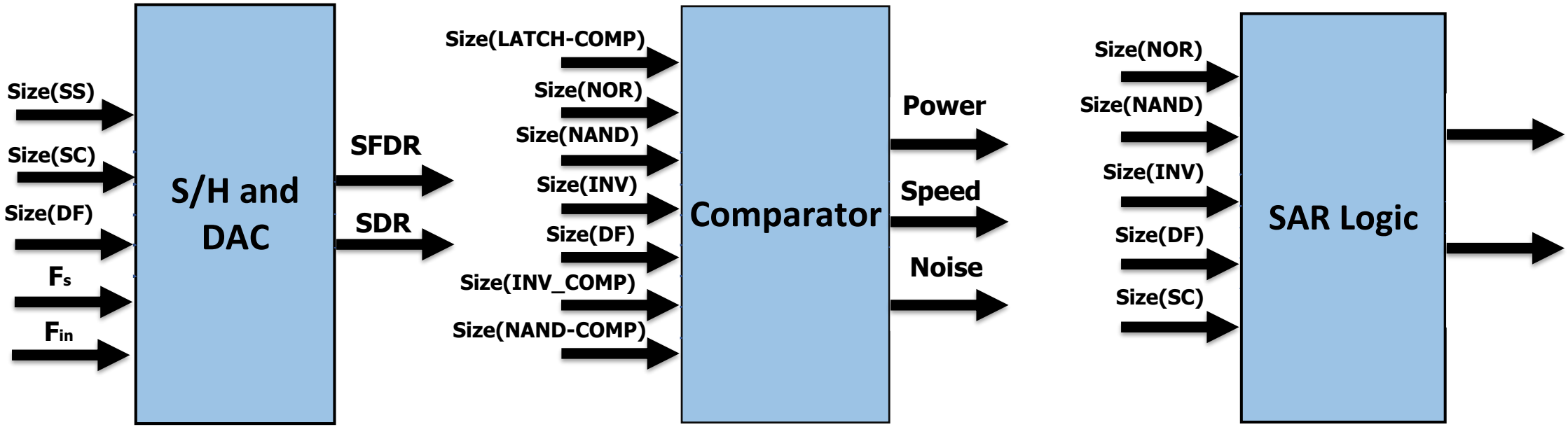
AMPSE design: SAR ADC



$$SNDR = \frac{\text{Signal [Full-Scale]}}{\text{Noise [S/H+DAC+COMP+Quantization]}}$$

$$PWR_{CORE} = \text{Power[COMP+CLK]}$$

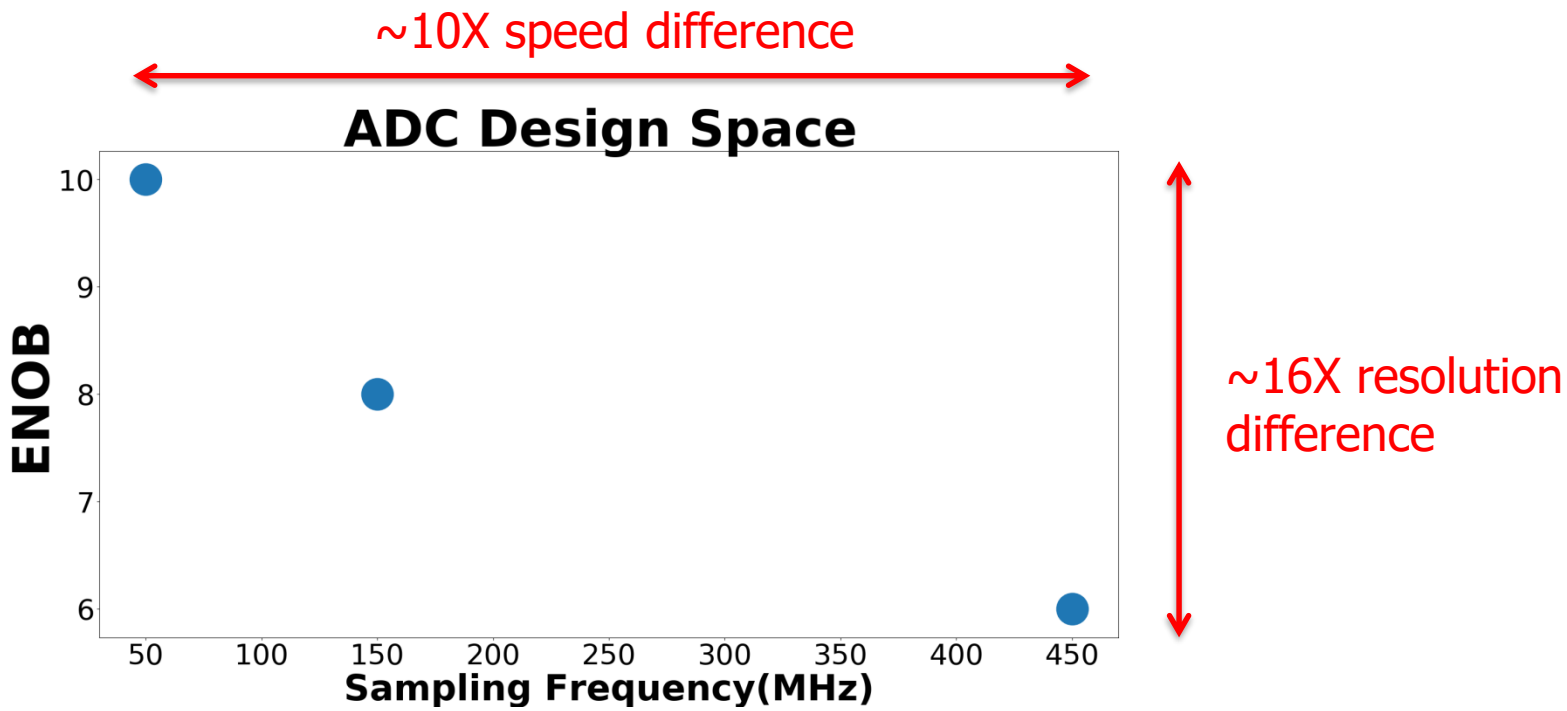
https://github.com/USCPOSH



Access broad range of design objectives

Let's try these…

- 50MS/s 10-bit SAR ADC
- 150MS/s 8-bit SAR ADC
- 450MS/s 6-bit SAR ADC



(1) $\sum T_{COMP,k} + (N-1)\cdot Max\{ T_{RS}, T_{DAC} \} < 75\% T_{period}$

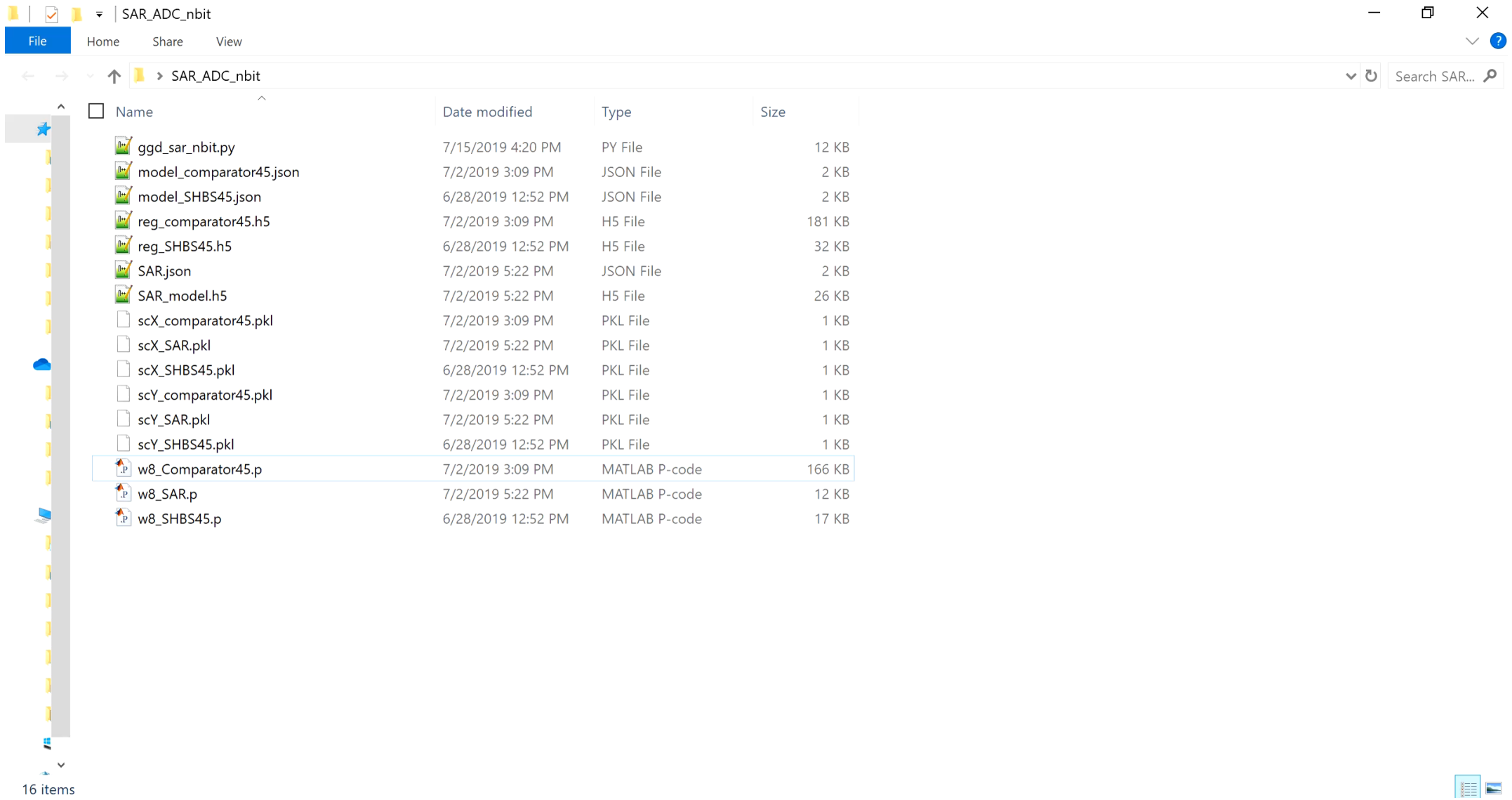
(2) $SFDR > SFDR_{target}$

(3) $SNDR > SNDR_{target}$

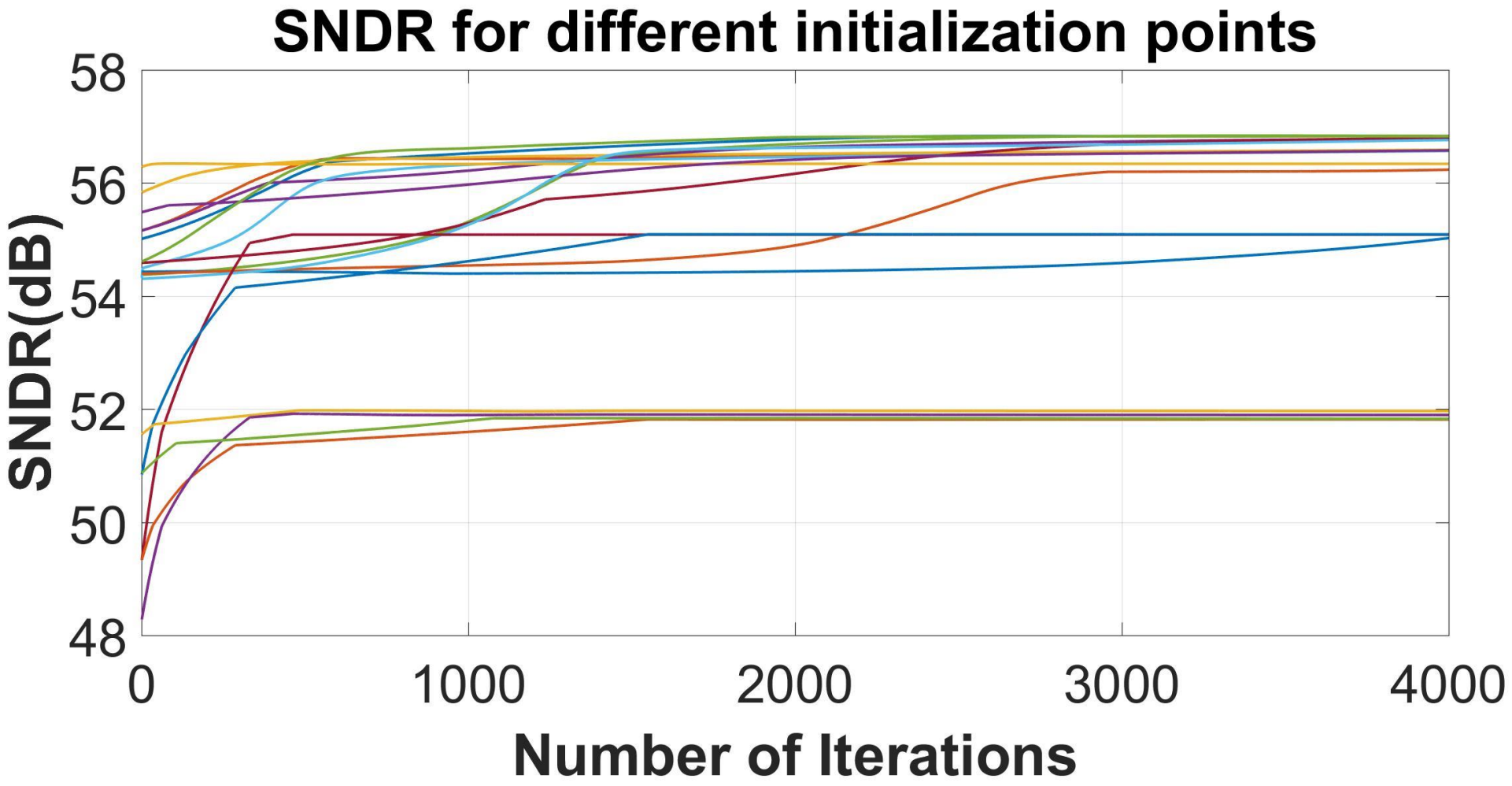
(4) …

Formulate corresponding constraints function for AMPSE

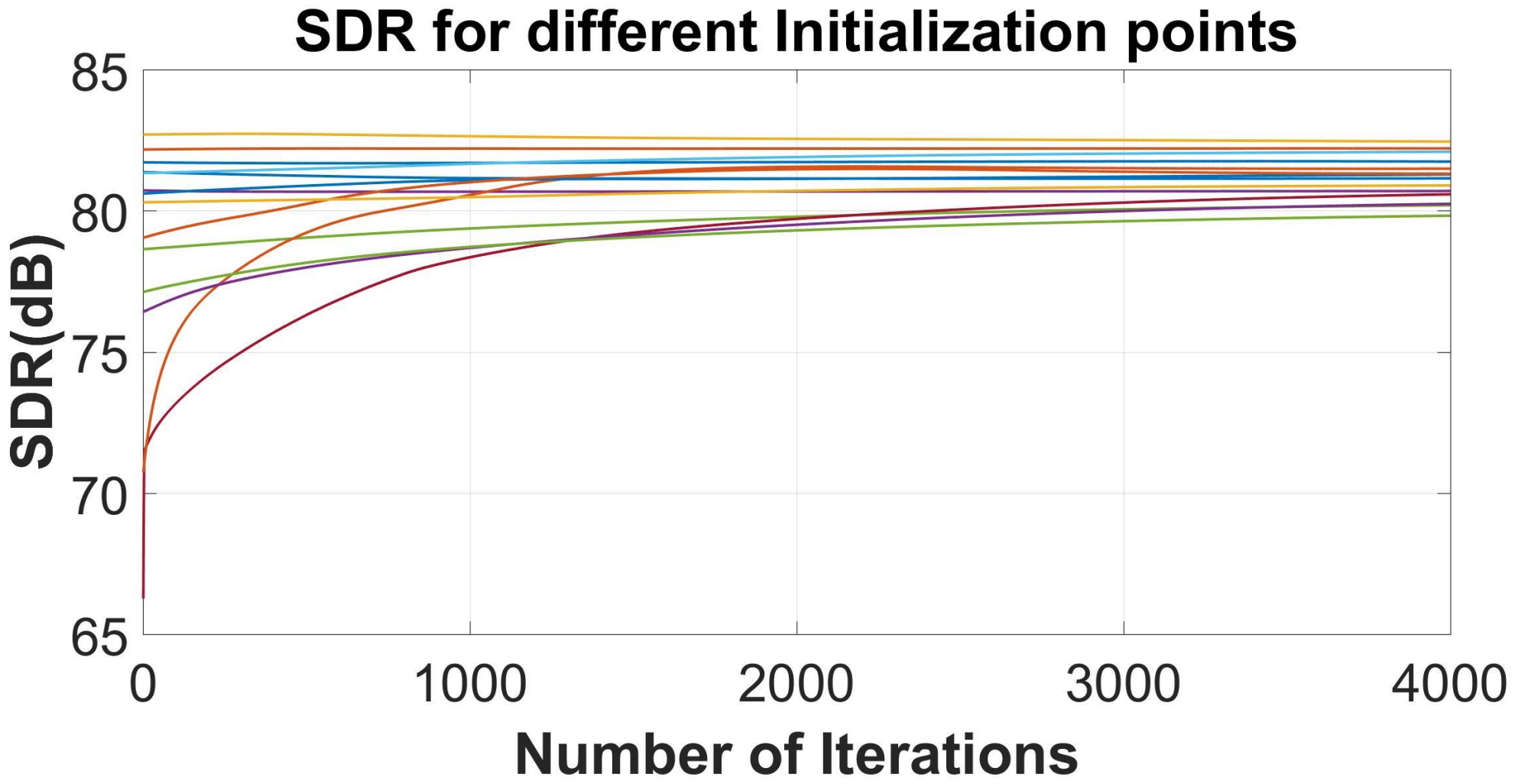
Use AMPSE for 10-bit ADC (schematic level)



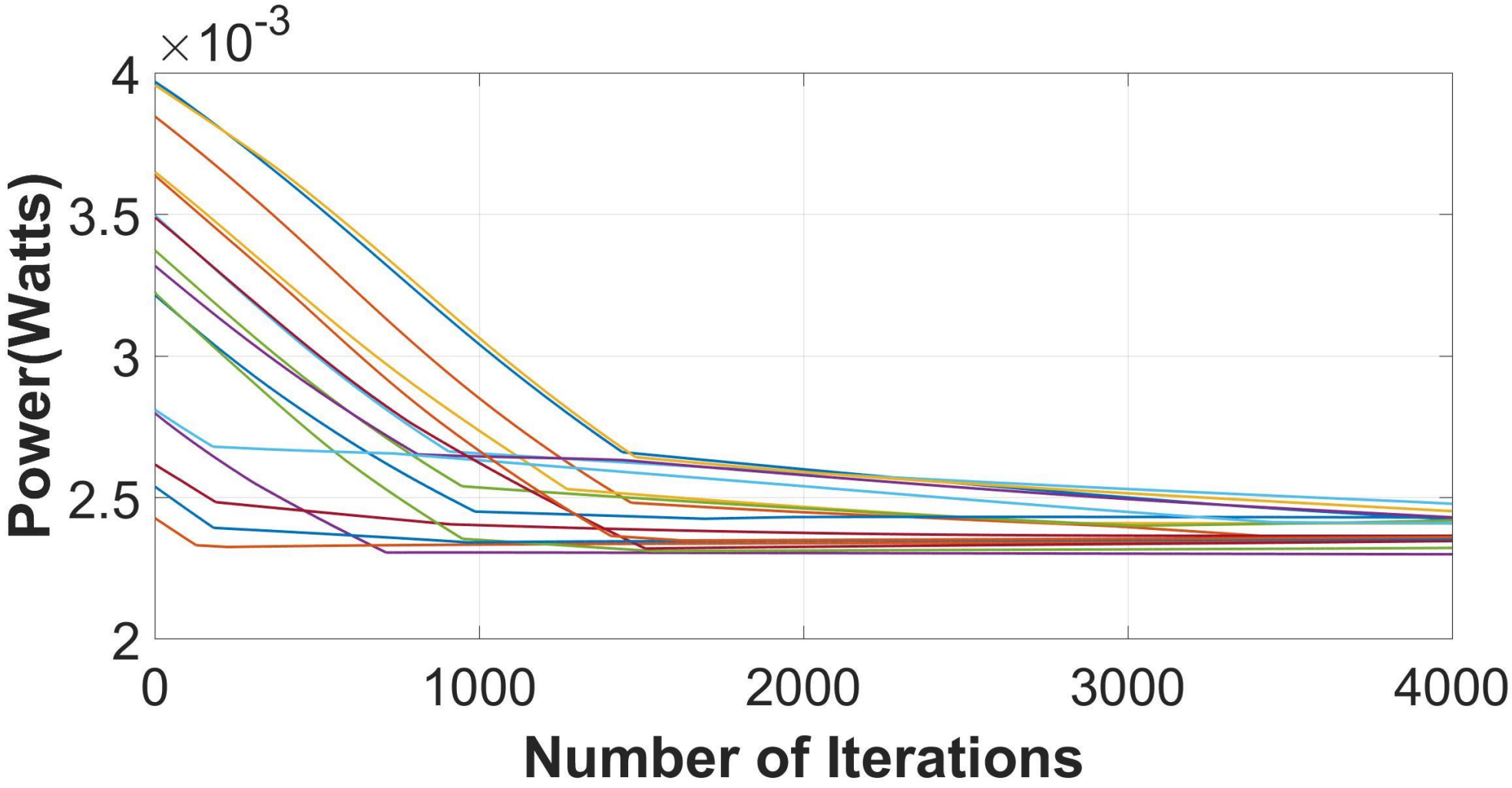
Parameter search process: 10-Bit SAR ADC design



Parameter search process: 10-Bit SAR ADC design



Parameter search process: 10-Bit SAR ADC design



SPICE validation of AMPSE design (schematic level)

- 50MS/s, 10-bit SAR ADC

Performance Metric	AMPSE design	SPICE Simulation
ENOB	9.14	8.5
SFDR	80.7dB(T/H Module)	60.15dB
Power Consumption	2.4mW	3.8mW

- 150MS/s, 8-bit SAR ADC

Performance Metric	AMPSE design	SPICE Simulation
ENOB	7.9	7.6
SFDR	70.76dB(T/H Module)	54.12dB
Power Consumption	4.43mW	6.7mW

- 450MS/s, 6-bit SAR ADC

Performance Metric	AMPSE design	SPICE Simulation
ENOB	5.9	5.3
SFDR	58.2dB(T/H Module)	41.2dB
Power Consumption	10.9mW	12.6mW

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