

ERI Design: USC POSH

Automated Analog Mixed Signal (AMS) IP generator for CMOS technologies

FA8650-18-2-7853

Under contract June 25, 2018. Phase IA completed June 24, 2019

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University of Southern California

ERI Detroit meeting

3.40pm, Wednesday July 17, 2019

Public open-source USC POSH repository, <https://github.com/USCPOSH>

Categories

Known Good Designs

[AMS_KGD](#)

Tools

[AMPSE](#)

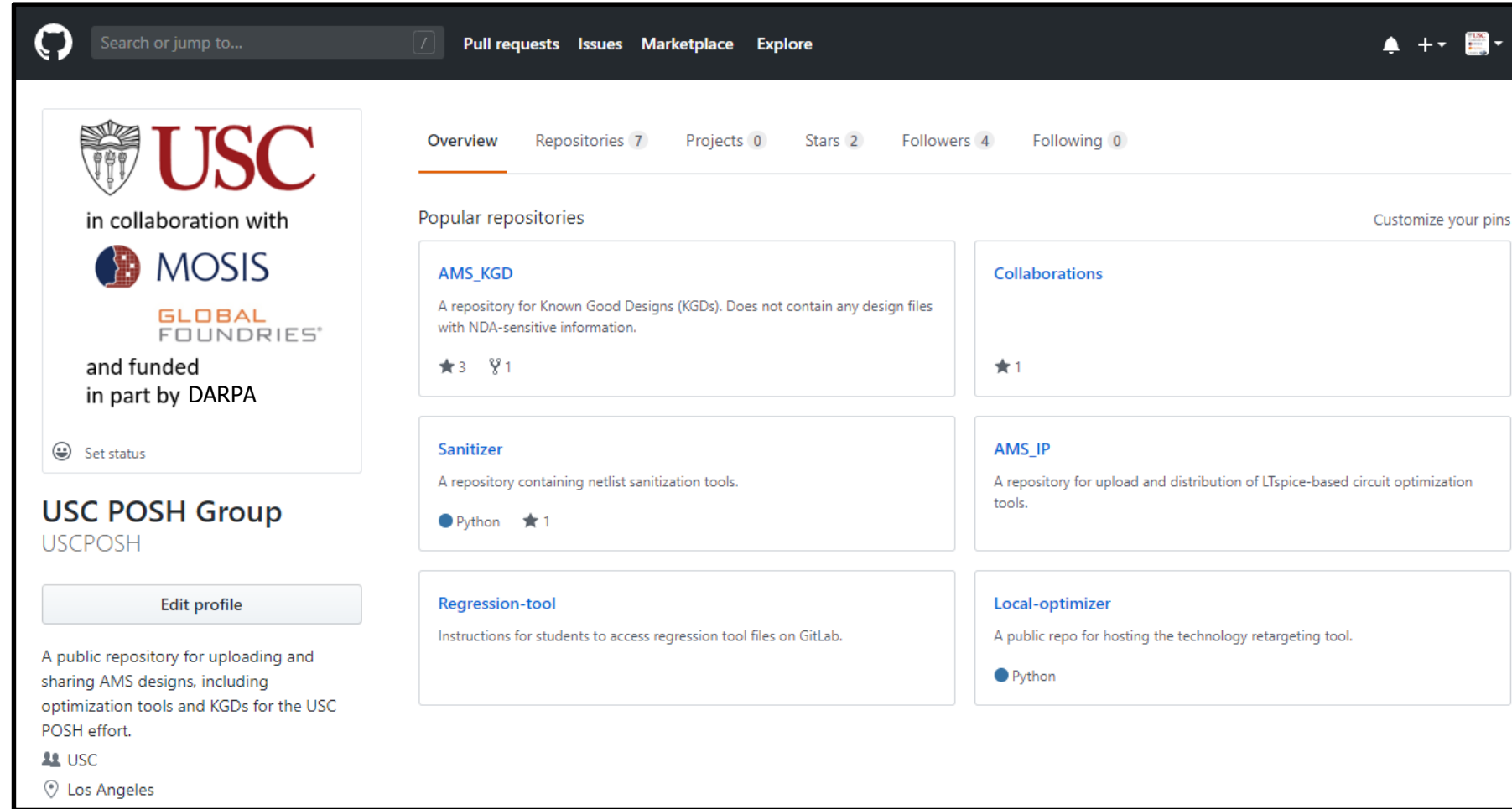
[Local optimization
& retargeting](#)

[Sanitizer](#)

Other

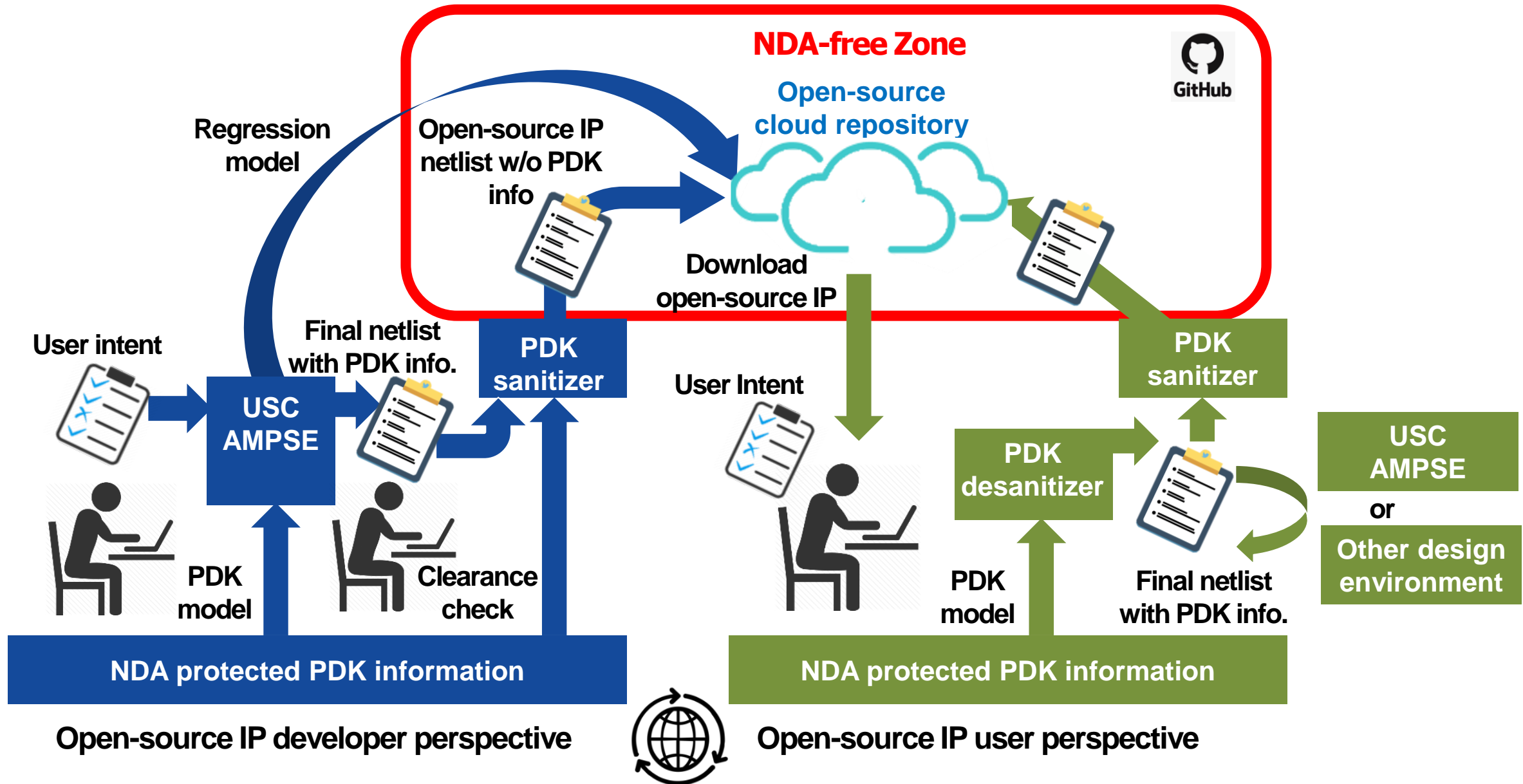
[Collaborations](#)

[Regression tool](#)



The screenshot shows the GitHub profile page for the USC POSH Group. The header includes the GitHub logo, a search bar, and navigation links for Pull requests, Issues, Marketplace, and Explore. The profile section features the USC logo, a collaboration with MOSIS and GLOBAL FOUNDRIES, and funding by DARPA. Below this is a 'Set status' button and the repository name 'USC POSH Group' with the username 'USCPOSH' and an 'Edit profile' button. A bio states: 'A public repository for uploading and sharing AMS designs, including optimization tools and KGDs for the USC POSH effort.' The location is listed as 'Los Angeles'. The 'Overview' tab is selected, showing statistics: 7 Repositories, 0 Projects, 2 Stars, 4 Followers, and 0 Following. A 'Popular repositories' section lists four repositories: 'AMS_KGD' (3 stars, 1 fork), 'Sanitizer' (1 Python file, 1 star), 'Regression-tool' (instructions for students), and 'Local-optimizer' (Python file). A 'Collaborations' section shows 1 collaboration.

Traversing NDA-protected and NDA-free zones



Public open-source USC POSH repository, <https://github.com/USCPOSH>

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[Local optimization & retargeting](#)

[Sanitizer](#)

Other

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The screenshot shows the GitHub profile page for the USC POSH Group. The profile header includes the USC logo, the text 'in collaboration with MOSIS GLOBAL FOUNDRIES', and 'and funded in part by DARPA'. Below this is the repository name 'USC POSH Group' and the username 'USCPOSH'. A description states: 'A public repository for uploading and sharing AMS designs, including optimization tools and KGDs for the USC POSH effort.' The location is listed as 'Los Angeles'. The 'Popular repositories' section lists: 'AMS_KGD' (3 stars, 1 fork), 'Sanitizer' (1 star, Python), 'Regression-tool' (instructions for students), 'Collaborations' (1 star), 'AMS_IP' (LTspice-based circuit optimization tools), and 'Local-optimizer' (technology retargeting tool, Python). The 'Sanitizer' repository is circled in red in the diagram on the left.

Traversing NDA-protected and NDA-free zones with sanitization

Sanitization

Netlist with PDK information (GF65)

```
subckt INV65_v1 IN OUT VDD VSS
  M1 (OUT IN VDD VDD) p### l=lppp w=wppp*mp m=1 nf=mp\
  *****\
  *****\
  *****\
  *****\
  *****\
  *****\
  M0 (OUT IN VSS VSS) n### l=linnn w=winnn*mn m=1 nf=mn\
  *****\
  *****\
  *****\
  *****\
  *****\
  *****\
ends INV65_v1
// End of subcircuit definition.
```

Eliminating PDK information (NMOS / PMOS)



Sanitized Netlist

```
subckt INV65_v1 IN OUT VDD VSS
  M1 (OUT IN VDD VDD) p### l=lppp w=wppp*mp m=1 nf=mp
  M0 (OUT IN VSS VSS) n### l=linnn w=winnn*mn m=1 nf=mn
ends INV65_v1
```

Desanitization

Sanitized Netlist

```
subckt INV65_v1 IN OUT VDD VSS
  M1 (OUT IN VDD VDD) p### l=lppp w=wppp*mp m=1 nf=mp
  M0 (OUT IN VSS VSS) n### l=linnn w=winnn*mn m=1 nf=mn
ends INV65_v1
```

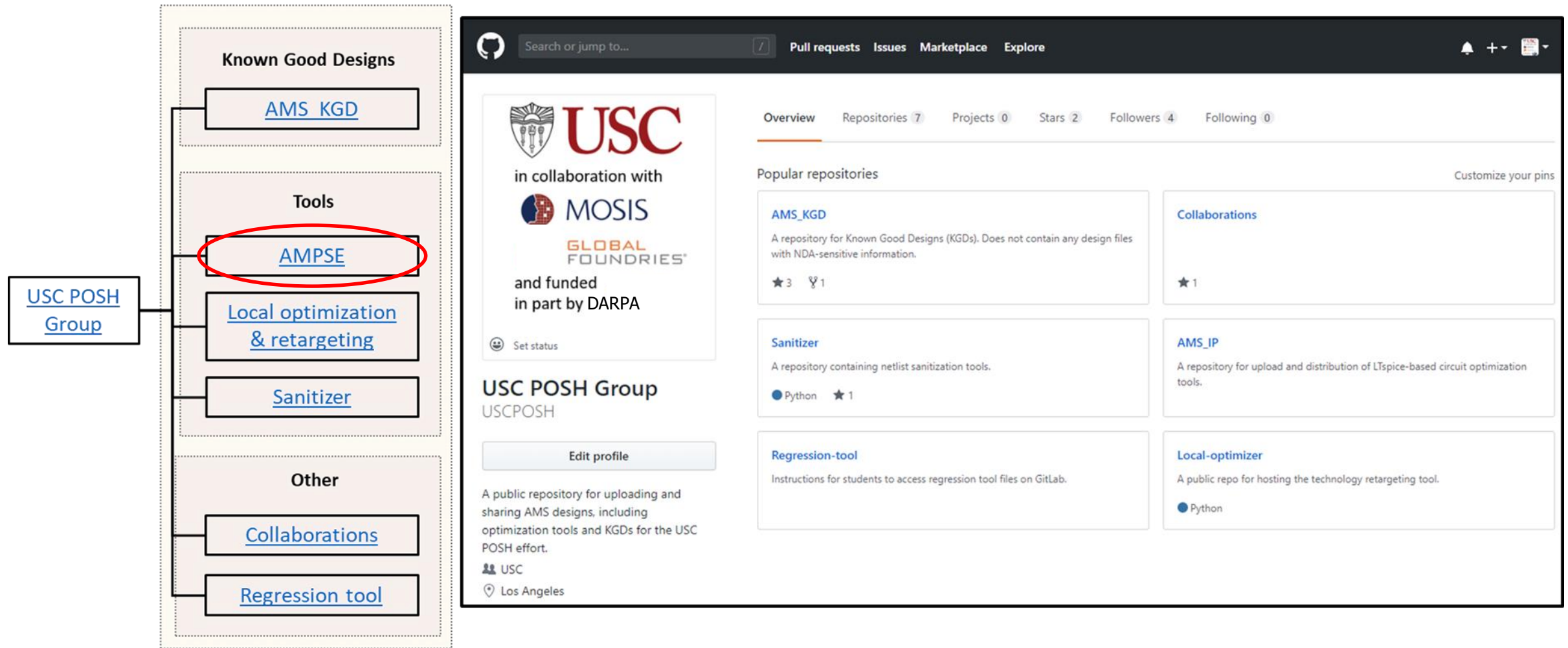
Adding PDK information necessary for accurate simulations



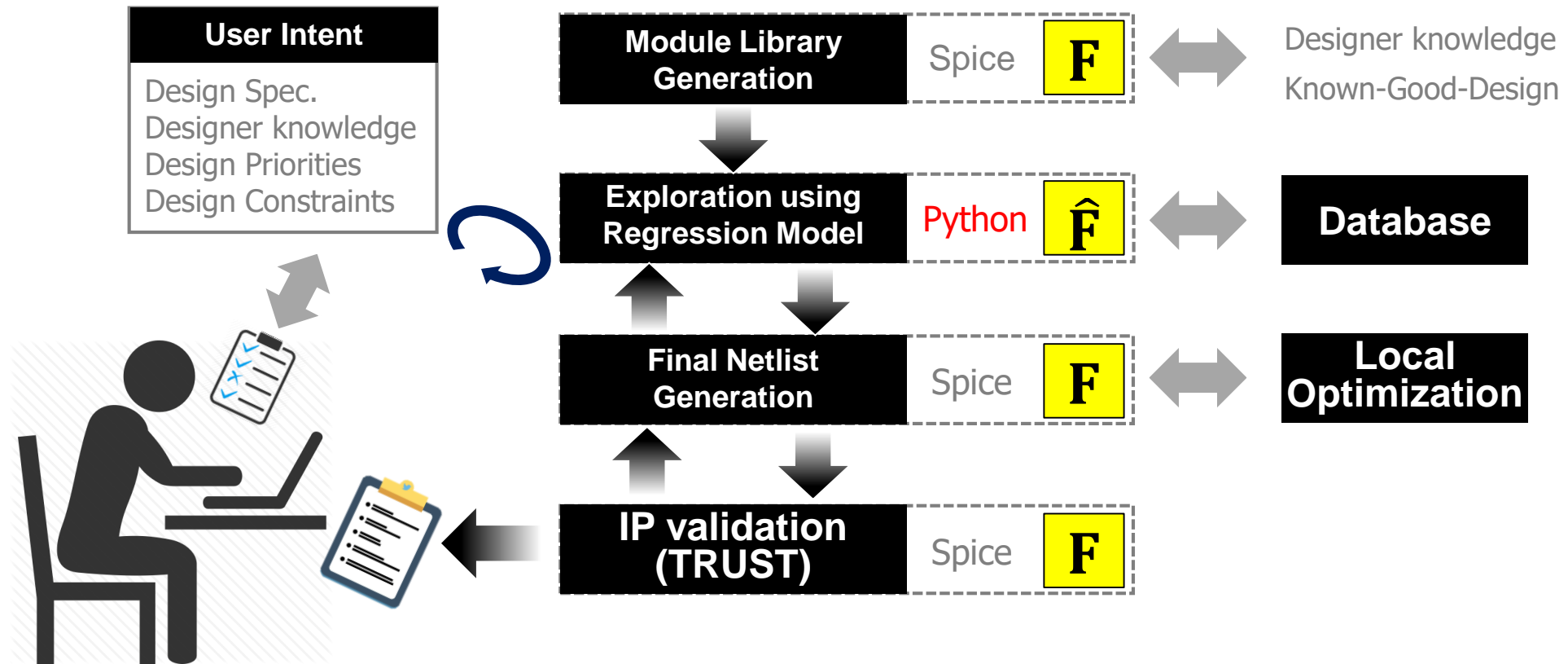
Netlist with PDK information

```
subckt INV65_v1 IN OUT VDD VSS
  M1 (OUT IN VDD VDD) p### l=lppp w=wppp*mp m=1 nf=mp\
  *****\
  *****\
  *****\
  *****\
  *****\
  *****\
  M0 (OUT IN VSS VSS) n### l=linnn w=winnn*mn m=1 nf=mn\
  *****\
  *****\
  *****\
  *****\
  *****\
  *****\
ends INV65_v1
// End of subcircuit definition.
```

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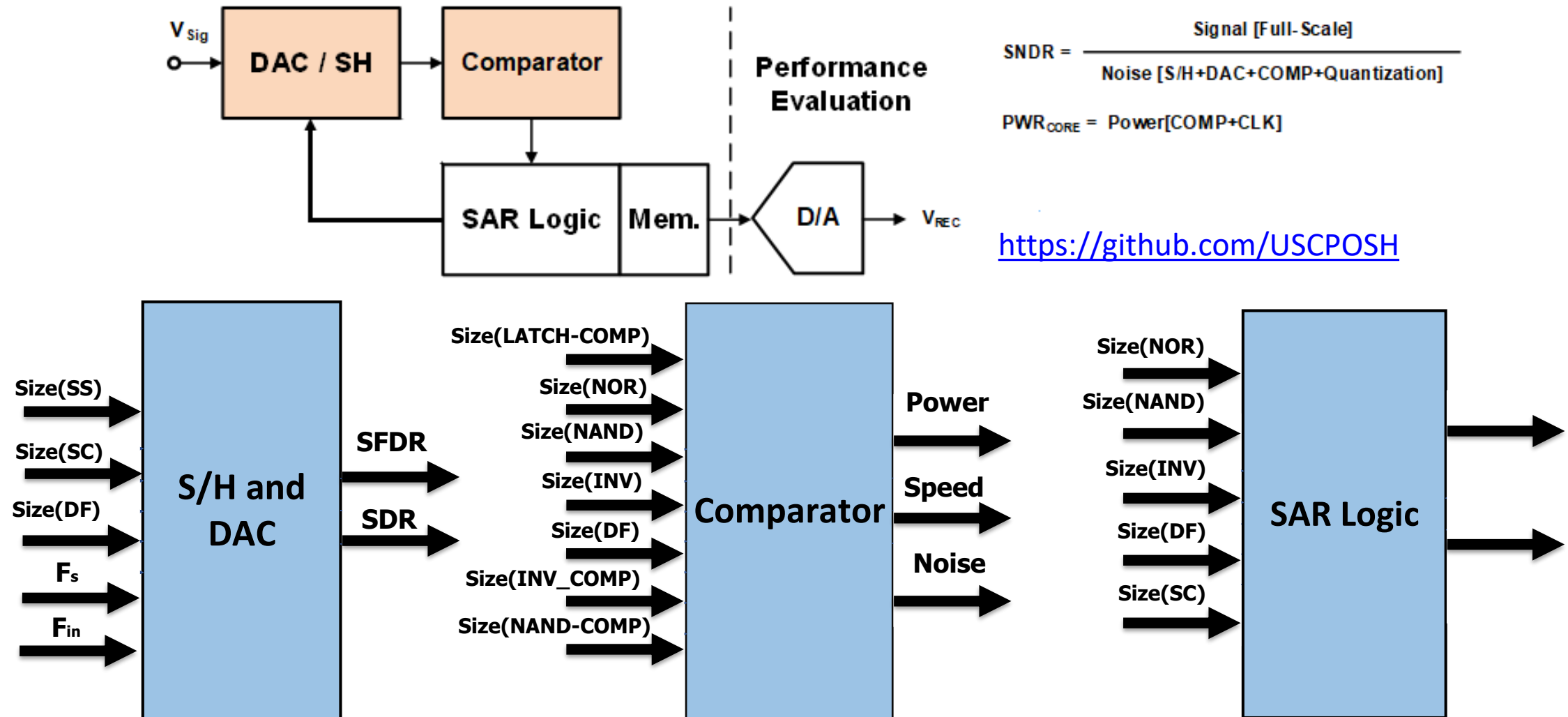


Analog Mixed-signal Parameter Search Engine (AMPSE) Design Flow



Expand AMS Design Space beyond single specification/technology for open-source (including Xyce) ecosystem

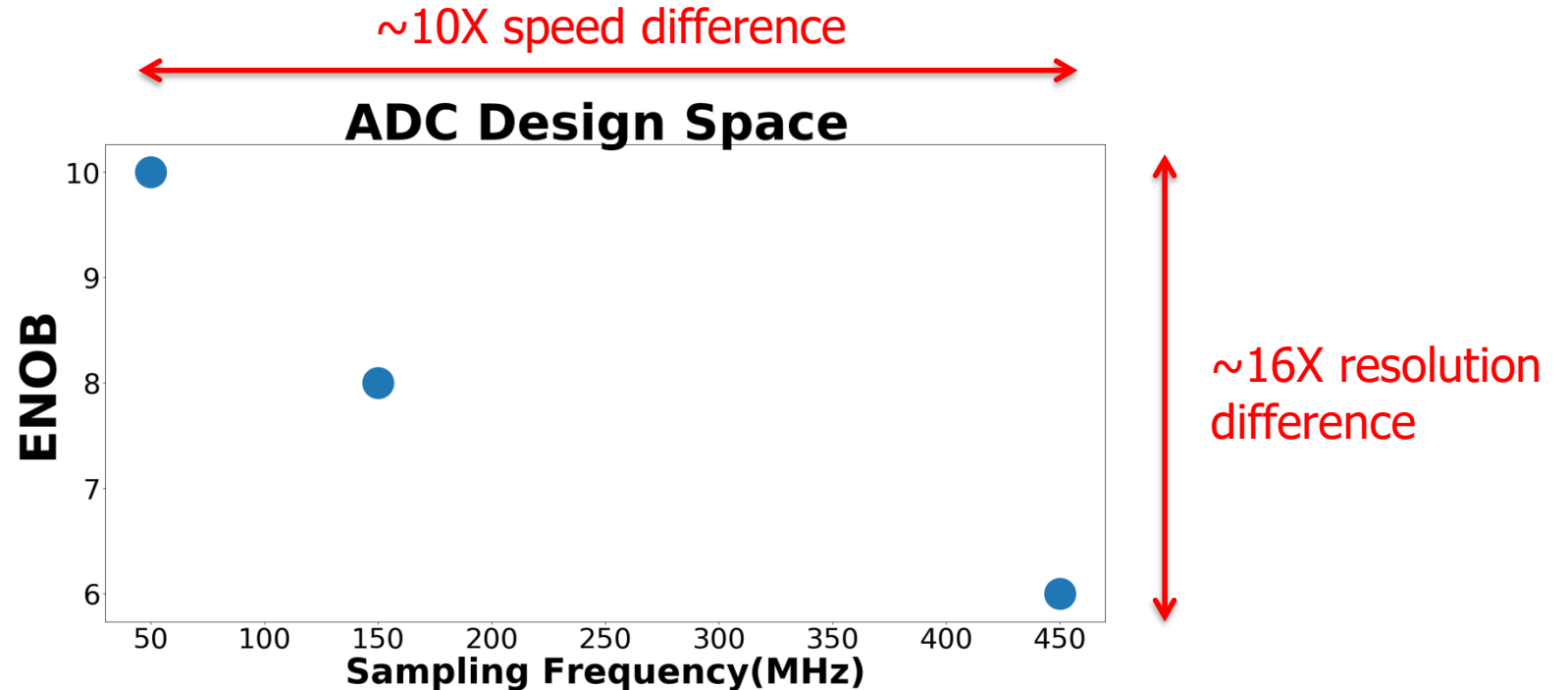
AMPSE design: SAR ADC



Access broad range of design objectives

Let's try these...

- 50MS/s 10-bit SAR ADC
- 150MS/s 8-bit SAR ADC
- 450MS/s 6-bit SAR ADC



$$(1) \sum T_{\text{COMP},k} + (N-1) \cdot \text{Max}\{ T_{\text{RS}}, T_{\text{DAC}} \} < 75\% T_{\text{period}}$$

$$(2) \text{SFDR} > \text{SFDR}_{\text{target}}$$

$$(3) \text{SNDR} > \text{SNDR}_{\text{target}}$$

$$(4) \dots$$

Formulate corresponding constraints
function for AMPSE

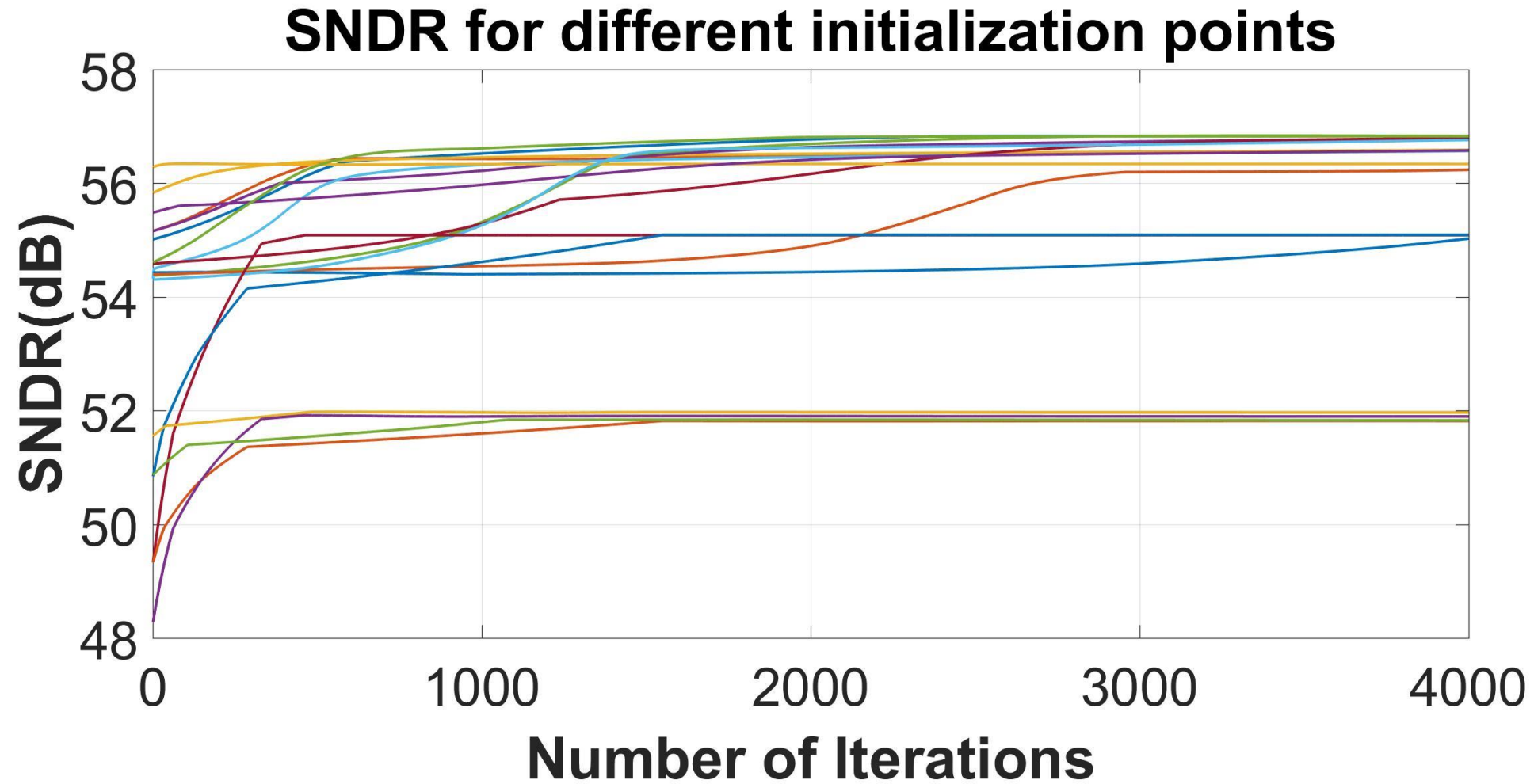
Use AMPSE for 10-bit ADC (schematic level)

The screenshot shows a Windows File Explorer window titled "SAR_ADC_nbit". The address bar shows the path "SAR_ADC_nbit". The left sidebar shows a navigation pane with a star icon and a list of folders. The main pane displays a list of 16 files with the following columns: Name, Date modified, Type, and Size.

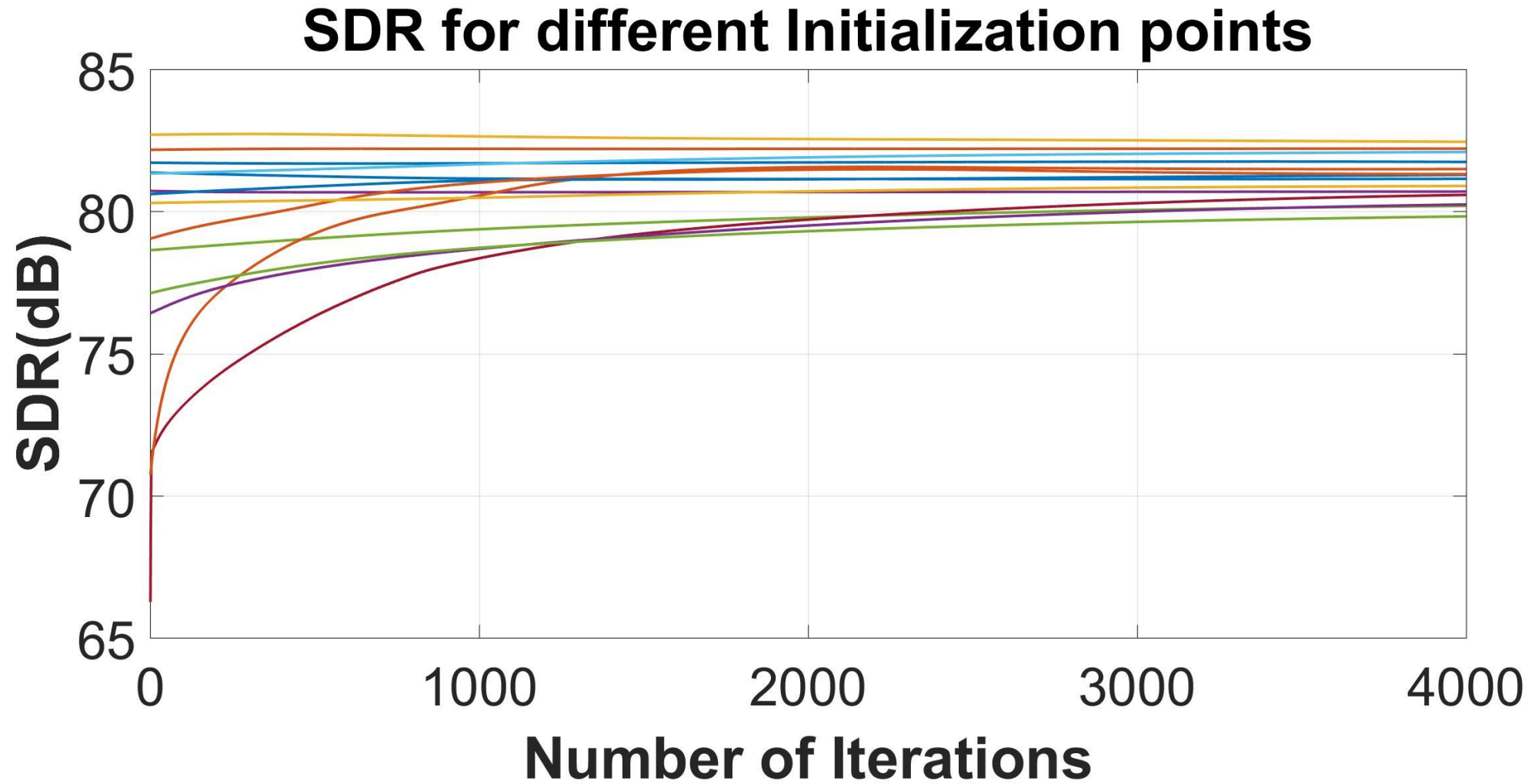
Name	Date modified	Type	Size
ggs_sar_nbit.py	7/15/2019 4:20 PM	PY File	12 KB
model_comparator45.json	7/2/2019 3:09 PM	JSON File	2 KB
model_SHBS45.json	6/28/2019 12:52 PM	JSON File	2 KB
reg_comparator45.h5	7/2/2019 3:09 PM	H5 File	181 KB
reg_SHBS45.h5	6/28/2019 12:52 PM	H5 File	32 KB
SAR.json	7/2/2019 5:22 PM	JSON File	2 KB
SAR_model.h5	7/2/2019 5:22 PM	H5 File	26 KB
scX_comparator45.pkl	7/2/2019 3:09 PM	PKL File	1 KB
scX_SAR.pkl	7/2/2019 5:22 PM	PKL File	1 KB
scX_SHBS45.pkl	6/28/2019 12:52 PM	PKL File	1 KB
scY_comparator45.pkl	7/2/2019 3:09 PM	PKL File	1 KB
scY_SAR.pkl	7/2/2019 5:22 PM	PKL File	1 KB
scY_SHBS45.pkl	6/28/2019 12:52 PM	PKL File	1 KB
w8_Comparator45.p	7/2/2019 3:09 PM	MATLAB P-code	166 KB
w8_SAR.p	7/2/2019 5:22 PM	MATLAB P-code	12 KB
w8_SHBS45.p	6/28/2019 12:52 PM	MATLAB P-code	17 KB

16 items

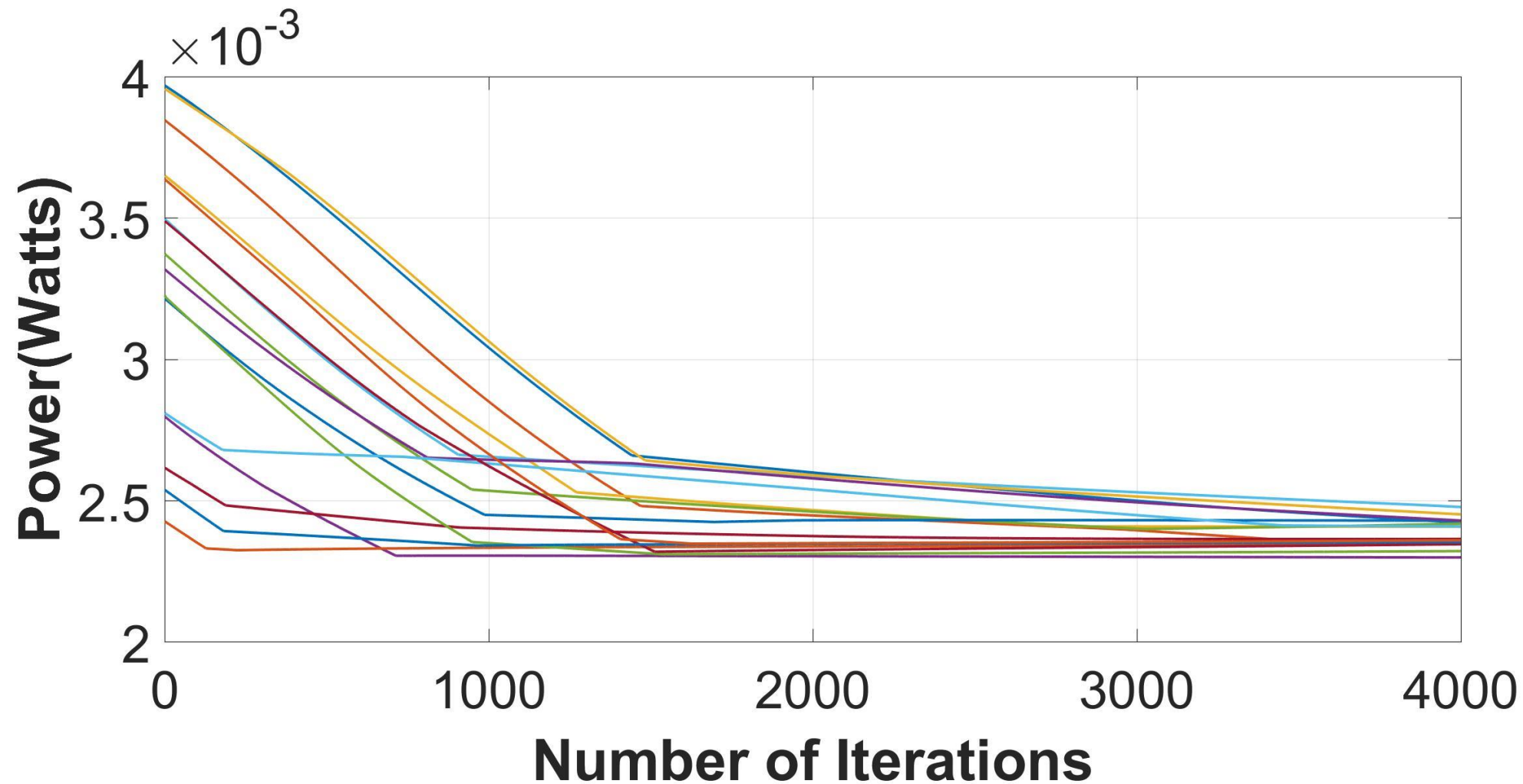
Parameter search process: 10-Bit SAR ADC design



Parameter search process: 10-Bit SAR ADC design



Parameter search process: 10-Bit SAR ADC design



SPICE validation of AMPSE design (schematic level)

- 50MS/s, 10-bit SAR ADC

Performance Metric	AMPSE design	SPICE Simulation
ENOB	9.14	8.5
SFDR	80.7dB(T/H Module)	60.15dB
Power Consumption	2.4mW	3.8mW

- 150MS/s, 8-bit SAR ADC

Performance Metric	AMPSE design	SPICE Simulation
ENOB	7.9	7.6
SFDR	70.76dB(T/H Module)	54.12dB
Power Consumption	4.43mW	6.7mW

- 450MS/s, 6-bit SAR ADC

Performance Metric	AMPSE design	SPICE Simulation
ENOB	5.9	5.3
SFDR	58.2dB(T/H Module)	41.2dB
Power Consumption	10.9mW	12.6mW

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