July 2019 Integration Week Demo

A SW/HW Sensory-Rich Monitoring System for SoC Designs

https://github.com/scale-lab/PVTSensors

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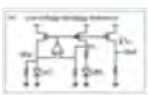
Students: Sofiane Chetoui (PhD student) and Xiaoyu (Steven) Lian (PhD student)

BROWN

Project overview

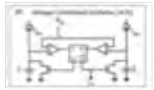
Task 1 HW components

1.1 thermal sensors



1.2 variability sensors

1.3 voltage margin sensors

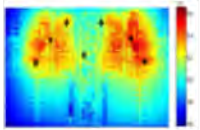


interfaces

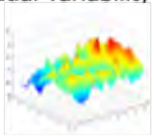
1.4 embedded RISCV-based µcontroller

Task 2 SW components

2.1 spatial thermal mapping



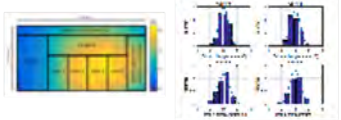
2.2 spatial variability extrapolation



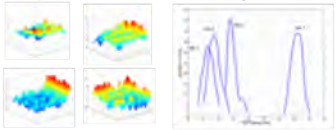
2.3 sensor fusion & inversion

Task 3 post-silicon calibration and validation

3.1 Thermal sensor calibration

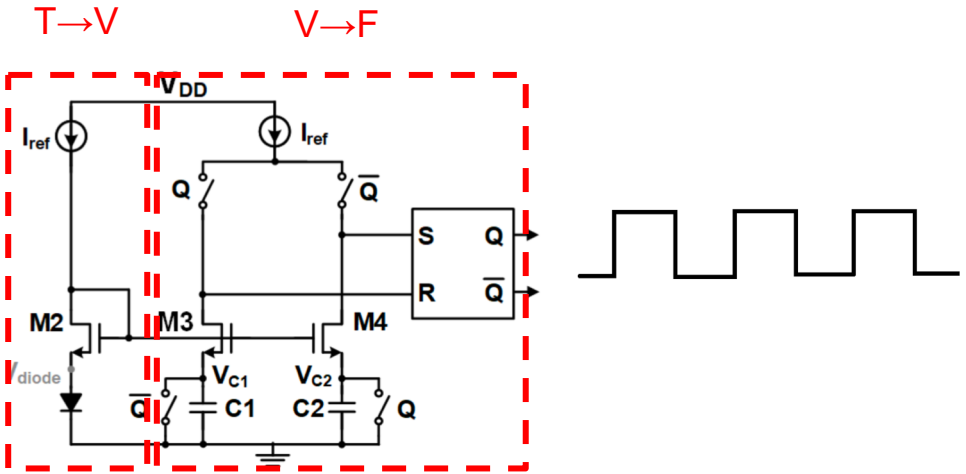


3.2 intra/inter-die variability calibration

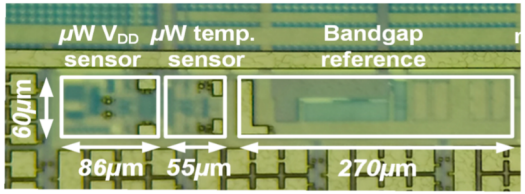


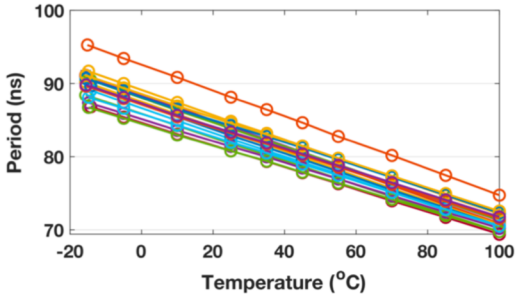
3.3 voltage margin calibration

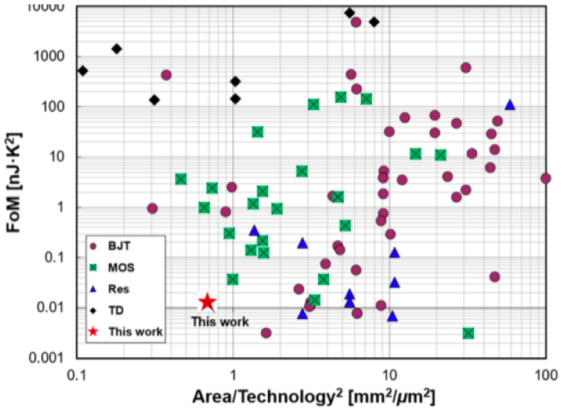
1.1 Thermal sensor design



180 nm tape out

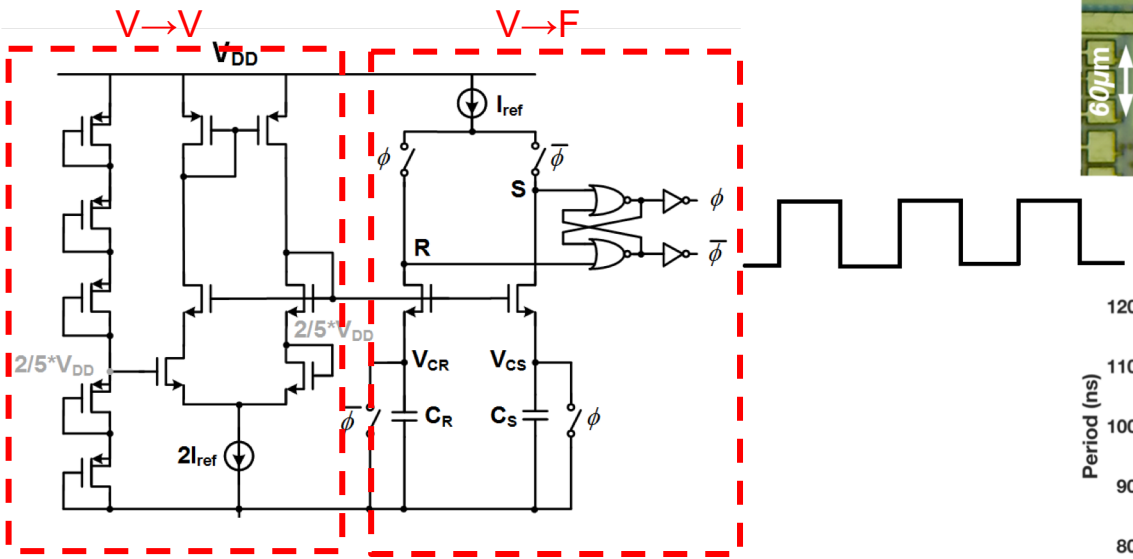




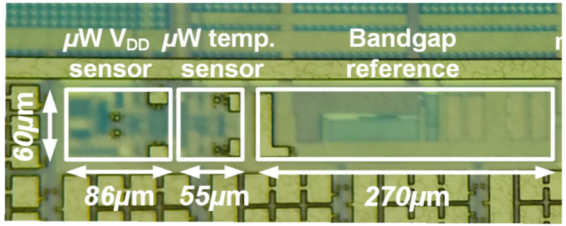


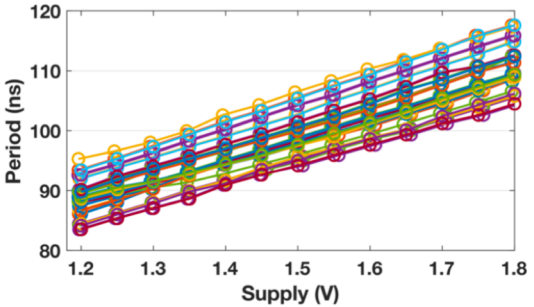
Proposed thermal sensor has an area of 0.022 mm^2, power 13.24 μW in 180-nm with 3$\boldsymbol{\sigma}$ inaccuracy of ±0.9 C. State-of-the-art Figure-of-Merit (FoM), highly area & power efficient sensor that reuses I_{ref} (article under revision).

1.2 Voltage sensor design



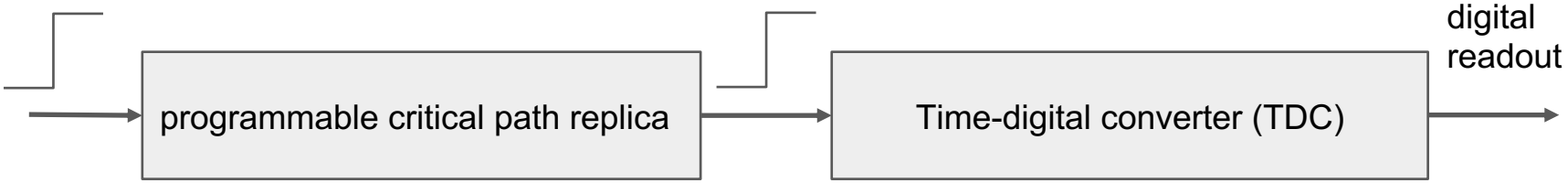
180 nm tape out

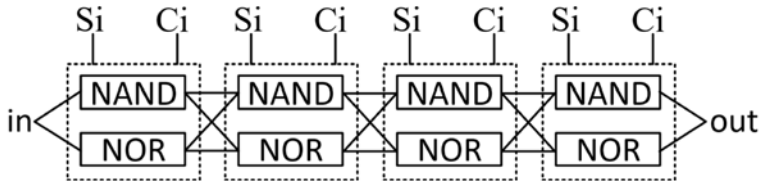




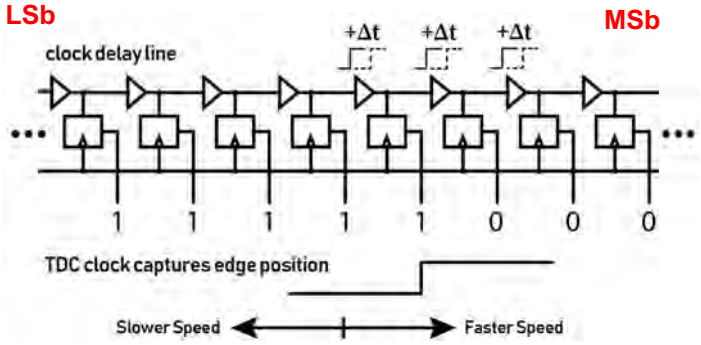
Proposed voltage sensor has a digital frequency output, an area of 0.024 mm^2, 15.54 μW, and conversion time of 22.4 μs. State-of-the-art highly area & power efficient sensor that reuses I_{ref} (article under revision).

1.3 P sensor (Critical path monitor)





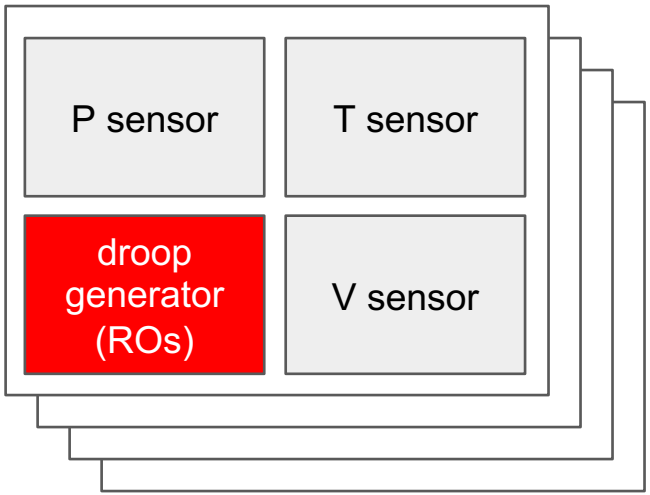
Ci, Si bits are programming bits that enable the critical path replica to have similar features to the actual critical path.



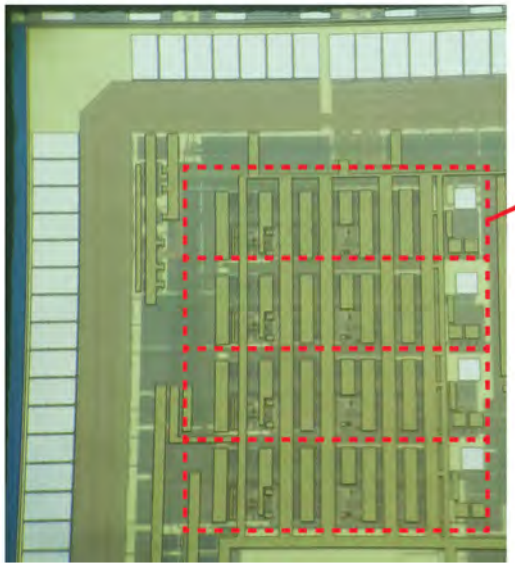
- Faster critical path → 1-0 transition pushed towards MSb
- Slower critical path → 1-0 transition pushed towards LSb

1.3 Second gen CPM test chip demo

each “core” contains:



180 nm tape out



Brown POSH PVT test chip #2
TSMC 180nm

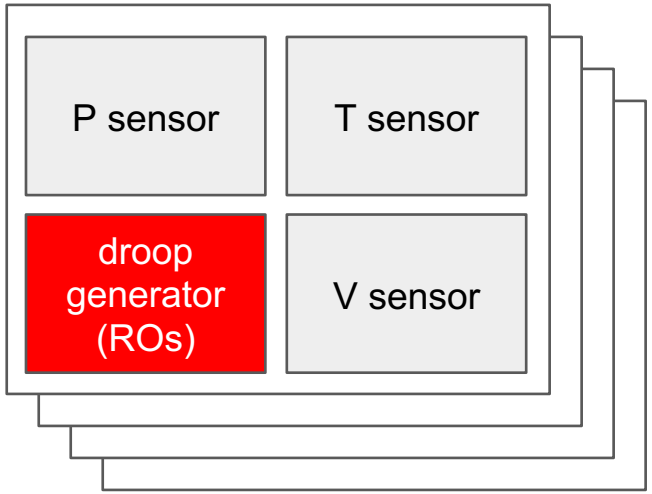
Channel 1/4:

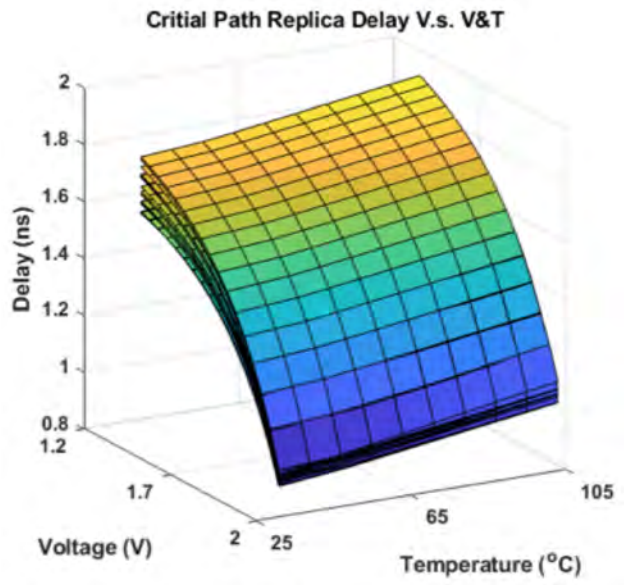
isolated VDD
supply droop generator
2 critical path (Process/timing) monitors
1 VDD sensor
1 Temperature sensor

Second gen chip has 4 “cores”

1.3 Multi-modal PVT demo

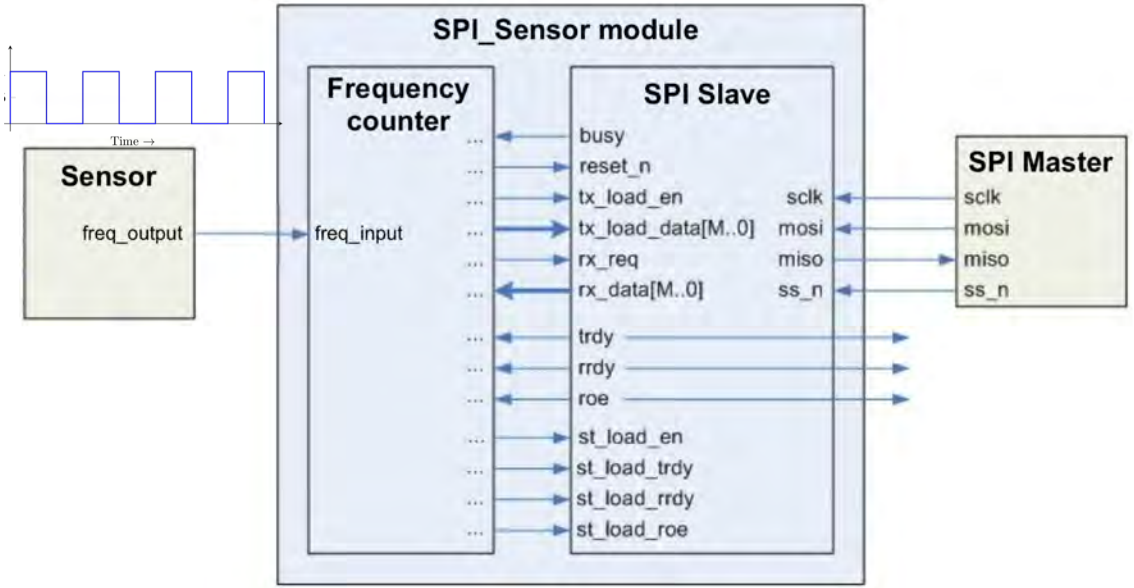
each “core” contains:





2.1 SPI interface

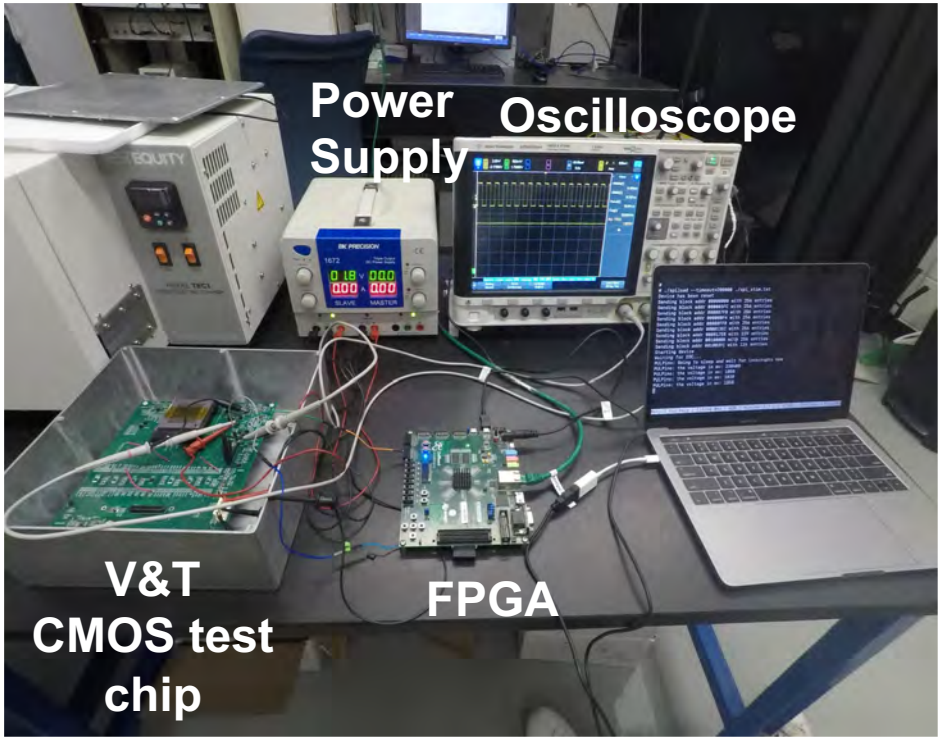
- Our sensors produce a periodic square wave (period proportional to T or V)
- Implemented a SPI sensor interface that connects our sensor outputs to any SPI master.

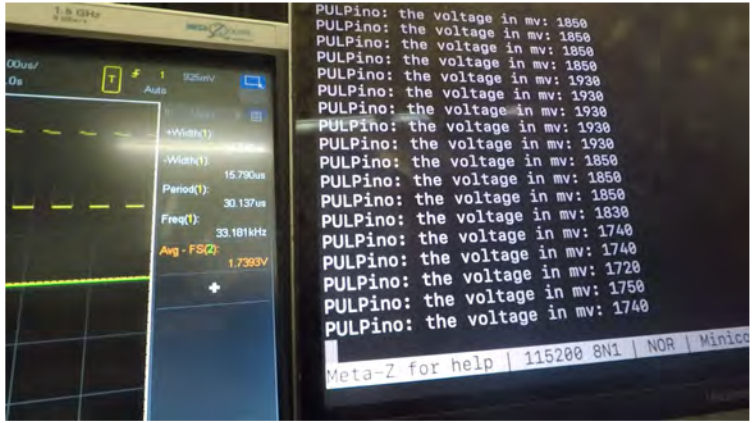


C -code

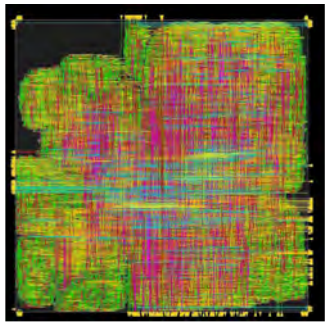
2.2 FPGA-based MCU

Using RISCV PULPINO controller on FPGA





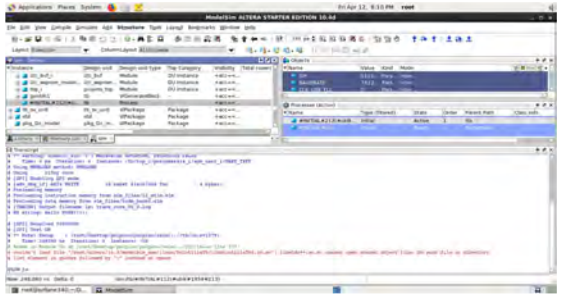
2.3 ASIC-based MCU



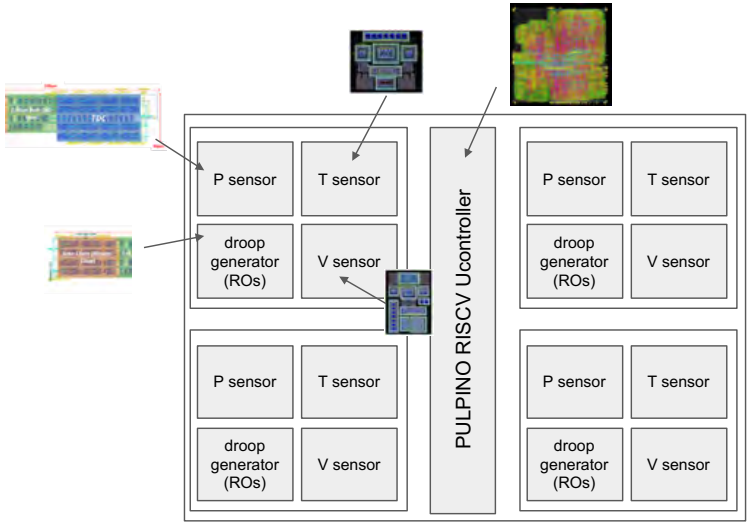
Frequency	Slack	Area (mm²)
No constraint	-	0.4508
10 MHz	88.21 (met)	0.4256
50 MHz	8.273 (met)	0.4255
100 MHz	0.146 (met)	0.4256

```
#include <stdio.h>

int main()
{
  printf("Hello POSH!!!!!\n");
  return 0;
}
```



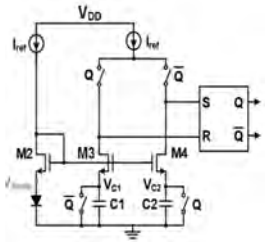
Third gen test chip (design underway):

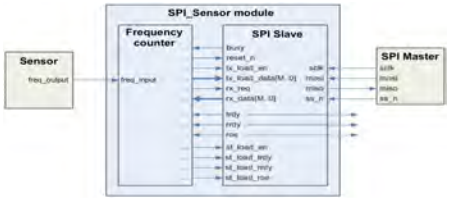


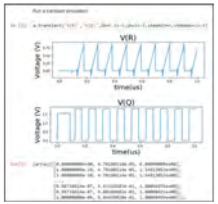
Summary of Github repo content

https://github.com/scale-lab/PVTSensors

- SPICE and Verilog-AMS netlists for all sensors.
- Xyce integration notebook.
- SPI digital interface Verilog and master C code.
- PULPINO MCU HW and SW chain port for FPGA implementation.







Thank you

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