July 2019 Integration Week Demo

A SW/HW Sensory-Rich Monitoring System for SoC Designs

https://github.com/scale-lab/PVTSensors

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Project overview



Task 3 post-silicon calibration and validation



3.3 voltage margin calibration



1.1 Thermal sensor design



Proposed thermal sensor has an area of 0.022 mm², power 13.24 μ W in 180-nm with 3 σ inaccuracy of ±0.9 C. State-of-the-art Figure-of-Merit (FoM), highly area & power efficient sensor that reuses I_{ref} (article under revision).

180 nm tape out





1.2 Voltage sensor design

180 nm tape out



Proposed voltage sensor has a digital frequency output, an area of 0.024 mm², 15.54 μ W, and conversion time of 22.4 μ s. State-of-the-art highly area & power efficient sensor that reuses I_{ref} (article under revision).

1.3 P sensor (Critical path monitor)



Ci, Si bits are programming bits that enable the critical path replica to have similar features to the actual critical path.

 Faster critical path → 1-0 transition pushed towards MSb

Faster Speed

TDC clock captures edge position

Slower Speed

 Slower critical path → 1-0 transition pushed towards LSb

1.3 Second gen CPM test chip demo





Second gen chip has 4 "cores"

1.3 Multi-modal PVT demo

P sensor T sensor droop generator (ROs) V sensor

each "core" contains:



2.1 SPI interface

- Our sensors produce a periodic square wave (period proportional to T or V)
- Implemented a SPI sensor interface that connects our sensor outputs to any SPI master.



2.2 FPGA-based MCU

Using RISCV PULPINO controller on FPGA





2.3 ASIC-based MCU



Frequency	Slack	Area (mm²)
No constraint	-	0.4508
10 MHz	88.21 (met)	0.4256
50 MHz	8.273 (met)	0.4255
100 MHz	0.146 (met)	0.4256

#include <stdio.h>

int main()
{
 printf("Hello POSH!!!!!\n");
 return 0;
}

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Third gen test chip (design underway):



Summary of Github repo content

https://github.com/scale-lab/PVTSensors

- SPICE and Verilog-AMS netlists for all sensors.
- Xyce integration notebook.
- SPI digital interface Verilog and master C code.
- PULPINO MCU HW and SW chain port for FPGA implementation.





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- b- cd ri5cy_gnu_toolchain
- c- run make, It will download some files, encounter in error and sto d- of build/src/medib-oc/acc/co

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e- Open cfms.gperf in your favorite text editor and remove lines below the first comment istarting at) f- operf -o -C -E -k '1-6.5' -(1 -0 -k lib) name o -L C++ --output-file cfms.h cfms.meef

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2- Source the binary files:





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