

# **ERI Design: IDEA and POSH Ethernet Controller Open Source IP Cores**

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CHINH LE  
LeWiz Communications, Inc.

IDEA and POSH Phase I Integration Exercise  
Detroit, MI

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## Open Session Slides

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# Program Overview (Open Session)

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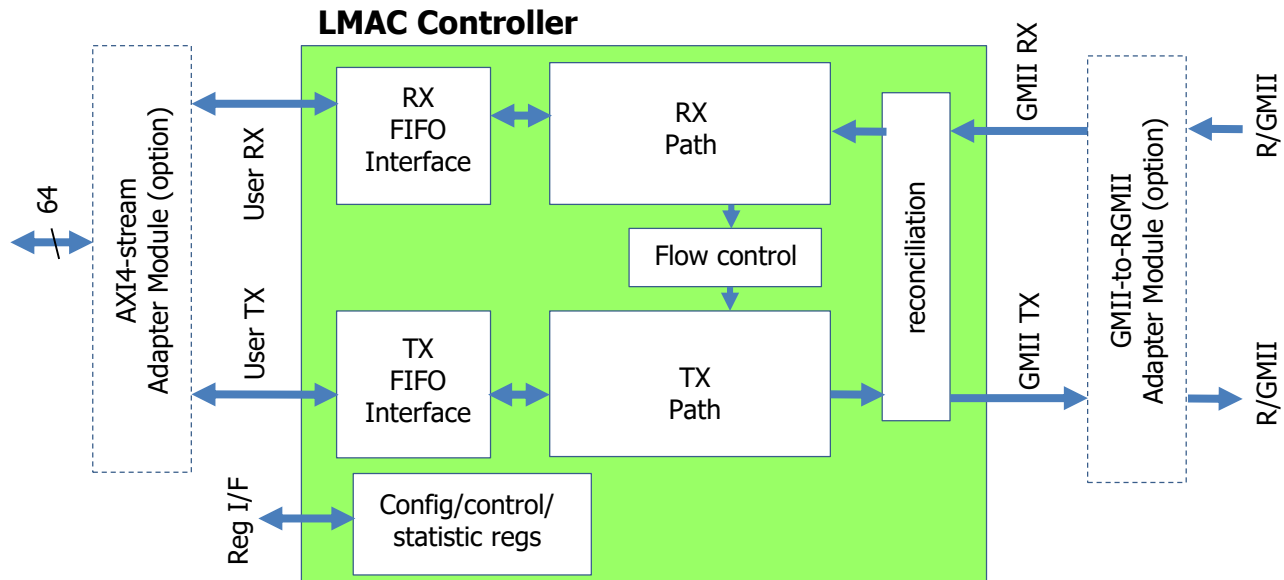
Development of 3 Open Source Ethernet controller (MAC) IP cores:

- Core 1: 10/100/1000Mbps
- Core 2: 10G/5G/2.5G/1Gbps
- Core 3: 100G/50G/40G/25G/10Gbps
- Designed for easy migration to SoC from FPGA emulation
- Unified architecture: Simpler interface, software driver, easy to migrate to different speed, different PHYs, suitable for small IoT to large applications
- Open source: but complete code, simulation bench, FPGA project, drivers, documentation, and support



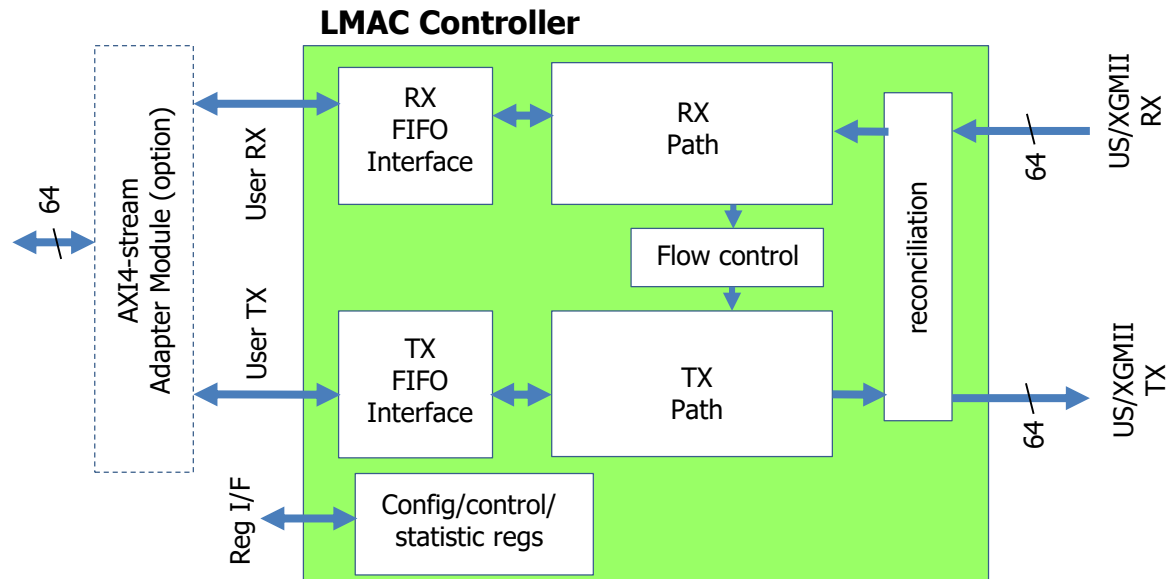
# Technical Approach (Open Session)

CORE 1: 10/100/1000Mbps



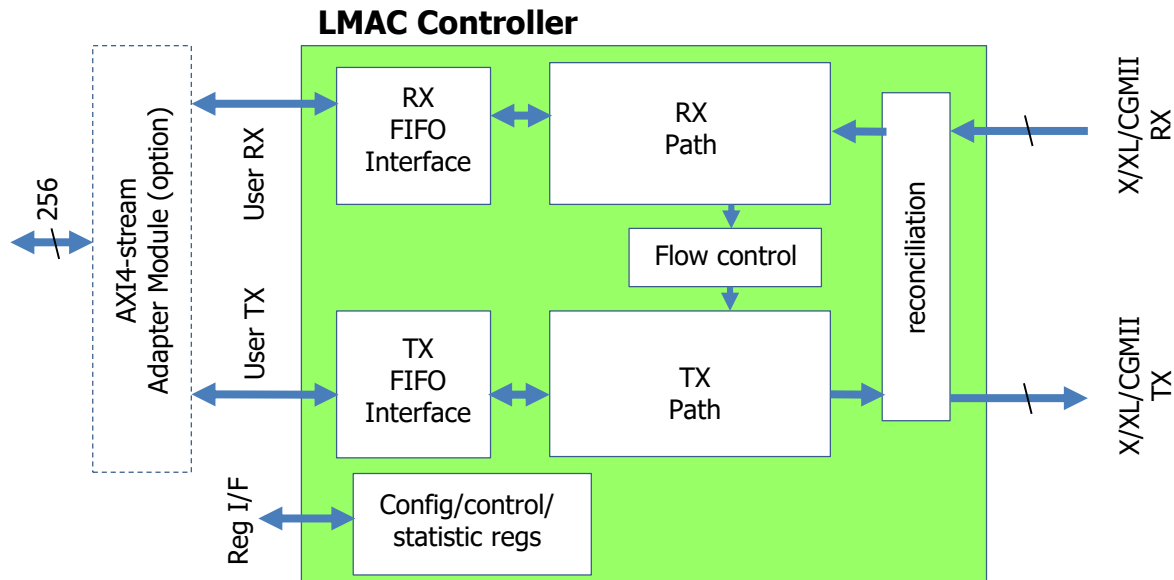
# Technical Approach (Open Session)

CORE 2: 10G/5G/2.5G/1Gbps



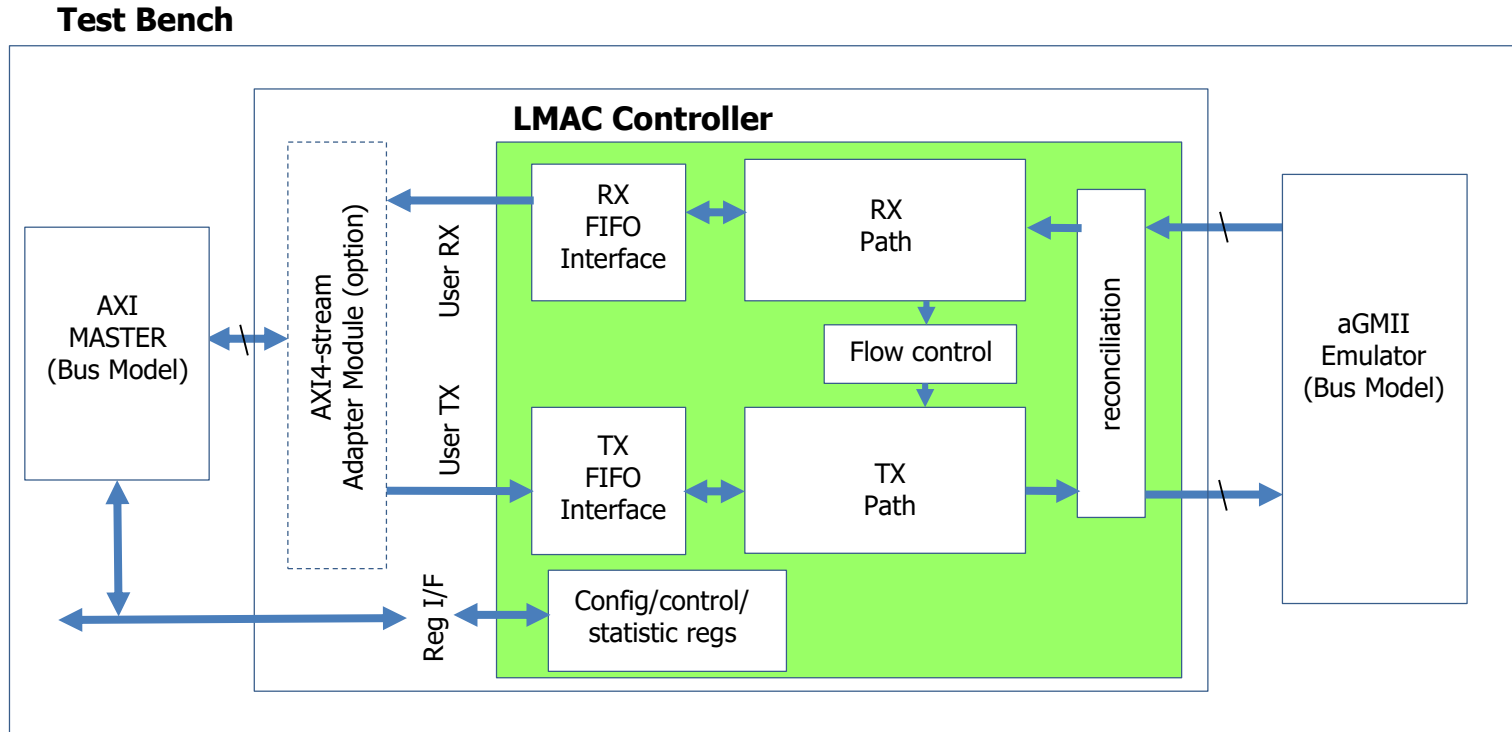
# Technical Approach (Open Session)

CORE 3: 100G/50G/40G/25G/10Gbps



# Technical Approach (Open Session)

Verification: Test bench (complex and most time consuming)



## NOTES:

- Bus models allows packet level testing
- Transmit and receive flows
- No vendor specific or technology dependent

# Technical Approach (Open Session)

## Status

- APPROVED FOR RELEASE TO GITHUB
  - Released Core 1 and 2
  - Documentation (specs and usage), Instructions
  - Tests and results used in verification of IP cores in simulation, test benches
  - Github.com → search for LMAC CORE
  - You should see LMAC\_CORE1 and LMAC\_CORE2
- LICENSING - open source hardware ecosystem
  - Access model – open source (Github)
  - License using Lesser GPL 2.1



# Future Plans (Open Session)

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- Near term plan:
  - 3 months – Core 3 architecture review and initial code release
  - 6 months – Final Core 3 release with docs, simulation bench

# Screenshot of Sim Script



```
1 ##
2 ## Copyright (C) 2018 LeWiz Communications, Inc.
3 ##
4 ## This library is free software; you can redistribute it and/or
5 ## modify it under the terms of the GNU Lesser General Public
6 ## License as published by the Free Software Foundation; either
7 ## version 2.1 of the License, or (at your option) any later version.
8 ##
9 ## This library is distributed in the hope that it will be useful,
10 ## but WITHOUT ANY WARRANTY; without even the implied warranty of
11 ## MERCHANTABILITY or FITNESS FOR A PARTICULAR PURPOSE. See the GNU
12 ## Lesser General Public License for more details.
13 ##
14 ## You should have received a copy of the GNU Lesser General Public
15 ## License along with this library release; if not, write to the Free Software
16 ## Foundation, Inc., 51 Franklin Street, Fifth Floor, Boston, MA 02110-1301 USA
17 ##
18 ## LeWiz can be contacted at: support@lewiz.com
19 ## or address:
20 ## PO Box 9276
21 ## San Jose, CA 95157-9276
22 ## www.lewiz.com
23 ##
24 ## Author: LeWiz Communications, Inc.
25 ## Language: Verilog
26 ##
27
28 # source SCRIPTS/8_PKT/Script4_RxPath_Test_10G.txt
29 # Script to test LMAC: test rx path, 64-bit mode (XGMII).
30 # fmac_speed: 000 = 10 Gig mode
31 #             101 = 5 Gig mode
32 #             010 = 2.5 Gig mode
33 #             001 = 1 Gig mode
34 # rx_pkt_gen_sel selects the source of the data on RxD and RxC. If 1 = data is from the rx_pkt_gen. If 0 = loopback data (TxD and TxC is sent to RxD and RxC).
35
36
37 vsim work.axis_lmac_tb
38
39 view wave
40 do E:/LMAC2_INFO/waveforms/rx_path_test
41
42 view -new wave
43 add wave -r /*
44
45 mem load -i E:/LMAC2_INFO/AXIS_MASTER/memory_wr_data.txt -format hex /AXIS_LMAC_TB/axi_stream_master/memory_wr_module/memory_wr_data
46 mem load -i E:/LMAC2_INFO/AXIS_MASTER/memory_wr_ctrl.txt -format hex /AXIS_LMAC_TB/axi_stream_master/memory_wr_module/memory_wr_ctrl
47
48 mem load -i E:/LMAC2_INFO/SCRIPTS/8_PKT/rx_pkt_gen_data.mem -format hex /AXIS_LMAC_TB/phy_emulator_10G/rx_pkt_gen_10G/rx_pkt_gen2kx64_inst/dram_data/mem
49 mem load -i E:/LMAC2_INFO/SCRIPTS/8_PKT/rx_pkt_gen_ctrl.mem -format hex /AXIS_LMAC_TB/phy_emulator_10G/rx_pkt_gen_10G/rx_pkt_gen2kx8_inst/dram_ctrl/mem
50
51 force -freeze sim:/AXIS_LMAC_TB/fmac_speed 3'd0 0
52
53 force -freeze sim:/AXIS_LMAC_TB/phy_emulator_10G/rx_pkt_gen_start_addr 64'd00 0
54 force -freeze sim:/AXIS_LMAC_TB/phy_emulator_10G/rx_pkt_gen_read_cnt 11'd0 0
55
56
57 # Select the rx_pkt_gen memory data
58 run 200ns
```

# Screenshot of Modelsim – exec & results



| Instance                  | Design unit             | Design unit type |
|---------------------------|-------------------------|------------------|
| AXIS_LMAC_TB              | AXIS_LMAC_TB            | Module           |
| axi_stream_master         | axi_stream_master       | Module           |
| memory_wr_module          | memory_wr_module        | Module           |
| memory_rd_8b_module       | memory_rd_8b_module     | Module           |
| memory_compare_8b         | memory_compare_8b       | Module           |
| register_interface1       | register_interface      | Module           |
| AXIS_LMAC_TOP             | AXIS_LMAC_TOP           | Module           |
| AXIS_BRIDGE_TOP           | AXIS_BRIDGE_TOP         | Module           |
| axis2fib_txctrl           | axis2fib_txctrl         | Module           |
| txdata_fifo256x64         | txdata_fifo256x64       | Module           |
| txwbctrl_fifo4x32         | txwbctrl_fifo4x32       | Module           |
| fib2fmac_txctrl           | fib2fmac_txctrl         | Module           |
| fmac2fib_rxctrl           | fmac2fib_rxctrl         | Module           |
| rxdata_fifo256x64         | rxdata_fifo256x64       | Module           |
| rxrbctrl_fifo4x32         | rxrbctrl_fifo4x32       | Module           |
| axis2fib_rxctrl           | axis2fib_rxctrl         | Module           |
| nif_if_bridge1            | nif_if_bridge           | Module           |
| rxregif_fifo4x8_done      | rxregif_fifo4x8         | Module           |
| txwregif_fifo4x8_start    | txwregif_fifo4x8        | Module           |
| rxregif_fifo4x32_data     | rxregif_fifo4x32        | Module           |
| txwregif_fifo4x16_address | txwregif_fifo4x16       | Module           |
| LMAC_CORE_TOP             | LMAC_CORE_TOP           | Module           |
| core                      | tc_core_fmcore          | Module           |
| txfifo                    | txfifo_1024x64          | Module           |
| tx_1G_wrap                | tx_1G_wrap              | Module           |
| tx_10G_wrap               | tx_10G_wrap             | Module           |
| rxfifo                    | fmcore_fifo4Kx64        | Module           |
| pkctrl_fifo               | fmcore_fifo4Kx8         | Module           |
| ipcs_fifo                 | fmcore_fifo512x64_2clk  | Module           |
| rx_xgmii                  | tc_core_rx_xgmii        | Module           |
| rx_decap                  | rx_decap                | Module           |
| byte_reordering           | tc_core_byte_reordering | Module           |
| rf_sfifo                  | br_sfifo4x32            | Module           |
| bfsol_sfifo               | br_sfifo4x32            | Module           |
| rx_5g                     | rx_5g                   | Module           |
| gige_s2p                  | gige_s2p                | Module           |
| ctrl_2g_5g                | ctrl_2g_5g              | Module           |
| gigerx_fifo256x64_2clk    | gigerx_fifo256x64_2clk  | Module           |
| gigerx_fifo256x8          | gigerx_fifo256x8        | Module           |
| gigerx_bctrl_fifo256x16   | gigerx_bctrl_fifo256x16 | Module           |
| g2x_ctrl                  | g2x_ctrl                | Module           |
| fmcore_register_if        | fmcore_register_if      | Module           |
| phy_emulator_10G          | phy_emulator_10G        | Module           |
| rx_pkt_gen_10G            | rx_pkt_gen_10G          | Module           |

```

# Loading work.txdata_fifo256x64
# Loading work.async_fifo
# Loading work.txwbctrl_fifo4x32
# Loading work.fib2fmac_txctrl
# Loading work.fmac2fib_rxctrl
# Loading work.rxdata_fifo256x64
# Loading work.rxrbctrl_fifo4x32
# Loading work.axis2fib_rxctrl
# Loading work.nif_if_bridge
# Loading work.rxregif_fifo4x8
# Loading work.txwregif_fifo4x8
# Loading work.rxregif_fifo4x32
# Loading work.txwregif_fifo4x16
# Loading work.LMAC_CORE_TOP
# Loading work.tc_core_fmcore
# Loading work.bxfifo_1024x64
# Loading work.tx_1G_wrap
# Loading work.tx_10G_wrap
# Loading work.gige_tx_encap
# Loading work.gige_tx_gmii
# Loading work.gige_crc32x64
# Loading work.tx_10G_wrap
# Loading work.tx_encap
# Loading work.tx_xgmii
# Loading work.tx_mac10g_crc32x64
# Loading work.fmac_fifo4Kx64
# Loading work.fmac_fifo4Kx8
# Loading work.fmac_fifo512x64_2clk
# Loading work.tc_core_rx_xgmii
# Loading work.fmac_saddr_filter
# Loading work.eth_crc32_gen
# Loading work.bsh32_dn_88
# Loading work.bsh8_dn_64
# Loading work.crc32_d64
# Loading work.crc32_d8s
# Loading work.crc32_d16s
# Loading work.crc32_d24s
# Loading work.rx_decap
# Loading work.tc_core_byte_reordering
# Loading work.br_sfifo4x32
# Loading work.rx_5g
# Loading work.gige_s2p
# Loading work.ctrl_2g_5g
# Loading work.gigerx_fifo256x64_2clk
# Loading work.gigerx_fifo256x8
# Loading work.gigerx_bctrl_fifo256x16
# Loading work.g2x_ctrl
# Loading work.fmac_register_if
# Loading work.phy_emulator_10G
# Loading work.rx_pkt_gen_10G
# Loading work.gigerx_fifo256x64_2clk
# Loading work.gigerx_fifo256x8
# Loading work.gigerx_bctrl_fifo256x16
# Loading work.g2x_ctrl
# Loading work.fmac_register_if
# Loading work.phy_emulator_10G
# Loading work.rx_pkt_gen_10G

**PASSED: Packet No.: 1 is received as expected.
**PASSED: Packet No.: 2 is received as expected.
**PASSED: Packet No.: 3 is received as expected.
**PASSED: Packet No.: 4 is received as expected.
**PASSED: Packet No.: 5 is received as expected.
**PASSED: Packet No.: 6 is received as expected.
**PASSED: Packet No.: 7 is received as expected.
**PASSED: Packet No.: 8 is received as expected.

VSIM 157> source SCRIPTS/8_PKT/Script4_RxPath_Test_10G.txt
    
```

Project: Library sim Files

Object: LMAC2 INFO Now: 13.204 ns Delta: 3 sim:/AXIS\_LMAC\_TB

