



# Modular System Design in 2.5D

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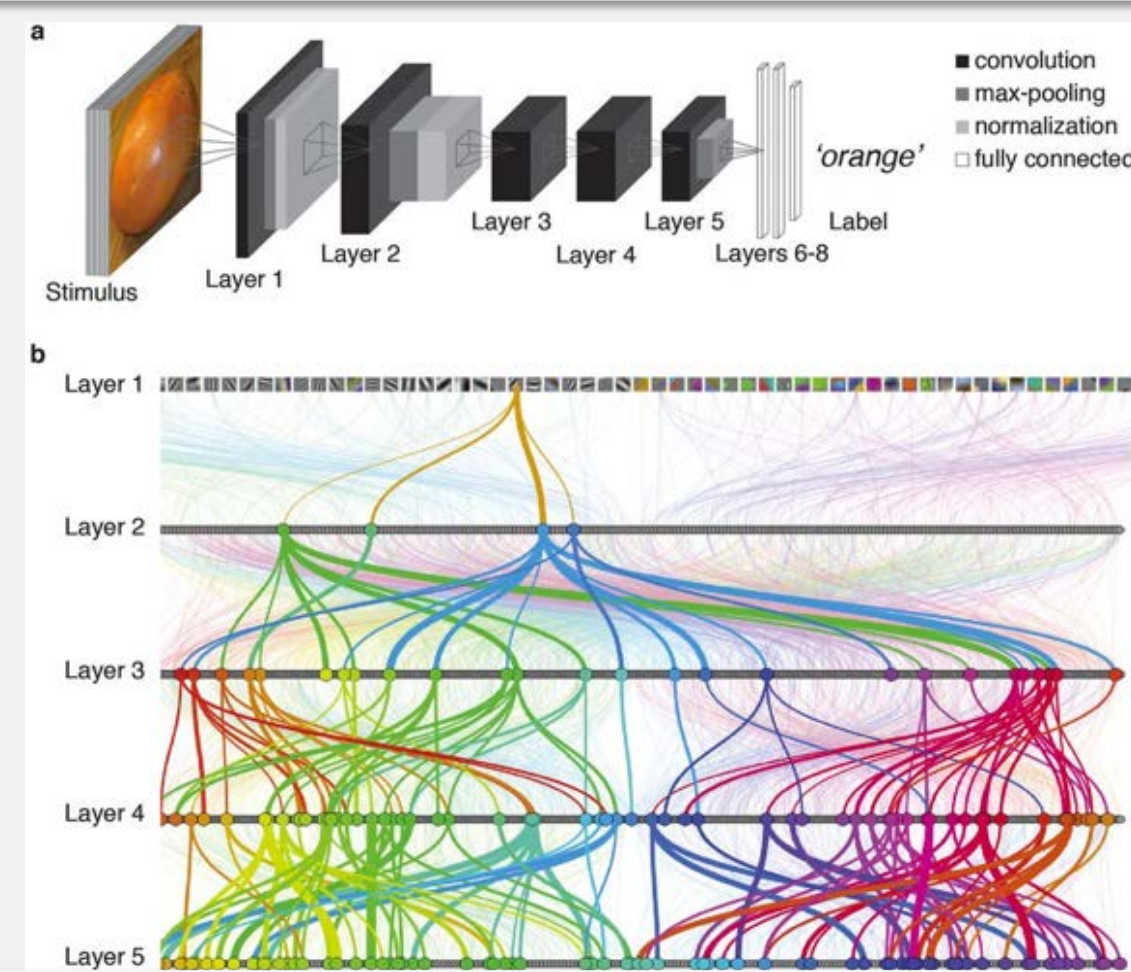


## 3D Heterogeneous Integration: Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)



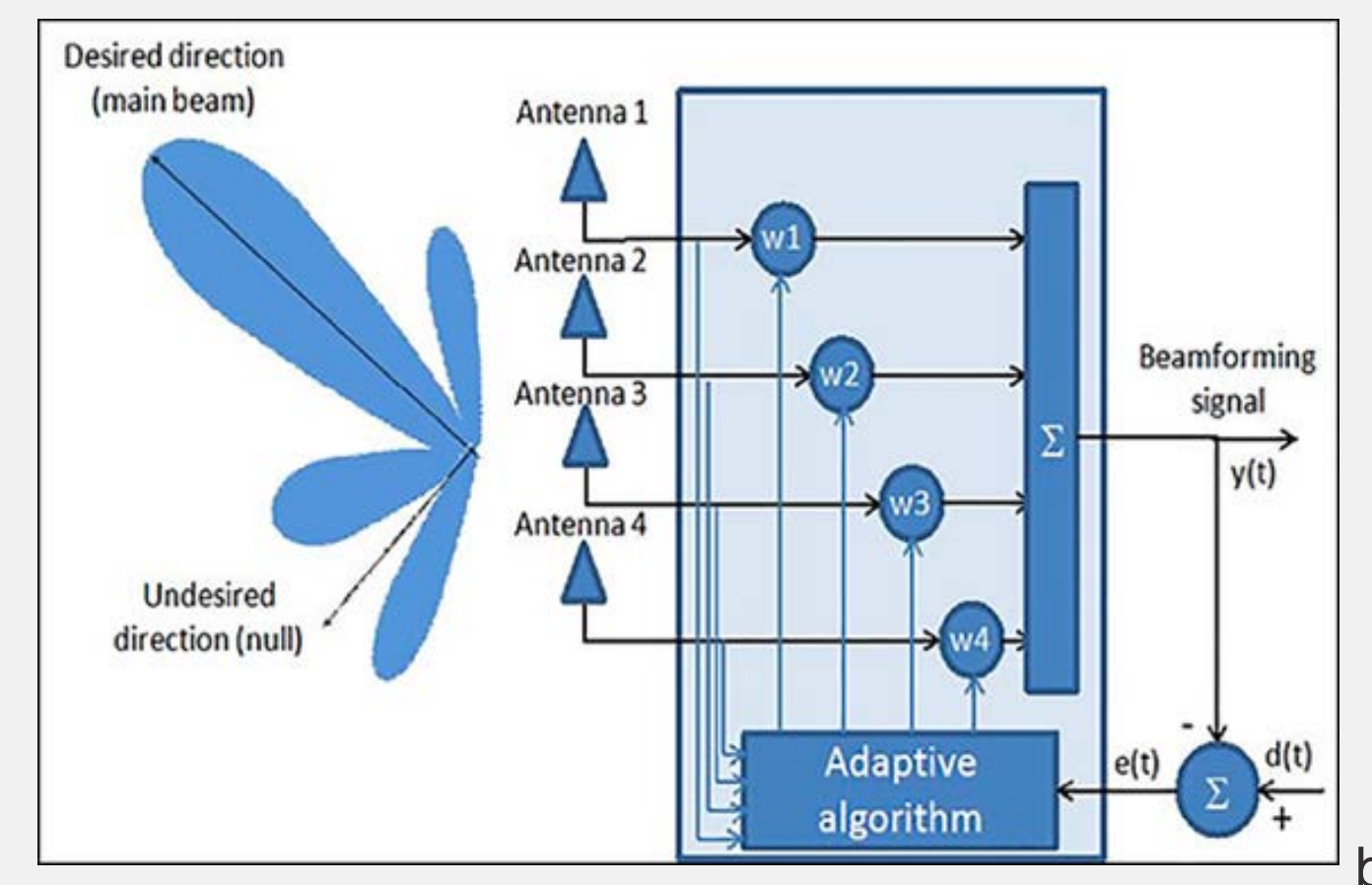
### Machine Learning Systems

- Large-scale compute
- Large memory capacity
- High access bandwidth

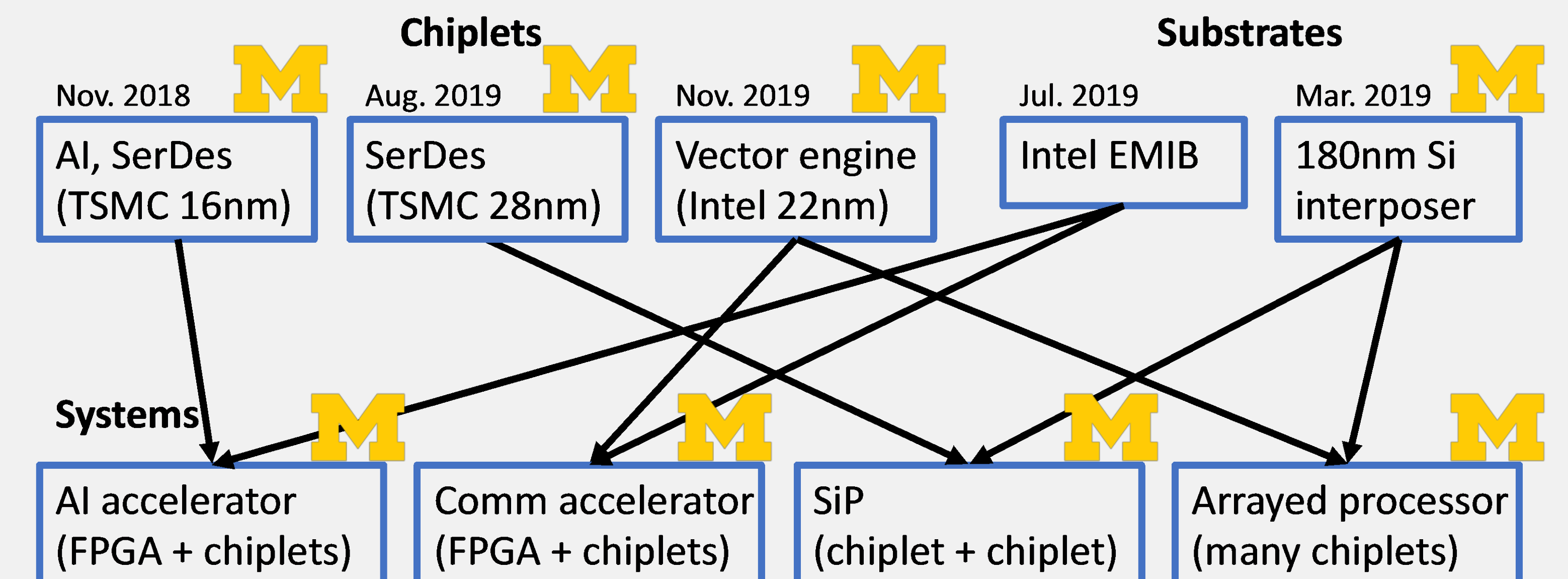


### Smart Antenna Systems

- Mixed-signal
- Heterogeneous integration
- High-bandwidth streaming



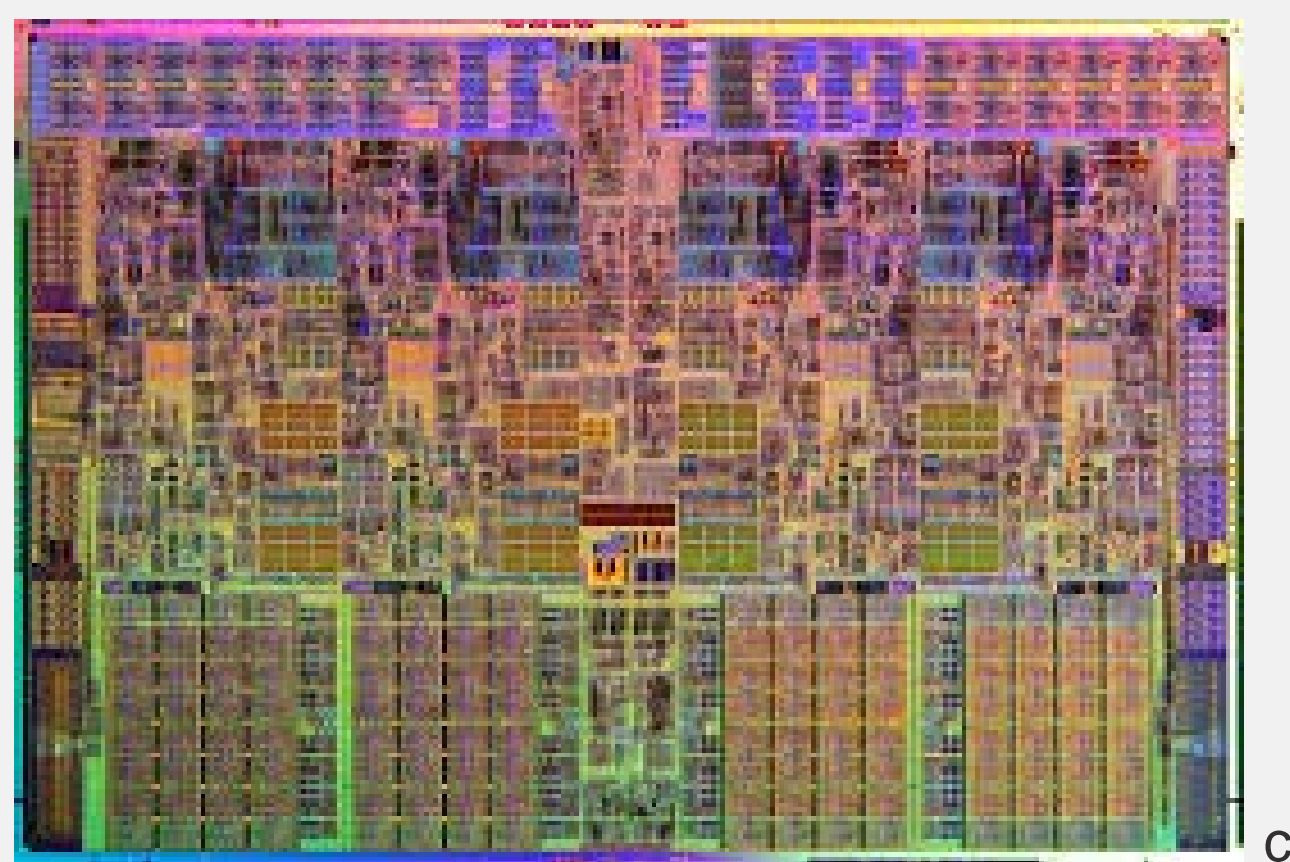
## Heterogeneous Chiplets, Flexible Integration



## Current Approaches

### Monolithic Integration

- Soft IP reuse
- High design effort, high risk
- Cost prohibitive



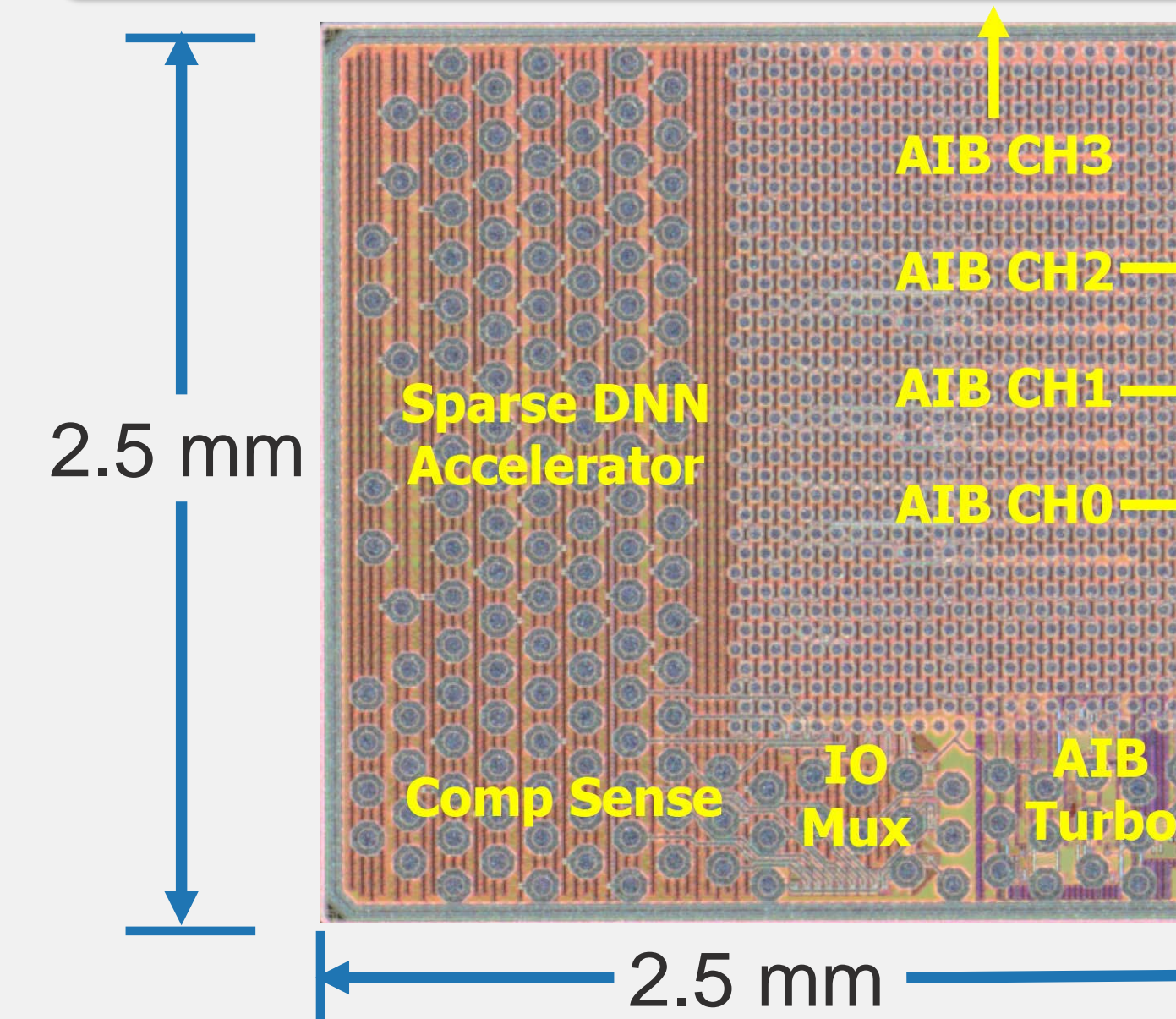
### Board-Level Integration

- Hard IP reuse
- Heterogeneous integration
- Low performance

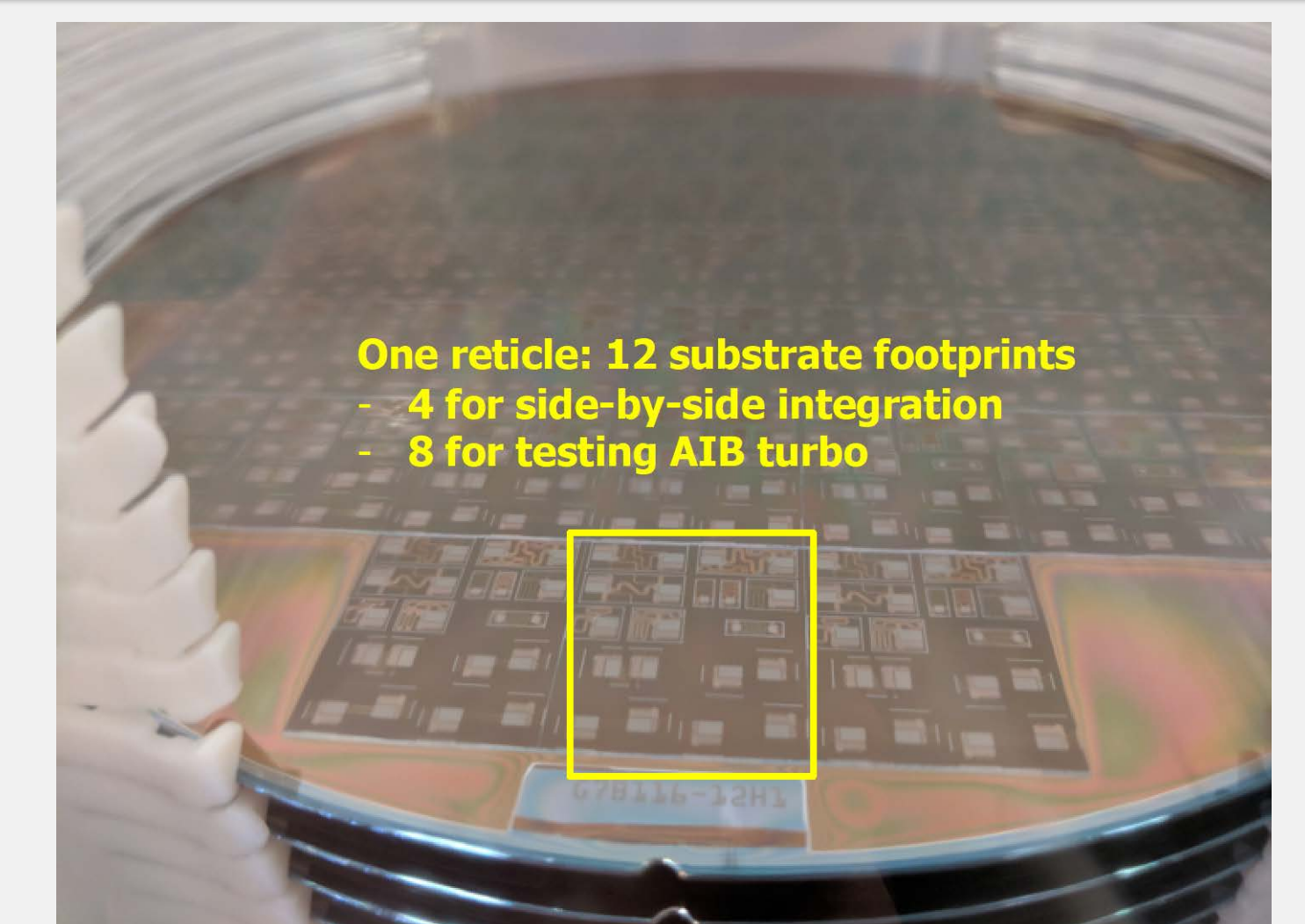


## Chiplet and Substrate Prototype Design

### 16 nm CMOS AIB Test Chip with Micro and Core Bumps

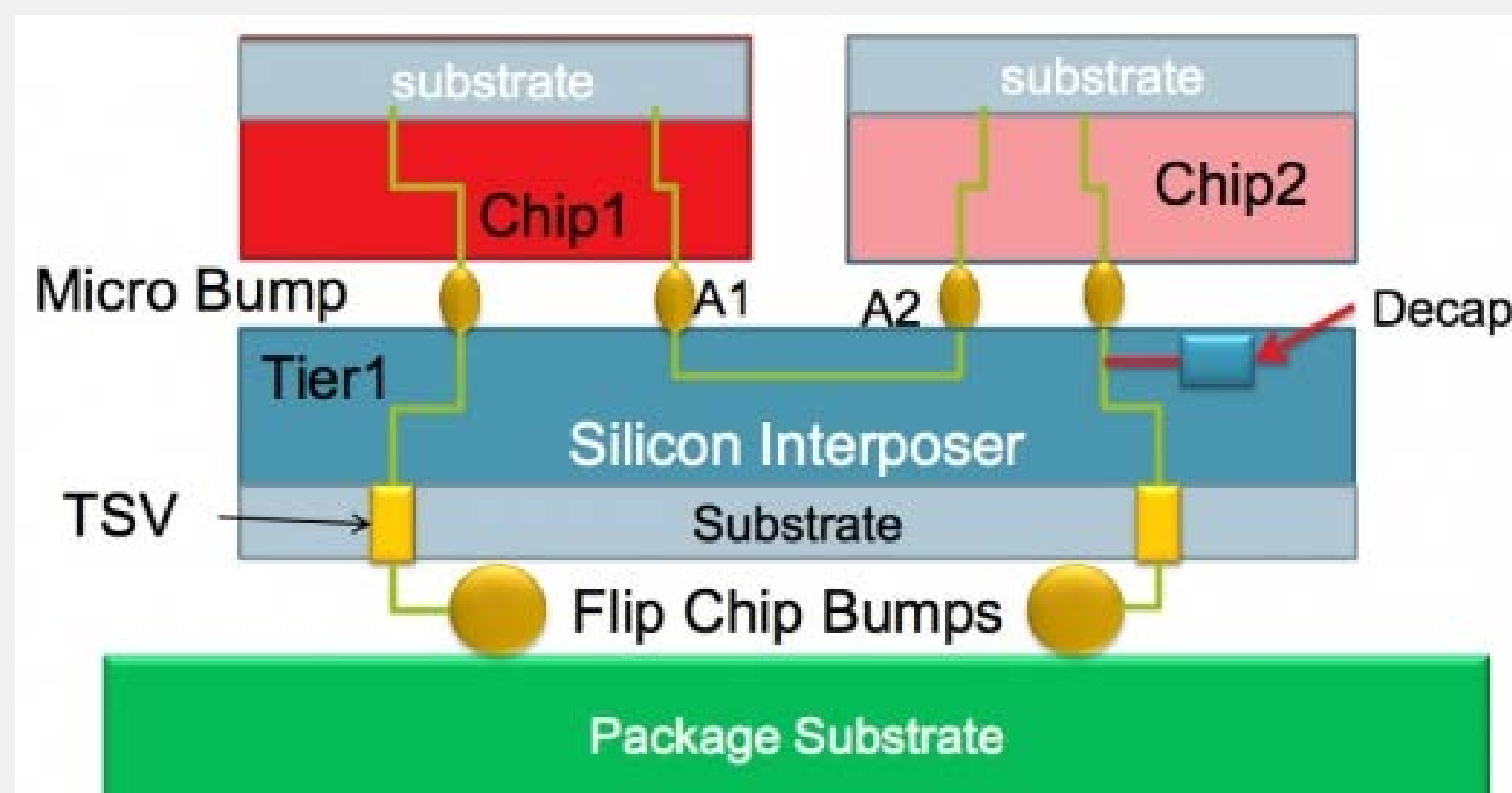


### 180 nm Passive Silicon Interposers



200mm CMOS wafers

## New Approach: 2.5D Integration



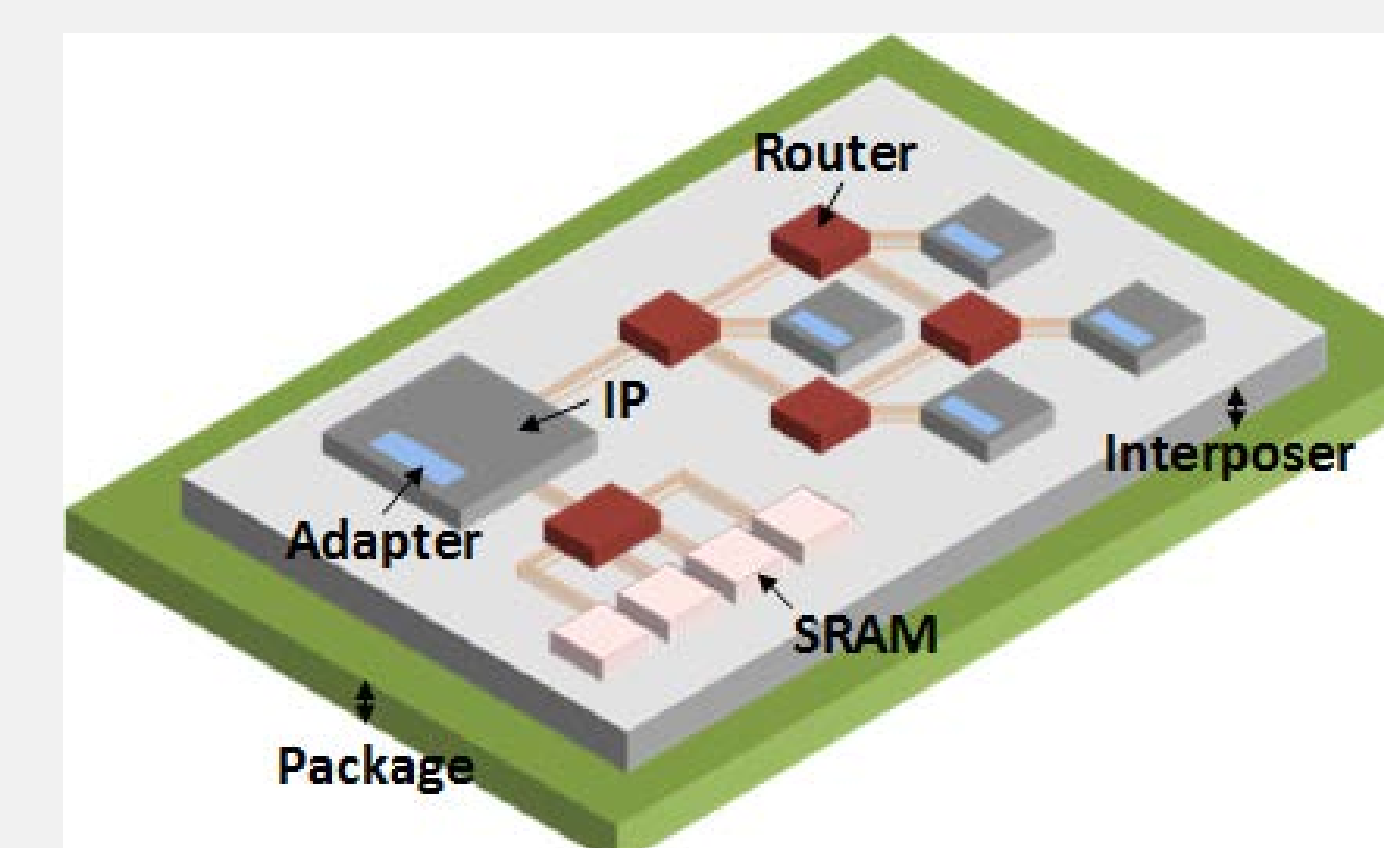
### Benefits:

- Hard IP reuse
- Lower effort, risk, & cost

### Challenges:

- Standard interface
- High-speed IO
- Availability of IPs

## Phase 1 Demo Systems



A large-scale AI system composed in 2.5D using chiplets

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## Potential Impacts

- IP reuse: >80%
- Heterogeneous integration
- NRE reduction: >70%
- Time reduction: >70%
- Performance: >100%

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