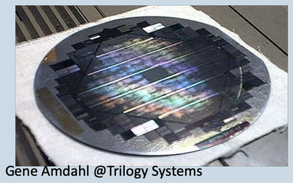
# Heterogeneous Systems-on-Wafers

**Siva Jangam, Boris Vaisband, and Subramanian S. Iyer**
**University of California, Los Angeles**

## 3D Heterogeneous Integration: Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)

*"It may prove to be more economical to build large systems out of smaller functions, which are **not packaged** ~~separately packaged and~~ **but intimately interconnected**."*
*—With apologies to Gordon Moore*


Gene Amdahl @Trilogy Systems

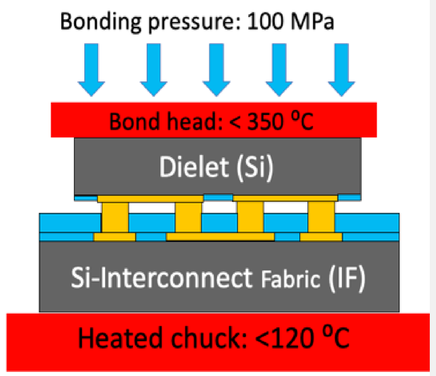
Early attempts at monolithic Wafer-Scale-Integration failed mainly due to yield limitations
Lets revisit this problem using advanced packaging and build Heterogeneous Wafer Scale Systems

Our approach:

- Replace PCB with a silicon wafer with fine pitch wiring - the **S**ilicon **I**nterconnect **F**abric (Si IF)
- Assemble heterogeneous dielets on the SI IF at 2-10 μm dielet-to-Wafer pitches (vs ~500 μm)
- Place these dielets as close as possible to each other i.e. 20-100 μm spacings (vs ~mm )

**You now have a Heterogeneous System-on-Wafer**

### Thermal Compression Bonding: Cu terminated dielets to Cu pillars on Si-IF




Challenges:

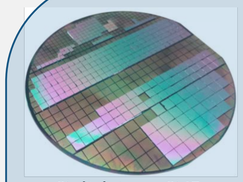
- Surface roughness
- Surface cleanliness

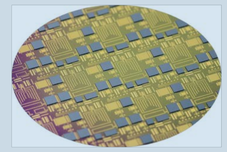
Process Parameters

- In situ cleaning
- Pressure
- Temperature
- Time

Material Parameters:

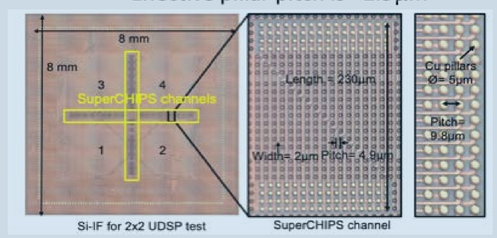
- Diffusivity
- Plastic Deformation

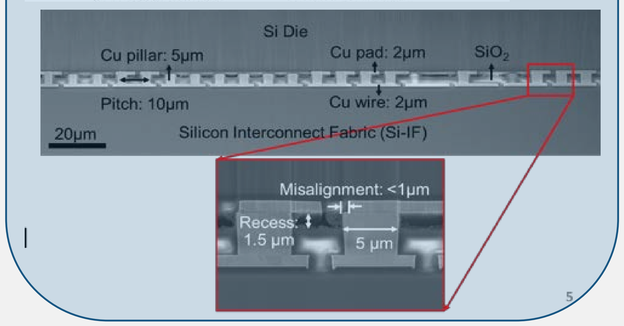

Si dielets on Si IF


InP dielets on Si IF

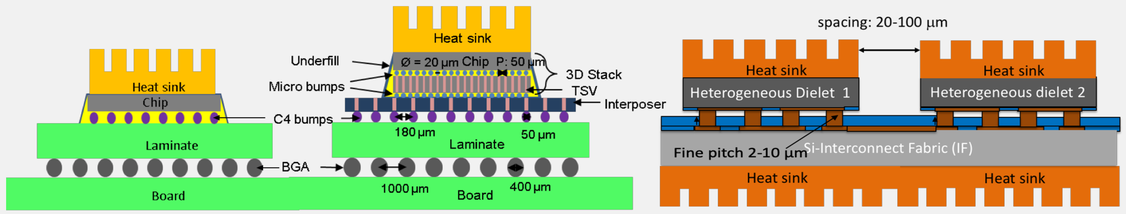
- Up to 4 Si IF wiring levels
- Pillar pitch 10μm - legacy compatible (> 200μm)
- +/- 1 μm alignment
- Cu (Si dielets) or Au (III-V dielets) terminations - No Solder
- Both shear force and resistance better than BGAs

2 wiring levels & 4 rows of pillars
=>Effective pillar pitch is <2.5μm




### PCBs vs. 3D/Interposer vs. Si-IF





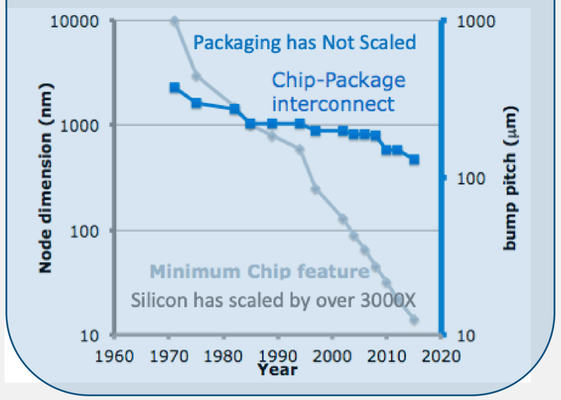


- Multiple packaging levels
- Limited heat sinking
- Solder based interconnects
- Underfill needed
- Limited by BGA pitch

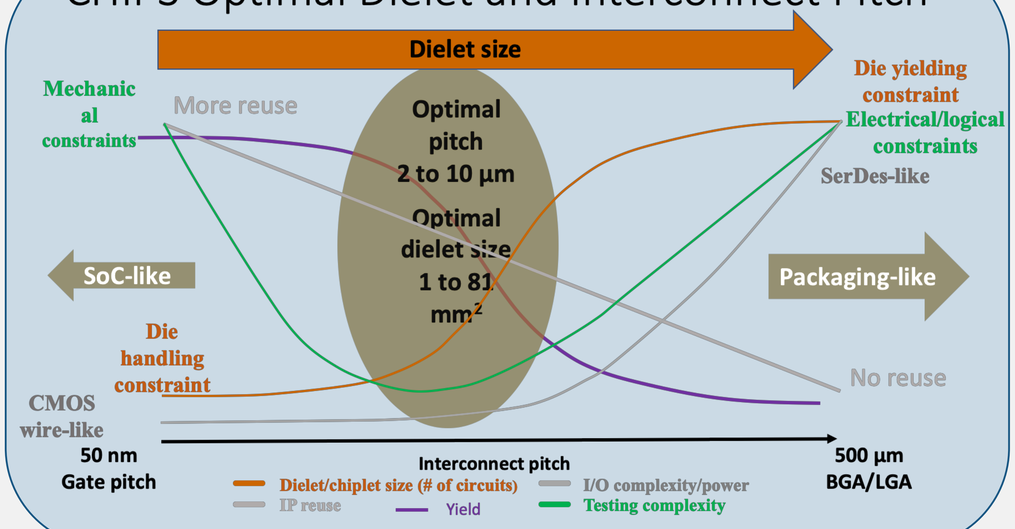
- PCB with and extra level
- Size limitation
- Needs expensive TSVs
- Interconnect pitch: 50 μm
- Thermal issues

- Single package level
- Excellent heat sinking
- Metal-metal interconnects
- No underfill
- Complete system integration

### Need a Moore's Law for Packaging!




### CHIPS Optimal Dielet and Interconnect Pitch




| *Interconnect pitch/protocol* | *10 μm on Si-IF SuperCHIPS* | | *50 μm on Interposer HBM2* | *400 μm on PCB/ SerDes* | *Improvement* |
|---|---|---|---|---|---|
| | *Async* | *Sync* | | | |
| No of links/mm | 200 | | 20 | 2.5 | 10-100X |
| Latency (ps) | 35 | 1 clock cycle | 240[2] | ~1,000 | 7-30X |
| Data-rate/link (Gbps) | 10 | 4 | 2[3] | 64[1] | 0.1-5X |
| Energy/bit (pJ/b) | <0.04 | <0.2 | 3.8[2] | 5.1[1] | 20-120X |
| Bandwidth/mm (Gbps/mm) | 8000* | 1600* | 170[3] | 90 | 10-100X |

**Small dielet integration on Si-IF enables:**

- **SoC performance (latency, bandwidth)**
- **>100x reduction in energy per bit**
- **Significantly reduced time to market**
- **10-50X reduction in NRE**
- **IP reuse**
- **Heterogeneity**

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