Development of Next Gen Processors

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Specialized Functions: Domain-specific System-on-Chip (DSSoC)

Overview and Background

The DASH-SoC team drives flexible DSSoC computational systems that reduce SWaP numbers and also dramatically increase processing flexibility.

Domain-Focused
Advanced
Software-Reconfigurable
Heterogeneous **SoC**

We break the fundamental trade that custom SoCs are required for power efficiency, but scalar processors are required for ease of implementation.

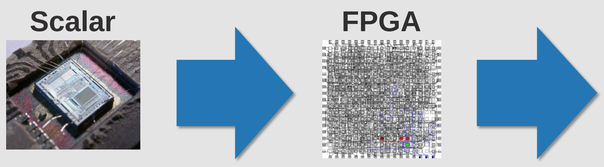
Goals

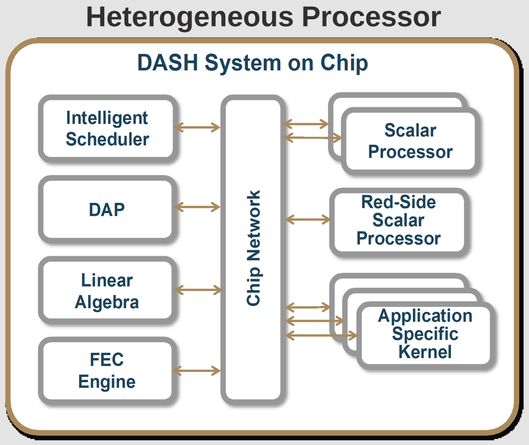
The main goal is to develop a chip as computationally powerful as a custom ASIC, but also as flexible and easy to program as a scalar processor. Specific goals include:

- Develop tools to design and use heterogenous processor for a range of signal processing applications
- Dramatically improve power efficiency
- Dramatically reduce engineering cost during SoC design and implementation

Evolution of Processors

- Transition from current scalar and FPGA approaches to heterogenous processor
- Improve computational performance
- Circumvent rigid custom SoC limitations





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This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA). The views, opinions and/or findings expressed are those of the author and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government.

Acronym	Definition
DAP	Domain Adaptive Processor
FEC	Forward Error Correction
QEMU	Quick Emulator
SoC	System on a Chip
ASIC	Application-Specific Integrated Circuit

Approach

- Provide tools across time scales: characterization & design, programming, and intelligent real-time resource management

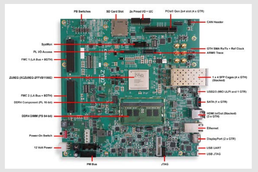
Characterization
Design
Compile Time
Runtime

Determine Characteristics of SoC → Design the Chip → Provide Software & Debug Tools → Intelligently Manage SoC Resources

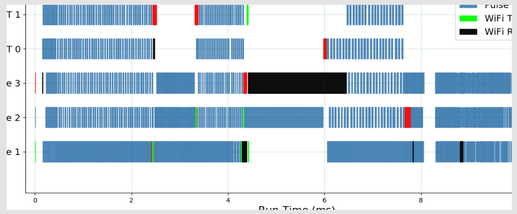
- Aid implementation by providing software design and testing support for heterogeneous processors
- Manage SoC resources with heuristic and learning systems
- Demonstrate tools and chip with over-the-air experiments

Results/Impact

- Developed high-performance ontological analysis tools
  - Demonstrated on multiple applications via LLVM extensions
- Automatically mapped algorithms to example chip layouts
- Developed QEMU simulation to enable system analysis
- Demonstrated preliminary intelligent scheduling on FPGA hardware emulations with hardware accelerations
  - Implemented multiple example processing elements



ZCU102 Evaluation Board



Task Scheduling

- Driving toward detailed hardware specification and performance estimates
- Developing multiple innovative processing elements
  - Energy Efficiency of DAP is 250 GOPs/W and unified FEC is 1 TOPs/W
  - 70x - 150x better than current general purpose processors (w/o compromising programmability for wireless communications applications)

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