Analog Mixed Signal (AMS) Open-source IP Ecosystem

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Design & Security: Posh Open Source Hardware (POSH)

Overview

- DARPA-funded ERI POSH TA-2: ***Open-source*** *automated analog mixed-signal (AMS) IP schematic generation and distribution via POSH repository*
- Start date June 25, 2018
- Leverage USC circuit designs in GF65LPe and GF12LP FinFET
- IP blocks that meet or exceed performance metrics at month 48:
  - PLL range: 10 MHz – 10 GHz
  - DLL range: 10 MHz – 10 GHz
  - ADC range: 1 – 10,000 MS/s
  - DAC range: 1 – 10,000 MS/s
- Key aspect of technical approach is use of machine learning (e.g., ANN) and optimization (e.g., convex) around known-good design (KGD) points
- Library of validated open-source mixed-signal IP circuit modules with initial delivery to repository at month 6
  - USC_65nm_SAR_ADC_Dec20_2018

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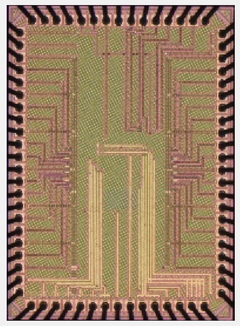
https://github.com/USCPOSH/usc-posh

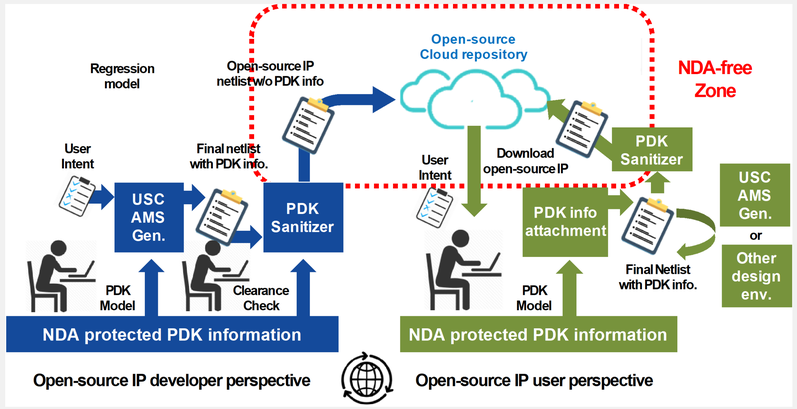
Background

- Previous attempts and lessons learned suggest narrow focused effort around proven known good designs (KGDs) and limited choice of architectures will be most successful approach
- Leverage extensive silicon-proven AMS and optimization experience at USC



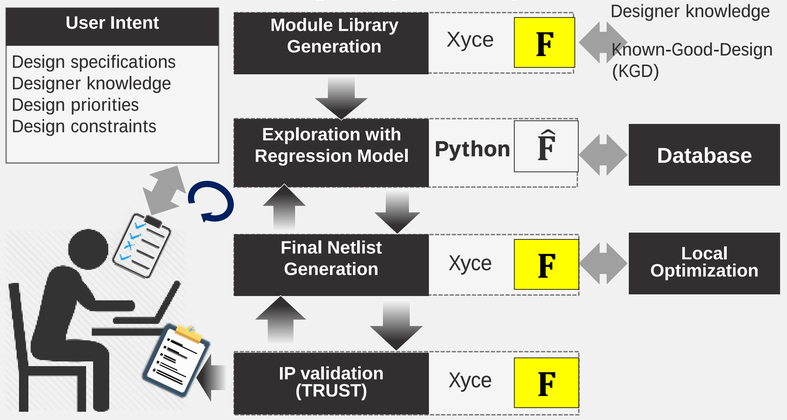
Research

Open-source IP development ecosystem



- Sanitizer tool to migrate IP (netlists) from NDA-controlled to NDA-free (i.e., open-source) zone
- De-sanitizer tool w/ NDA to migrate sanitized IP from NDA-free to NDA zone for customization
- GitHub repository for KGD, open-source software, open-source design and test-bench modules

Open-source IP Generator: AMS Parameter Search Engine (AMPSE)



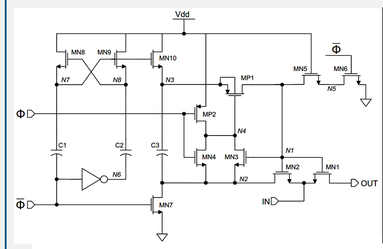
- Silicon-proven KGD in bulk CMOS and FinFET
- Automated IP generation with global (neural networks) and local convex optimization
- Open-source IP validation: TRUST system

Impact

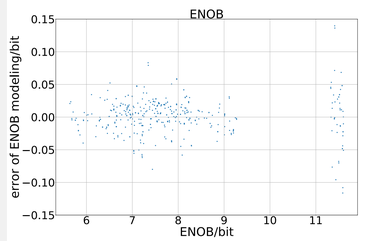
Fast circuit module modeling

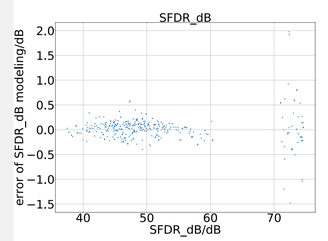
Neural network based regression model used to characterize parameters-to-metrics mapping of primitive AMS circuit modules. Has sufficient modeling accuracy for appropriate AMS metrics.

Example: bootstrap sampler modeling



Parameters	Metrics
Next stage loading (F)	ENOB (bit)
Sampling capacitance (F)	
Switch size (m)	SFDR (dB)
Sampling frequency (Hz)	

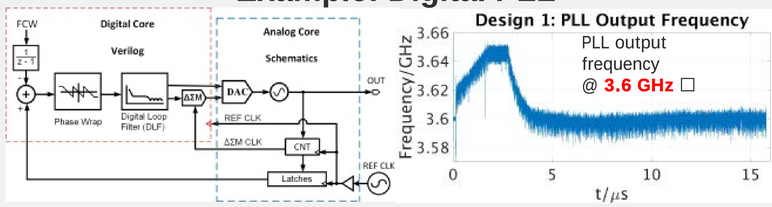




Fast block-level circuit netlist generation

Based on designer's knowledge, block-level specifications are divided into module constraints. In the AMPSE design flow, module-level regression is used to efficiently generate block-level netlists.

Example: Digital PLL



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