OpenFPGA: A Framework Enabling Rapid Prototype of Customizable FPGAs

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Design & Security: Posh Open Source Hardware (POSH)

Motivations

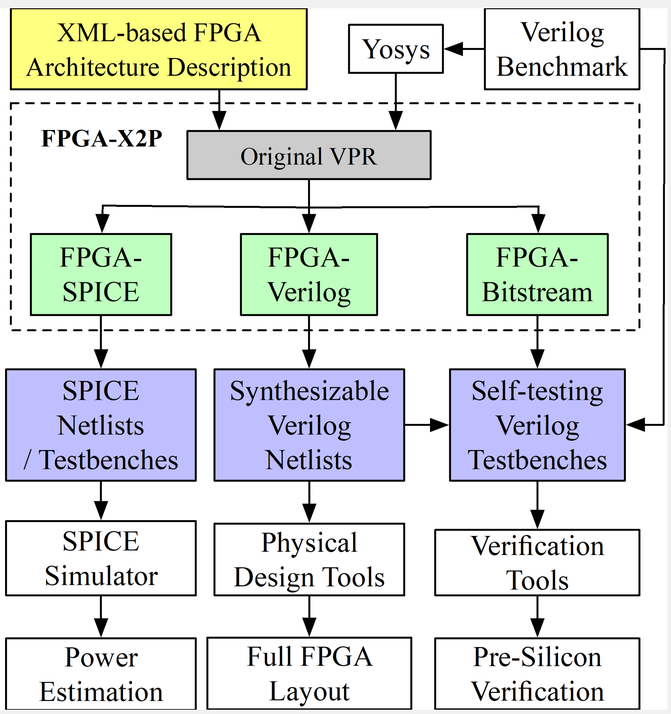
Most FPGAs are close-source and developed in full-custom approaches:

- **Year-long development cycle**
- **Teams of hardware engineers to produce manual layouts**
- **Teams of software engineers to develop ad-hoc CAD tools**
- **Rework when technology changes**

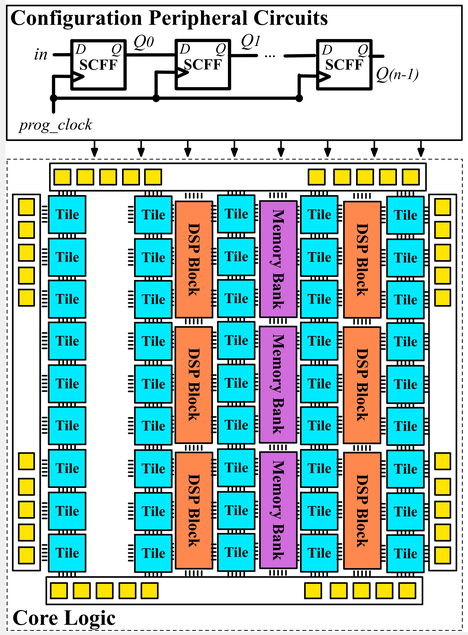
OpenFPGA Overview

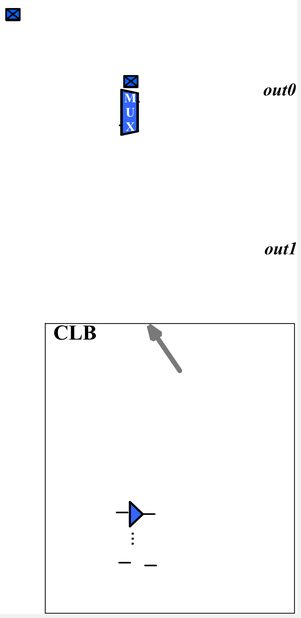
Use semi-custom design approaches:

- **Fully customizable architecture using a XML-based language**
- **Technology-independent Verilog netlists, testbenches, P&R scripts**
- **Automatic layout generation**
- **Instant Verilog-to-Bitstream support**



Rapid Prototyping FPGA from XML-to-Layout





- **Homogeneous FPGA**
- **Heterogeneous blocks**
- **Fully customizable multi-mode CLB support**
- **Standard cell support**
- **Support customized cells and even circuit designs, e.g. multiplexers, LUTs**

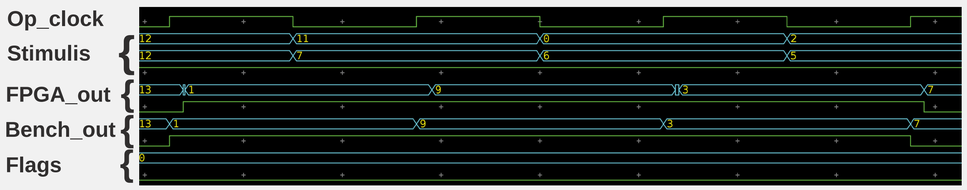
Full-fabric Pre-silicon Verification

Verified >30 benchmarks

- **HDL simulation with testing vectors**
- **Formal verification**

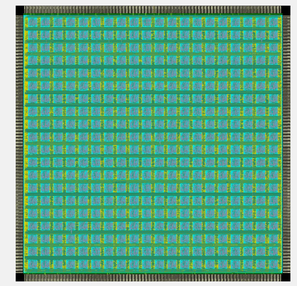
Supported Tools

- **Synopsys VCS&Formality**
- **Mentor ModelSim**
- **Icarus**

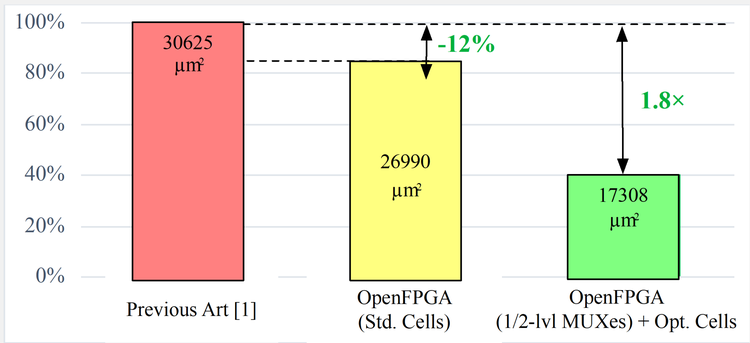


Pre-silicon Evaluation

- **Technology node: 40nm**
- **FPGA Architecture: a 20x20 array of Stratix-IV-like CLBs**
- **Customized cells for multiplexers and SCFFs**
- **Fabric GDSII generation: ~24hr**



Area: (measured by GDSII layout)



Performance: (STA on GDSII layout)

Path Type Delay (ns)	Previous Art (TT) [1]	OpenFPGA (TT)
5-LUT	0.46	0.14 (3.3x)
6-LUT	0.5	0.15 (3.3x)
1-bit Adder	0.7	0.49 (1.4x)
20-bit Adder	1.63	1.04 (1.6x)
Local Routing	0.27	0.14 (1.9x)
L-4 track	2.53	0.52 (4.9x)
L-16 track	4.02	1.00 (4x)
Average	100%	2.9x

Github Repository:
https://github.com/LNIS-Projects/OpenFPGA
Online Documentation
https://openfpga.readthedocs.io/en/latest/

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Reference:
[1] B. Grady, J.H. Anderson, "Synthesizable Heterogeneous FPGA Fabrics," the IEEE International Conference on Field-Programmable Technology (IEEE FPT), Naha, Japan, December 2018.