Development of Next Gen Processors for RF Systems
DASH - SoC (Heterogeneous SoC)

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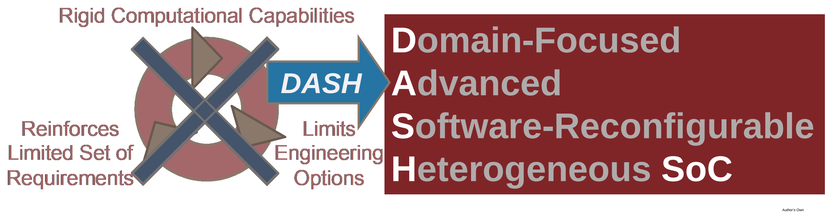
ELECTRONICS RESURGENCE INITIATIVE SUMMIT & MTO Symposium 2020 | Seattle, WA | August 18-20

Domain Specific System-on-Chip (DSSoC)

5G and Future RF

Background

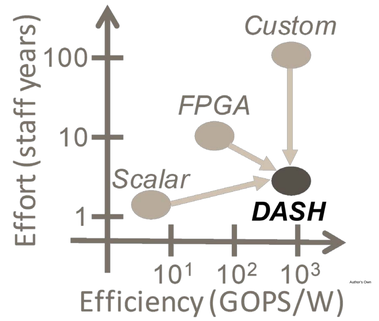
The DASH team is building a framework to develop flexible, high-performance, low-power, domain-specific SoCs, while assuring non-expert programmability. We are developing an example SoC for software-defined RF systems: radios; radars; spectral awareness; positioning, navigation, and timing; and RF convergence. DASH allows RF system designers to escape the traditional power & development-cost limits to innovation.

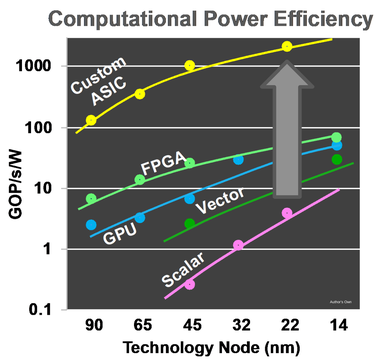


Goals

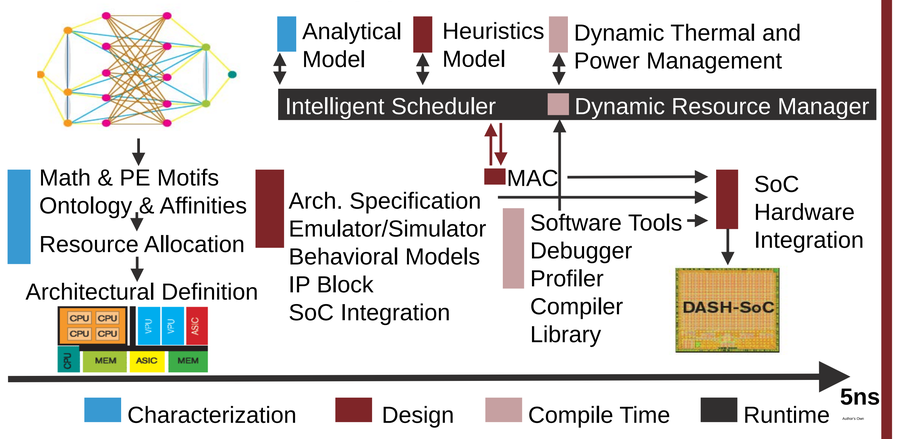
We develop an SoC that is as computationally powerful as a custom ASIC and as flexible and easy to program as a scalar processor.

- Develop tools to design and use a heterogenous processor for a range of signal processing applications
- Significantly improve power efficiency
- Dramatically reduce cost of implementation effort for heterogeneous SoCs

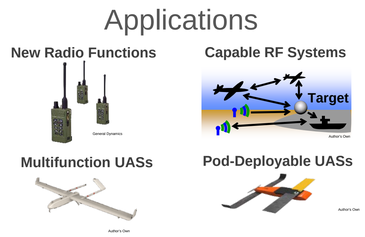


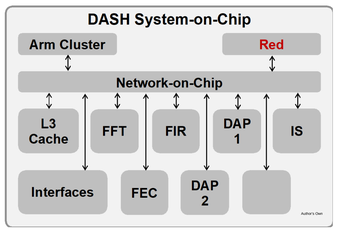


Approach



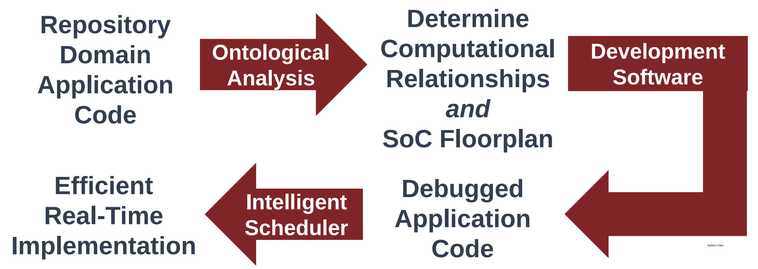
- Provide tools across time scales: characterization & design, programming, and intelligent real-time resource management
- Automate application mapping and architecture-aware code transformations through LLVM IR analysis, semantic optimization, kernel-based DAG generation and multi-function binary representation.
- Develop custom IL tool to rapidly implement optimize scheduling and thermal management strategies to dispatch applications on heterogeneous processors
- Optimize high-performance Arm CMN-600-based network-on-chip
- Develop novel flexible accelerators (advanced systolic array and unified error-correction processors) to supplement array of fixed accelerators





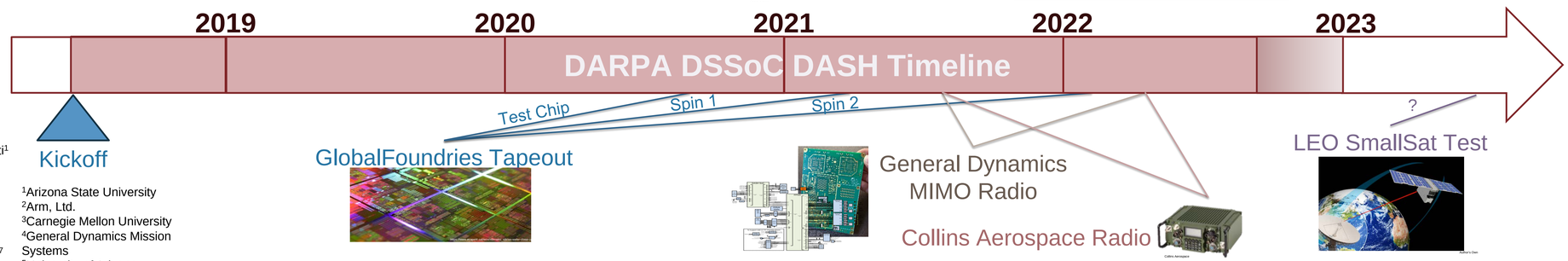
Results and Impact

- Estimated power consumption to be within a factor of 2 to 3 of full-custom for multiple applications
- Demonstrated novel dynamic tracing tool (speed ~ 50x)
- Developed a formal representation for parallel kernels to support heterogenous processing
- Demonstrated automatic fat-binary code transformations across processer types
- Demonstrated rate-flexible SoC network on-chip (RTL, latency < 5 ns)
- Developed dynamic, IL-based real-time scheduler for multiple applications and accelerators (99% of optimal scheduler, FPGA-Demo)
- Developed multiple task-specific accelerators, novel high-performance systolic array accelerator, and high-performance general forward-error-correction engine (RTL, FPGA-Demo)



Impact

- Enables wide range of new abilities for 5G, DoD, and other next generation RF systems
- Supports new and evolving types of users (human and non-human) and operating environments



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Acronym	Definition
SoC	System on Chip
ASIC	Application-Specific Integrated Circuit
LLVM IR	Low Level Virtual Machine
IR	Intermediate Representation
DAG	Directed acyclic graph
IL	Imitation Learning
RTL	Register-Transfer Level

This research was developed with funding from the Defense Advanced Research Projects Agency (DARPA).
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