DEMONSTRATION OF A STRATEGIC RAD-HARD 90-nm FDSOI CMOS PROCESS

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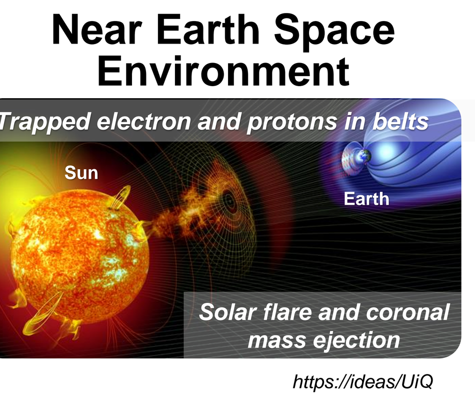
Rad-Hard Microelectronics — ***Security and Access***

Background

Strategic Rad-Hard (SRH) Applications

Extreme Radiation Levels

Near Earth Space Environment



https://ideas/UiQ

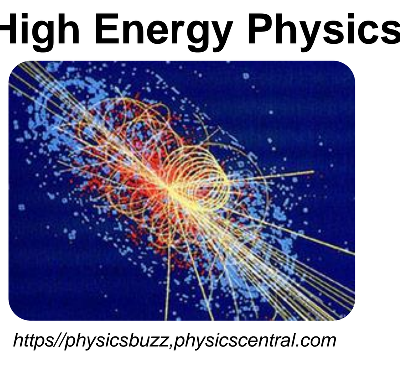
National Defense Systems

Usnews.com

Deep Space Missions

https//www.jpknasa.gov

High Energy Physics



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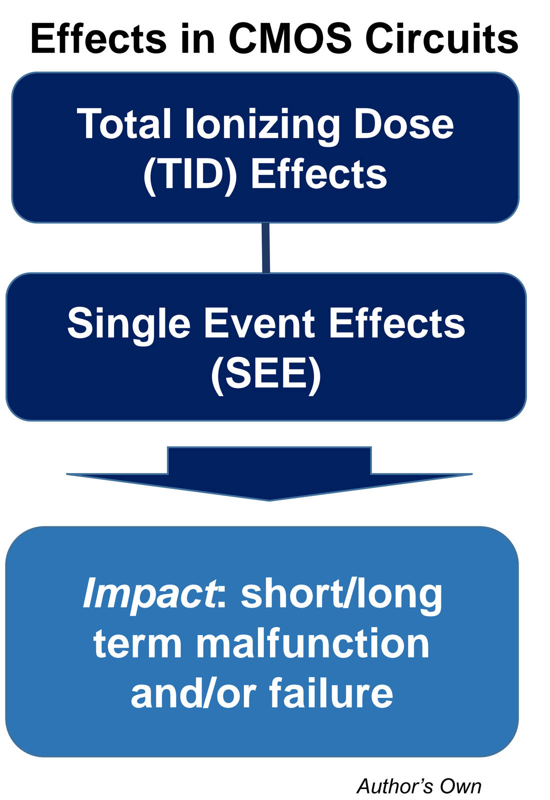
Effects in CMOS Circuits



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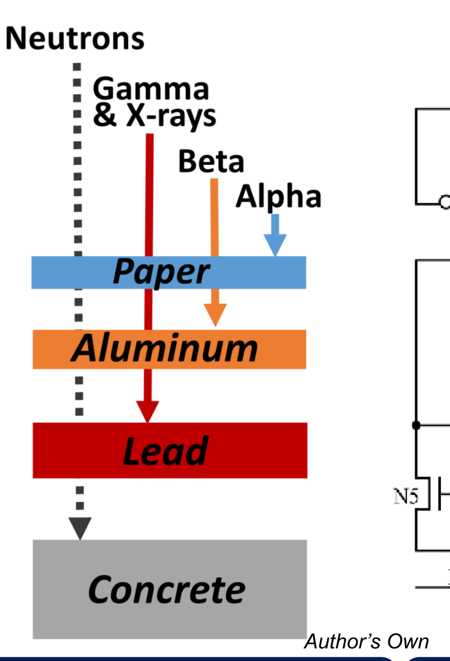
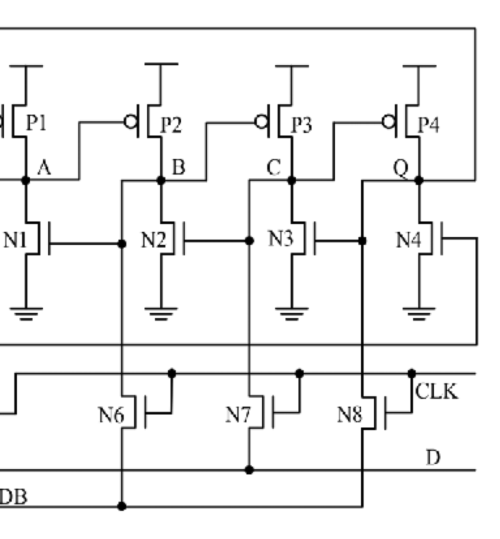
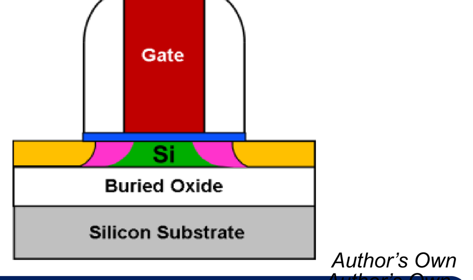
Mitigation Approaches





Silicon-on-Insulator Technology

- For best radiation tolerance
- RHBP to increase tolerance to TID and SEE effects
- Only 3 Trusted RHBP Foundries in US



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Low radiation level → *Extreme radiation level*

MIT Lincoln Laboratory 90-nm Fully Depleted SOI (FDSOI) Process

- Full CMOS fabrication at MIT LL in the Microelectronics Laboratory
  - 70k ft², Class-10 & 100 cleanroom
  - Production-class toolset for 200-mm wafers
  - ISO-9001:2015; Trusted design, aggregation, post processing and packaging certified
- Custom 90-nm Rad-Hard-by Process (RHBP) fabrication
  - FDSOI for low-power high-speed performance
  - Specialized fabrication modules to mitigate radiation-induced defects in isolation and buried oxide films for enhanced tolerance to TID
  - Most advanced RHBP node in a DoD-accredited Trusted Foundry
  - Unique RHBP FDSOI, not commercially available

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Government-owned semiconductor research and fabrication prototyping facility that supports the design, fabrication, and packaging of specialized devices

MINSEC Program Goal
Demonstrate the capabilities of MIT LL 90-nm RHBP FDSOI process for Strategic Rad-Hard applications

Approach

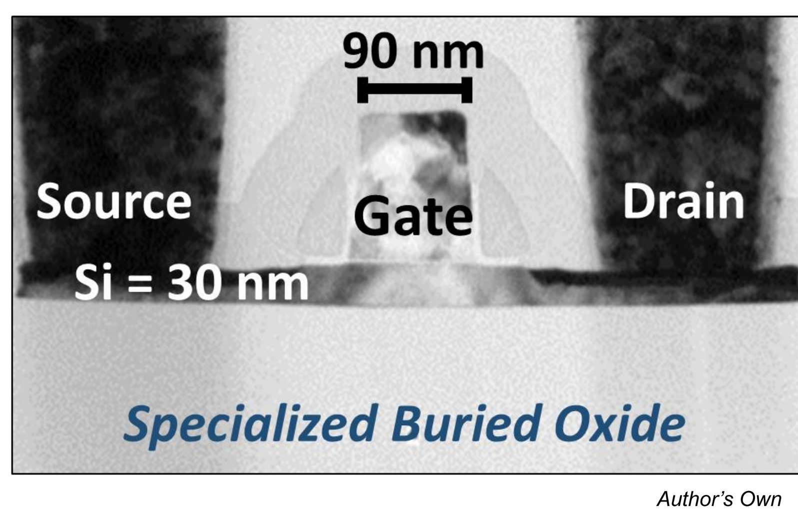
Initial Phase

- Leverage expertise and collaborations across government laboratories and FFRDCs
  - NSWC Crane, NIWC Pacific, DMEA, Sandia National Labs, DRAPER
- Design and fabricate radiation test vehicles with and w/o RHBD
- Develop rad-hard transistor designs with effective body contacts
- Develop standard cell libraries and IP for Rad-Hard circuit design
- Develop technology computer-aided design (TCAD) simulation decks

90-nm RHBP FDSOI Features

Core Voltage	1.2 V
Gate oxide	1.8-nm, SiON
Isolation	Shallow Trench
Min width, length	L=90 nm, W=200 nm
SOI	30 nm thick
Threshold, V_{TH}	Dual – high, low
Leakage, Ioff	< 1nA/µm
Silicide	$CoSi_2$
7 Metal AlCu	5M: t= 200 nm, 2M: t= 0.5 and 5 µm
Resistors	15 to 3,000 ohm/sq
Capacitors	MOScap, Varactor, VNCAP, BOXCap
Inductor	M7 spiral, nH range

90-nm FDSOI SEM Cross-section



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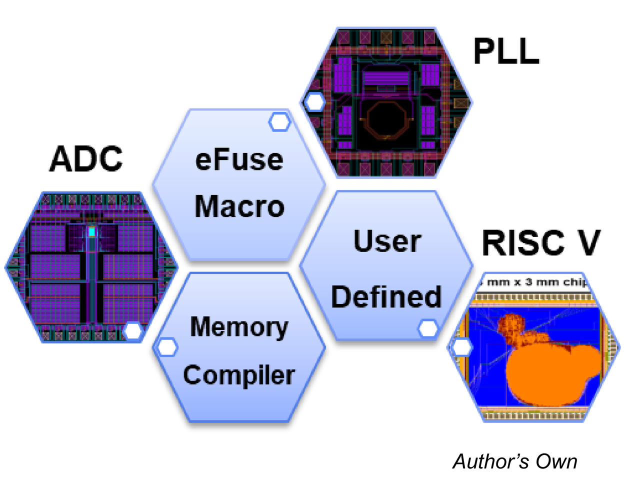
FDSOI IP in Development



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MIT LL Prototyping Flow

Design support
- Comprehensive PDK, Cadence & Calibre tools
- Validated custom & digital design flows
- Standard Library and IP (standard & Rad-Hard)

Reticle Assembly
- Floor planning
- Final DRC, design-to-mask translation, OPC
- GDS layer to external mask vendor

Fabrication
- Full flow in the Microelectronics Lab
- Extensive in line monitoring

Automated testing
- Keithley S600, Veriigy 93000
- Aracor 4100

Packaging
- Wirebonding
- Bump bonding
- 2.5D and 3D integration

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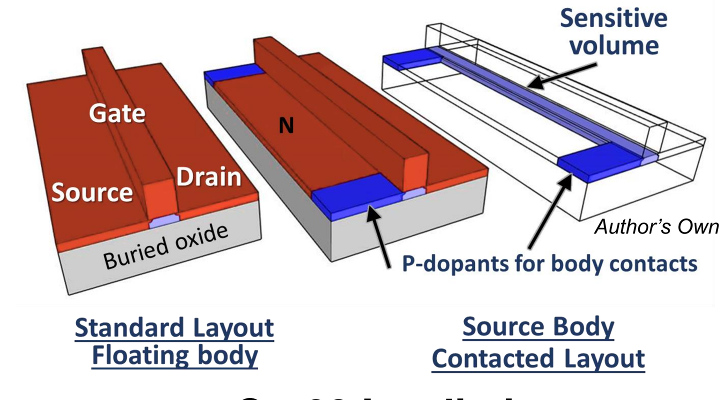
Ongoing Phase

- Transfer MIT LL 90-nm FDSOI process to SkyWater for SRH CMOS circuit production for government and commercial applications
- Support commercial partners development activities
- Continue developing process enhancements and extend process capabilities
- Support radiation effect simulations in collaboration with government and industrial partners

Results and Impact

Rad-Hard Transistor Designs

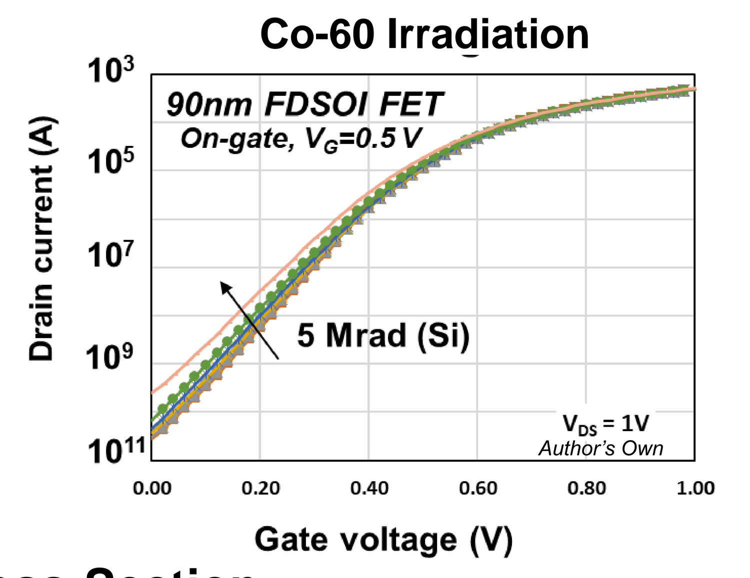
- Demonstrated designs with effective body tie to suppress floating body effects: source-body-contact, T-gate and H-gate variants



TID Demonstration

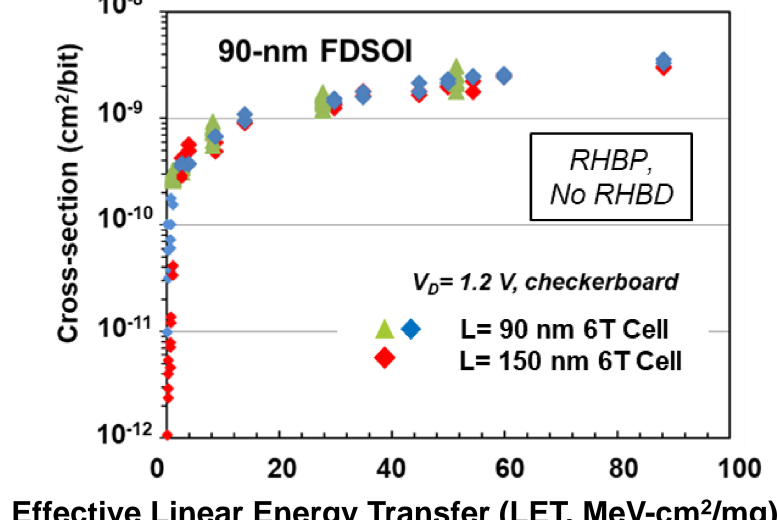
- Transistor testchip with various widths and lengths
- Threshold voltage shift ~ 25 mV at 1Mrad(Si) and ~ 73 mV at 5 Mrad(Si) for all of the transistor geometries.
- Transistor operation not degraded up to 5 Mrad(Si)

Co-60 Irradiation



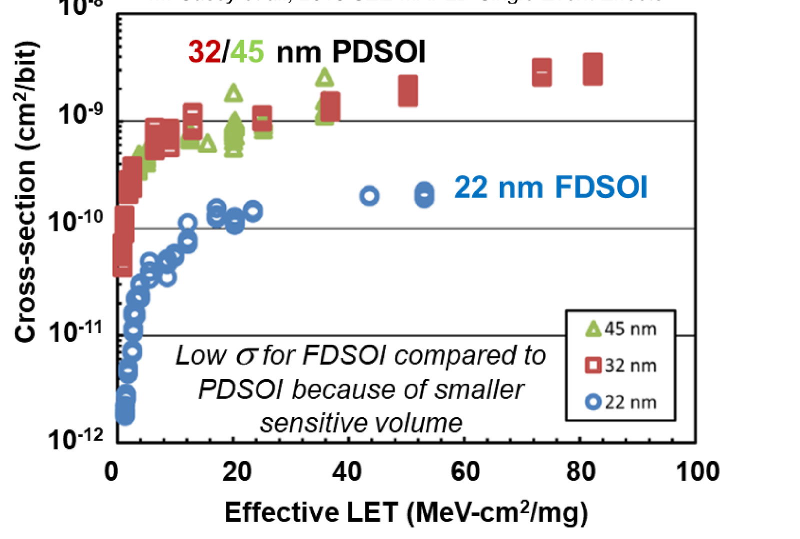
Heavy Ion Cross-Section

MIT-LL 90-nm FDSOI SRAM



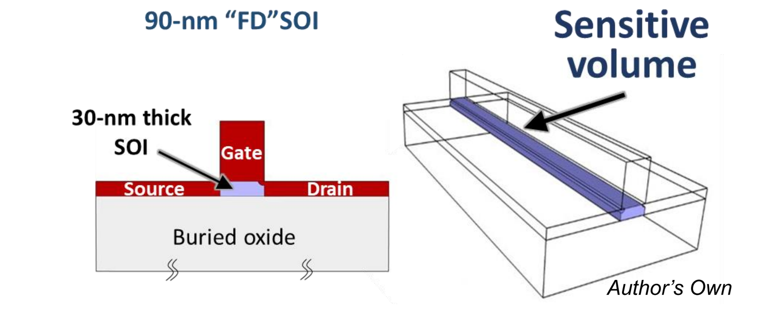
Commercial FDSOI/PDSOI SRAM[1]

[1] M. Casey et al., 2018 SEE-MAPLD Single Event Effects



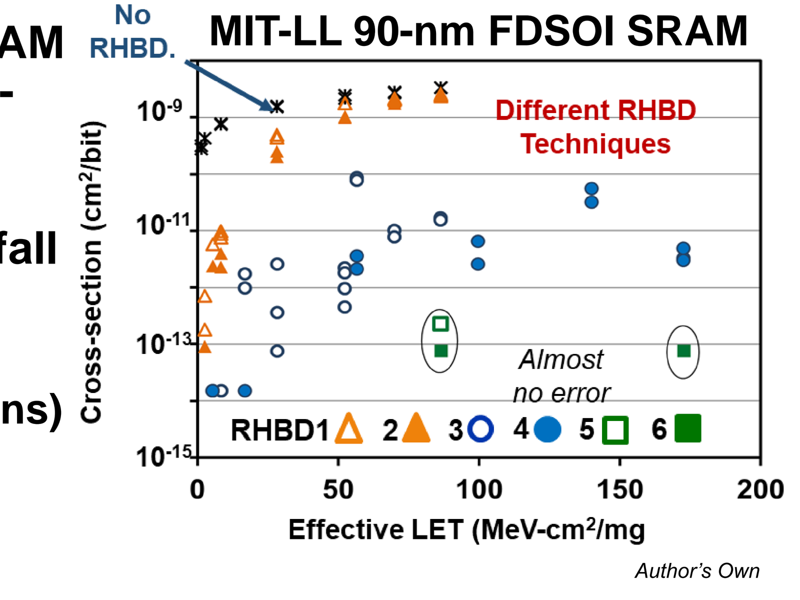
- Texas A&M tests for multiple LET & incident angles
- MIT LL 90-nm RHBP SRAM with *No Rad-hard by Design*
- Multiple bit upsets: < 1%

- Published results for commercial FDSOI and Partially Depleted SOI
  - 90-nm FDSOI equivalent to 32/45-nm PDSOI → 1 to 2 nodes performance advantage
  - Sensitive volume: FDSOI << PDSOI



- Demonstrated that 90-nm RHBP SRAM with RHBD will decrease SEE cross-section and increase LET threshold
- Next MIT LL multi-project wafer run with new RHBD prototypes due for fall 2020
  - MIT LL, DoD, DOE, FFRDC and university contributions (> 30 designs)
- MIT LL 90-nm SRH FDSOI tech transfer underway to SkyWater Technology

MIT-LL 90-nm FDSOI SRAM



MIT LL and collaborators within DoD and DOE working to ensure US leadership in SRH microelectronics

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