Aligned Carbon: Nanotubes for Integrated Circuits

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Aligned Carbon

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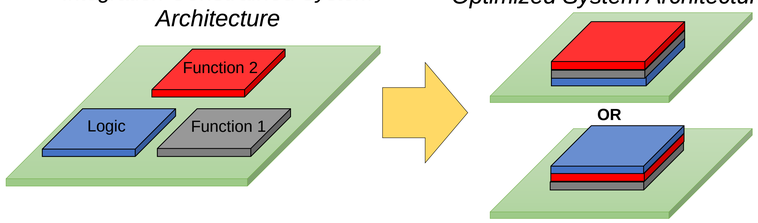
INNOVATE ***Heterogeneous 3D***

Motivation

Universal Challenge: Integration of logic with other semiconductor technologies

Integration Constrained System Architecture *Optimized System Architecture*



Integrating high performance transistors monolithically as the last layer or the middle layer of a chip enables:

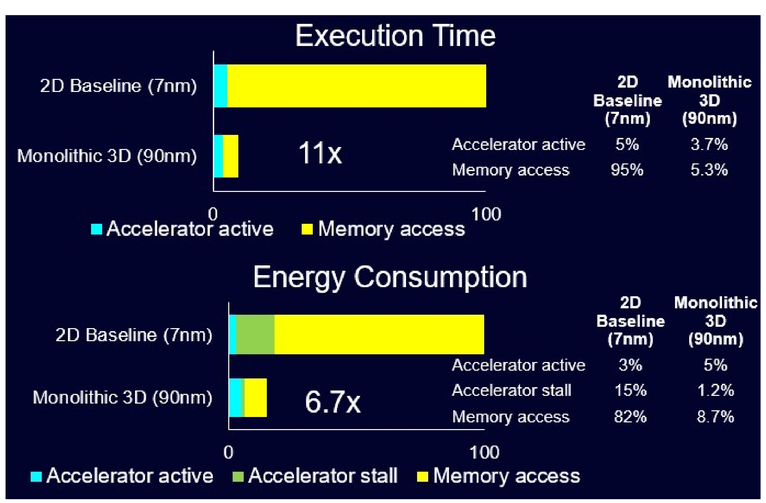
- Simplified packaging – Less chips to integrate, smaller packages.
- Improved performance – No communication bottlenecks between chips
- Lower power consumption – No high speed links or retimers

Computing — **Logic & Memory on Logic** (Memory / Logic / Logic)
Impact: >1000X throughput improvement for datacenters, edge computing, Machine Language / Artificial Intel.

Photonics — **Logic on Photonics** (Logic / Photonics)
Impact: Ultra dense and efficient optical transceivers for high throughput switch ASICs in datacenters

MEMs — **Logic on MEMs** (Logic / MEMs)
Impact: Ubiquitous sensors for edge computing

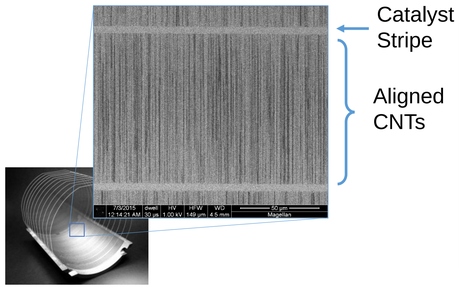
CNT-Based Monolithic 3D



S. Mitra Stanford University

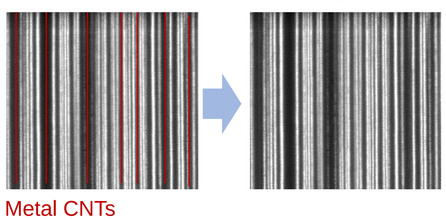
75x improvement in energy delay product (EDP) using 8 generation old silicon technology node

Approach



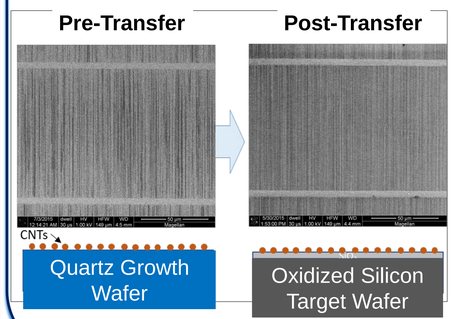
1) Aligned Growth

- Growth of high-density single walled aligned Carbon NanoTubes (CNTs) on quartz wafers 100mm (now) & 200mm (2H 2020)
- CMOS compatible catalyst stripes with >>100 µm tubes
- Leverages best known techniques and custom growth systems



2) Purification

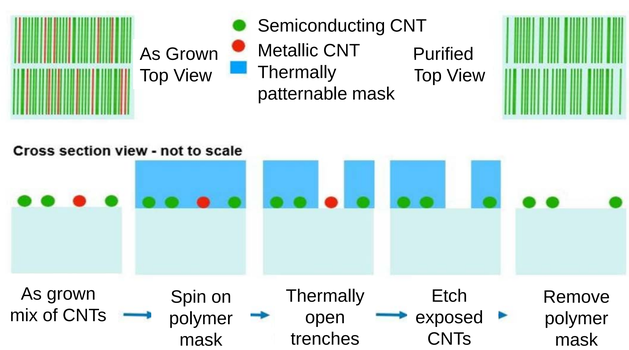
- Key company IP
- In-situ removal of metallic CNTs on the growth wafer (prior to transfer)
- Avoids need to build additional circuitry to induce electrical breakdown on target wafer
- Avoids wet bench processing of target wafer



3) Transfer

- CNTs are embedded in a CMOS compatible sacrificial layer and transferred to target wafer
- Alpha prototype transfer tool to automate transfer process availability target 2H 2020
- If needed, multiple transfers can increase density on target wafer

Purification

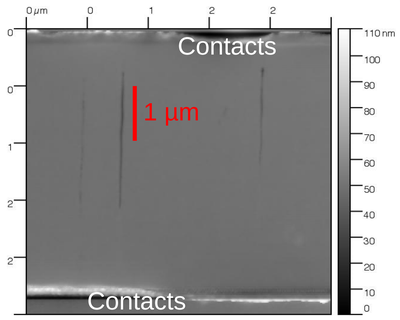


Wafer-scalable, high throughput method
Zero additional mask layers for target wafer

Purification Initial Results

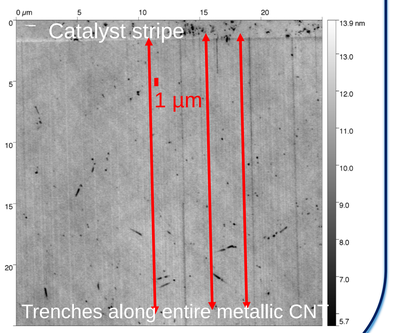
Using electrical bias to selectively open up trenches

- Transferred CNT material to target wafer and processed target wafer with 3 mask layers to enable bias to be applied and selectively heat the metallic CNTs.
- Micron-scale trenches opened in resist along metallic CNTs

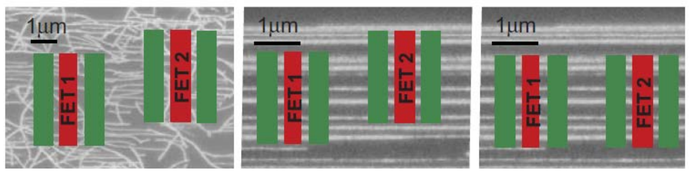


Using Aligned Carbon approach to selectively open up trenches

- CNT growth wafer covered in thermally responsive polymer and exposed leaving open trenches along the entire length of metallic CNTs
- Promising results are being optimized



Versus State of the Art



- **350x lower probability of device failure**
- **26.5x** lower probability of device failure is from building CNT Field Effect Transistors (FETs) on long, aligned CNTs
- **13x** lower probability of device failure is from aligned-active layout technique (i.e. spatial correlation of FETs with the same CNTs)

Improved Transistor Performance

- Significantly lower (~100x) device failure when employing active-align layout techniques with long (>100µm) CNT arrays
- More uniform CNT FET voltage transfer curves due to highly aligned, uniform, and pure CNTs
- Increased current density, transconductance, and lower threshold voltage of CNT FETs due to higher quality, (lower impurities and defects relative to solution-based purification) aligned CNTs

Improved Manufacturability

- Uniform CNT coverage over entire wafer
- No wet processing, consistent with High Volume Manufact. foundry approaches
- Avoids CNT aggregation & metal contamination associated with solution-based CNT purification materials
- Simplifies foundry process and supply chain

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