Photonic Chiplets for Tb/s Chip-to-Chip I/O

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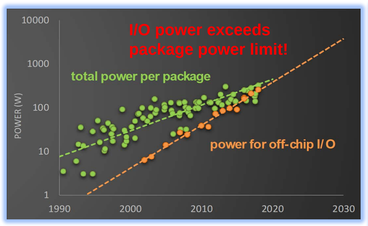
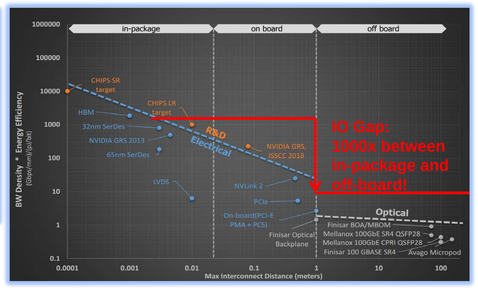
Photonics In-Package for Extreme Scalability (PIPES)

Heterogeneous 3D

Background: The Case for Optical I/O

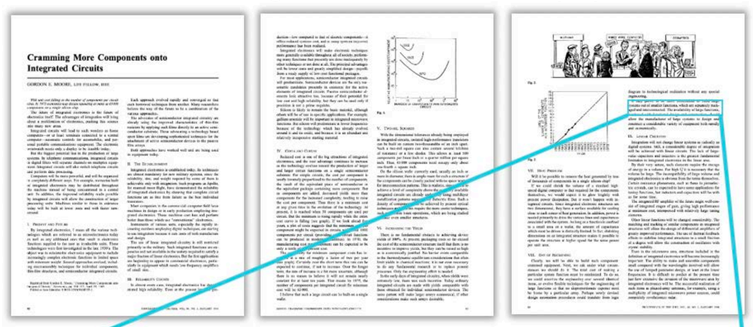


[G. Keeler, DARPA ERI 2019]



Off-chip I/O is consuming too much power and is becoming the dominant fraction of power consumption in advanced ASICs.

Gordon Moore's original "Moore's Law" paper:

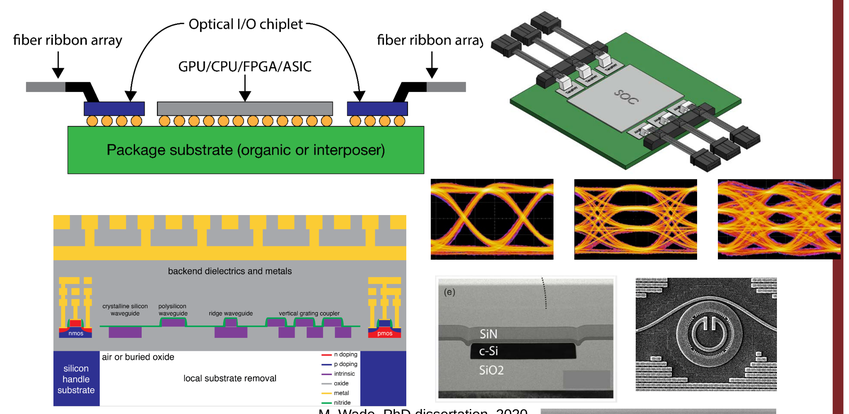


It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected.

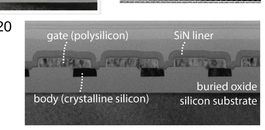
By replacing off-chip I/O with optical I/O rather than electrical I/O, the traditional bandwidth versus distance trade-off can be broken. This allows highly efficient distributed systems to be designed with impacts in:

- High-performance computing
- AI/ML
- Disaggregated compute/memory resources
- Memory semantic fabrics
- Disaggregated sensors and compute (e.g. phased array radars)

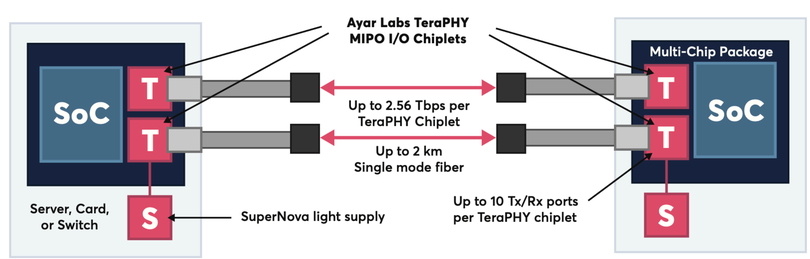
Approach: Photonic Chiplets



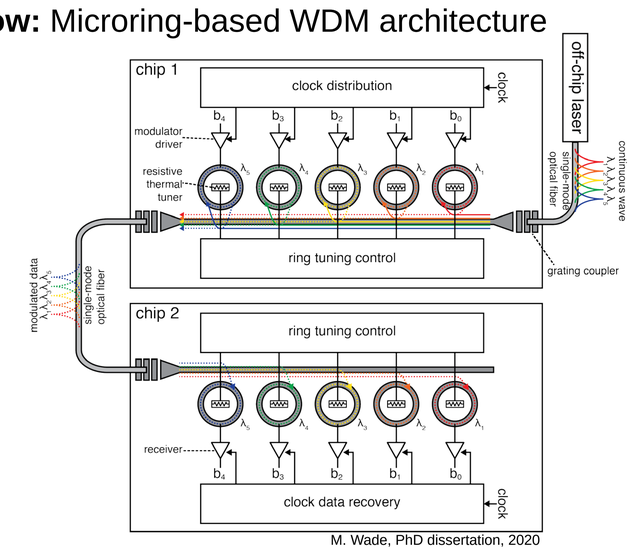
M. Wade, PhD dissertation, 2020



Monolithic integration of electronics and photonics creates a new generation of high-performance photonic chiplets.

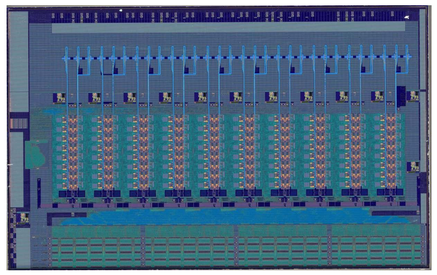


Above: Block diagram of chip-to-chip photonic I/O with external laser source.
Below: Microring-based WDM architecture

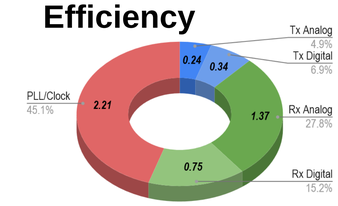


M. Wade, PhD dissertation, 2020

Results and Impact

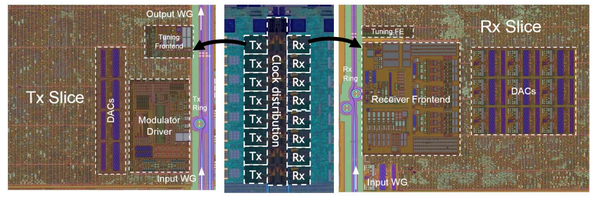


Measured Energy Efficiency

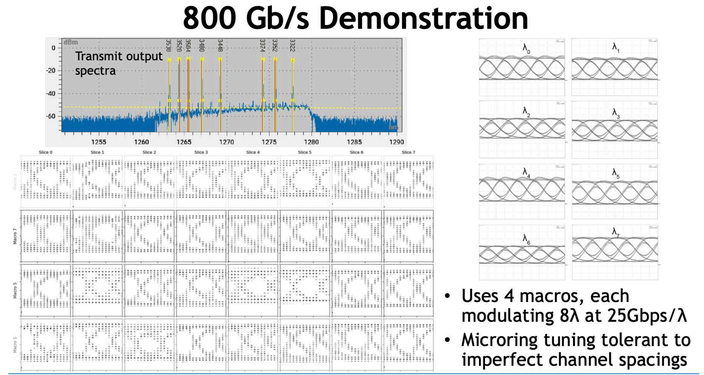


4.9 pJ/bit Tx+Rx

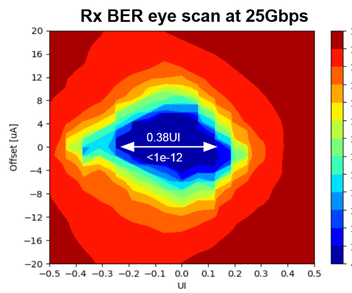
Above: Image of TeraPHY chiplet
Below: Zoom in to Tx and Rx macros

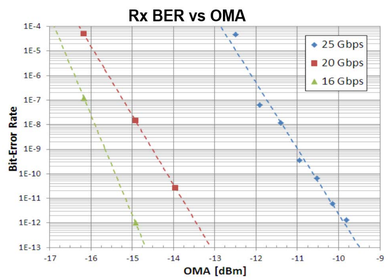


800 Gb/s Demonstration

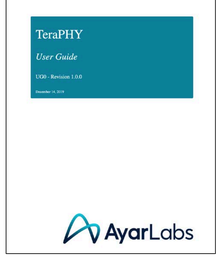


- Uses 4 macros, each modulating 8λ at 25Gbps/λ
- Microring tuning tolerant to imperfect channel spacings





Hardware evaluation kits available now!



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