Energy Efficient Electrical and Optical Co-packaged Transceiver for Large Scale In-package Optical IO

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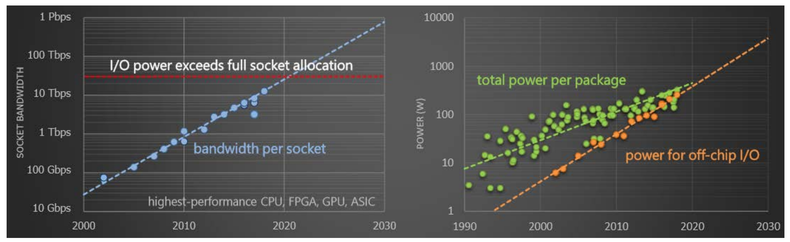
XILINX

PIPES — ***Heterogeneous 3D***

Introduction

Electrical I/O Limited in Bandwidth (BW), Power and Reach

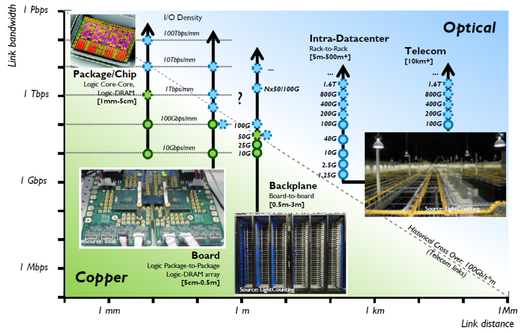
- **Thermal solution expensive→ Need disruptive power efficient solution to increase BW by 100X while staying within thermal limits**



[source: PIPES Kick-off]

Silicon photonics (PIC) based optical link a potentially disruptive solution

- **Can achieve >100X BW increase but >100X power reduction a challenge**



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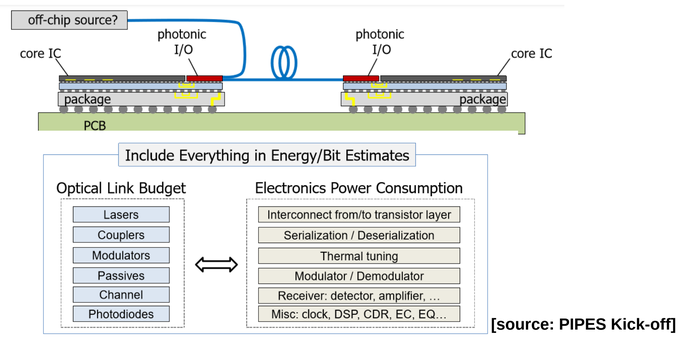
- **Power efficiency limited primarily by Electrical ICs (EIC) electrical interconnects and by optical losses including Laser wall plug efficiency (WPE)**



[source: PIPES Kick-off]

Program Goal: Demonstrate >1Tb/mm Edge BW with end-to-end <2.5pJ/b Power Efficiency including Laser

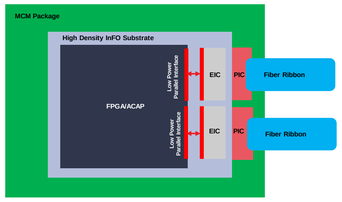
	Phase 1	Phase 2	Phase 3
Key outcomes	10T technology demonstration*	Enhanced 10T demo* AND Packaged MCM demo	100T technology demo* AND Differentiating Access
Aggregate bandwidth	10 Tbps	10T demo: 10 Tbps MCM: proposer defined	100 Tbps
Energy per bit	2.5 pJ/bit	1 pJ/bit	1 pJ/bit
Edge bandwidth density	1 Tbps/mm	2 Tbps/mm	2 Tbps/mm
Link latency	200 ns + TOF	100 ns + TOF	100 ns + TOF
Link reach (between packages)	20 meters	20 meters	20 meters
Bit error ratio (BER)	10^{-9}	10^{-12}	10^{-12}
Link margin	0 dB	2 dB	4 dB
Packaged units delivered	--	2x 10T demo units 10x MCM units	2x 100T demo units
Operating temperature range	--	Room temperature to 80°C	Room temperature to 80°C
Solder reflow compatible	--	250°C, 5 min	250°C, 5 min
Integration and optical packaging technique	manual assembly	manual assembly	automated
Total port count	proposer defined	proposer defined	proposer defined

* Technology demonstrators are satisfied by co-packaging optical I/O with a proxy IC core to generate and receive data streams.

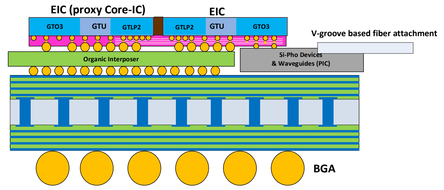
Approach

Heterogeneous Electro-Optical integrated WDM Transceiver can meet both edge bandwidth density as well as power efficiency

- **Electronics (EIC) implemented in TSMC 7nm FinFET for high BW and energy efficiency**
  - **Optical transceiver with drivers & TIAs supporting 53Gb/s NRZ**
  - **Low power parallel interface to FPGA/ASIC core over integrated fan-out (InFO) fine-pitch silicon RDL (GTLP2) @ 13.25Gbp/s**
  - **USR/XSR 112G/56G PAM4/NRZ SerDes for off-chip access (GTU)**
- **16-λ WDM Silicon Photonics (PIC) implemented in GF 45SPCLO process to meet 1Tb/mm edge bandwidth density with V-groove fiber coupling**

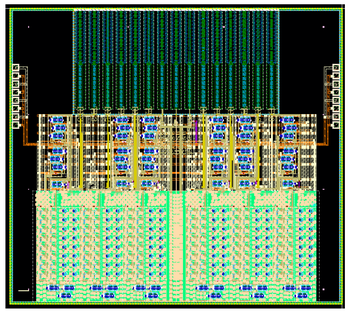


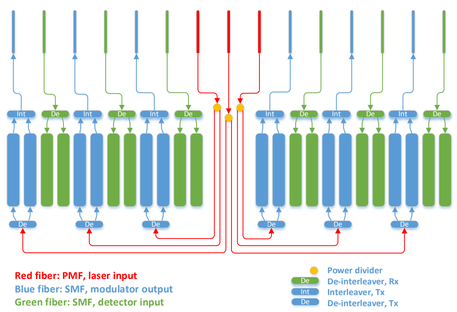
FPGA/ACAP with Co-packaged Optical I/O



10Tb/s MCM Prototype with Proxy Core

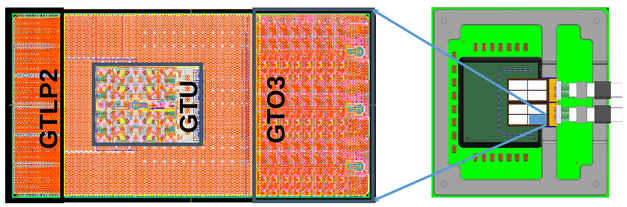
Photonics IC (PIC): 92 53Gb/s channels, 16-λ WDM per fiber with Micro-Ring Modulator (MRM) in TX, MZI based de-interleaver followed by Cascaded Ring Resonator (CRR) de-MUX in RX



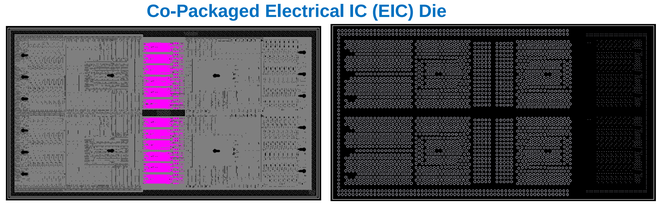


PIC Prototype : 16-λ WDM, 848Gb/s per TX/RX fiber (5Tb/s per PIC, 10Tb/s per MCM)

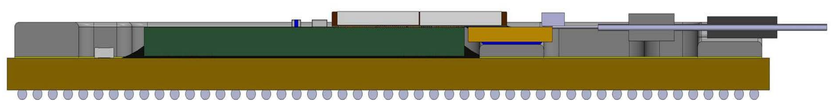
Electrical IC (EIC): 7nm GTO3 Optical Transceiver @53Gb/s & Parallel Link GTLP2 Transceiver @13.25Gb/s over dense Fine Pitch InFO Technology



Co-Packaged Electrical IC (EIC) Die



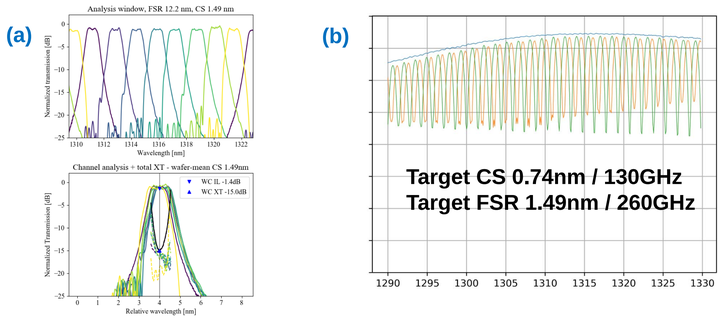
InFO Die (showing C4 bump and Fine Pitched GTLP2 Connectivity)



X-Section of MCM Prototype with EIC & PIC Assembly

Results and Impact

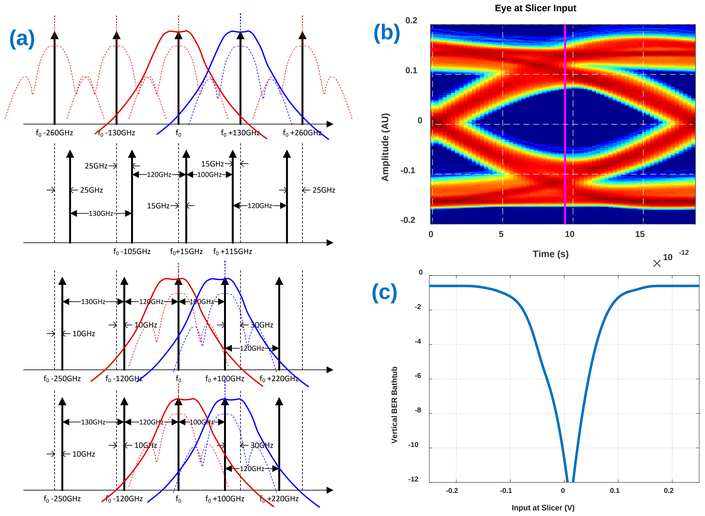
- **First versions of PIC (1.1), EIC, & InFO are currently in fabrication**
- **Heterogeneous co-package integration development is on track.**
- **16-λ DFB laser fabrication and laser assembly is on track.**
- **Preliminary characterization of short-loop PIC 1.1 wafer for Si Pho components shows that designs are within targets.**



Wafer Probe Measurement of (a) 1X8 CRR Filter & (b) Interleaver

End-to-end Electro-Optical WDM Link Performance Modeling, which includes the following:

- **Laser noise (RIN)**
- **Cross-talk with WDM channel wavelength excursion**
- **Optical connector, coupling, and waveguide losses**
- **Modulator frequency response, non-linearity and optical power**
- **Driver/TIA frequency response, including micro-bump parasitic**
- **Electrical Impairments: TX/RX jitter, thermal Noise, supply Noise**



(a) CRR Filter response w/non-uniform channel spacing, (b) RX Eye Diagram at the slicer & corresponding (c) Bit-Error-Rate (BER)

Performance Summary w/Laser (RIN) & Optical Crosstalk with all the Electrical Impairments shows design meets program goals w/ 15% Laser WPE & w/ <2.56pJ/b power efficiency

Optical Crosstalk \ RIN	-135	-140	-145	RIN off
BER – Worst laser spacing	7.94e-10	2.40e-12	1.15e-14	5.01e-15
BER – Regular laser spacing	2.14e-11	2.88e-14	4.90e-16	1.10e-16

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