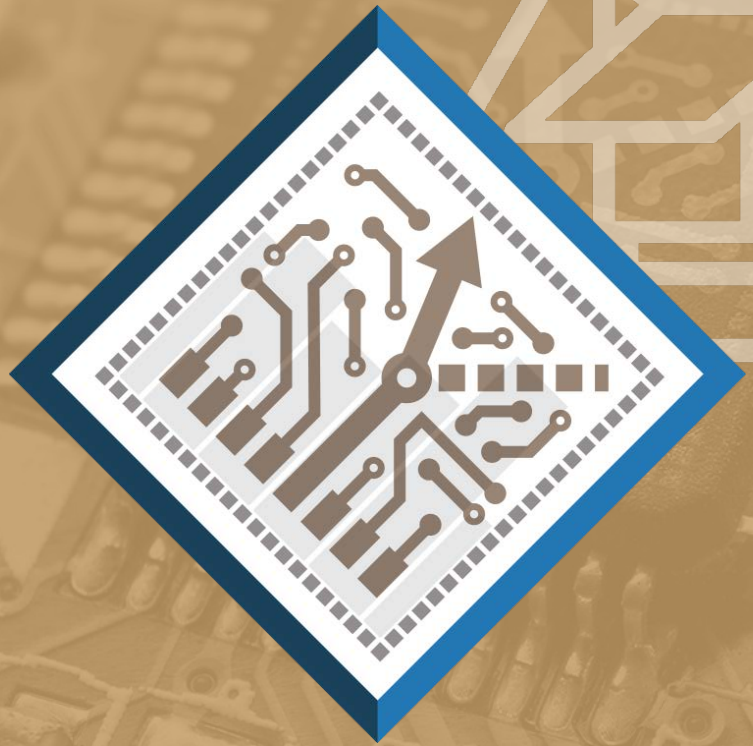
# THE ELECTRONICS RESURGENCE INITIATIVE

# HETEROGENEOUS INTEGRATION FOR RF & MIXED SIGNAL SYSTEMS

| start | end | Company | Presenter | Topic |
|---|---|---|---|---|
| 8:30 | 9:00 | DARPA | Tim Hancock | Review of DARPA Investments |
| 9:00 | 9:30 | Raytheon | Jeff LaRoche | GaN-on-Si |
| 9:30 | 10:00 | Teledyne | Miguel Urteaga | InP BEOL |
| 10:00 | 10:30 | Qorvo | Kevin Anderson | 2.5D/3D for III-Vs |
| 10:30 | 10:45 | Break | | |
| 10:45 | 11:15 | HRL | Florian Herrault | MECA, MECAMIC |
| 11:15 | 11:45 | Micross | Alan Huffman | Interposers, TSVs, bumping |
| 11:45 | 12:30 | Panel | All presenters | |



# HETEROGENEOUS INTEGRATION FOR RF & MIXED SIGNAL SYSTEMS

# Metal-Embedded Chip Assembly (MECA)

## RF IC Manufacturing and Multi-Chip Module Packaging with Integrated Thermal Management

**Florian Herrault, PhD**
**HRL Laboratories, LLC**
**July 17, 2019**

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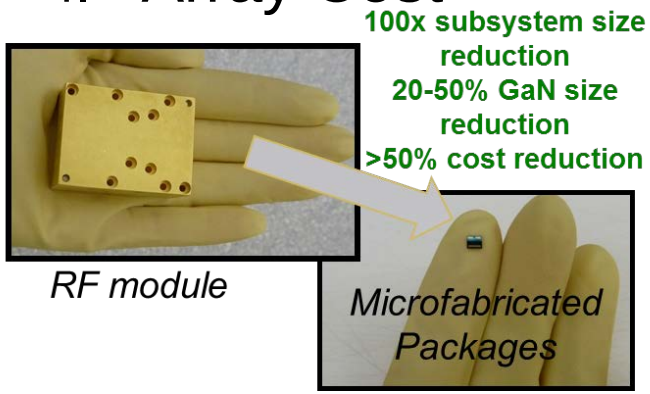
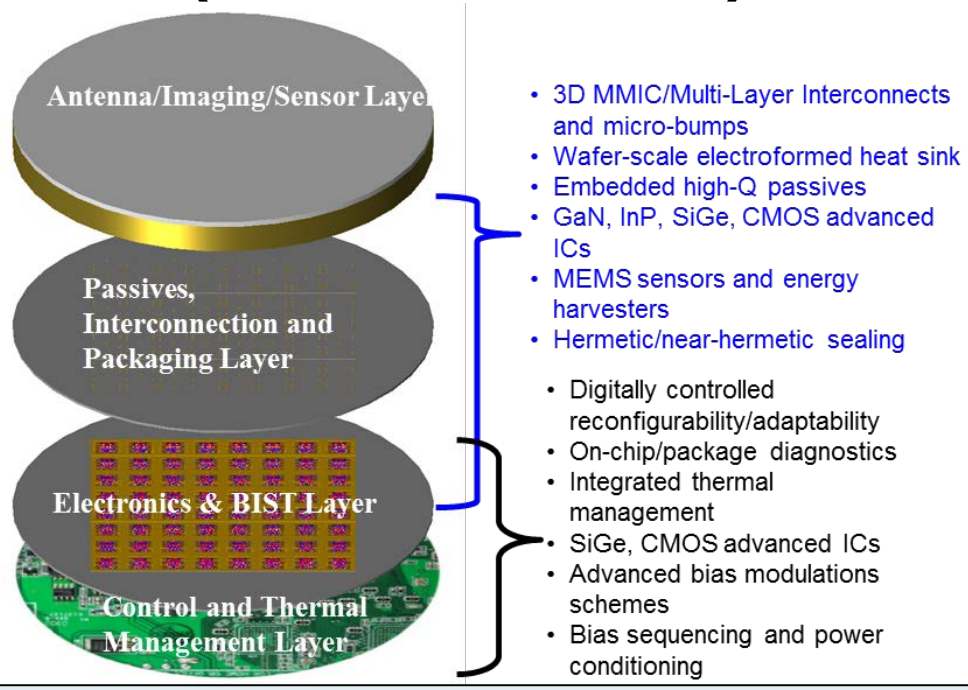
# Opportunities and Challenges of 3D IC

**2.5D and 3D integration** of microelectronic subsystems (e.g., Digital SoC, IR FPA, mmW Phased Arrays, MEMS/CMOS) is considered the **next technology node technology breakthrough beyond Moore's Law (more than Moore).**

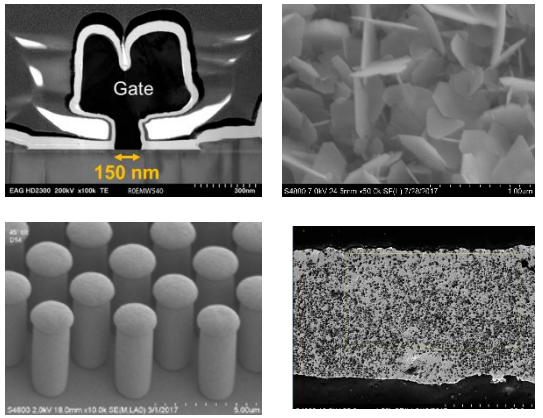
- However, major technical challenges in:
  1. Thermal management
  2. Electrical interface
  3. Wafer-to-wafer design match requirements
  4. Array Cost



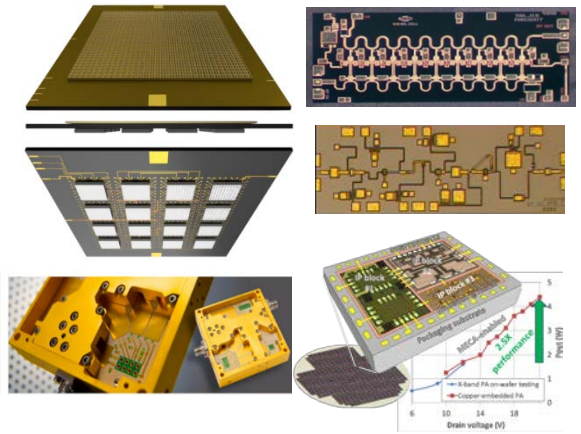

HRL is addressing these challenges by developing key heterogeneous integration technologies for next-generation high-performance subsystems

# HRL's RF and mm-Wave Portfolio



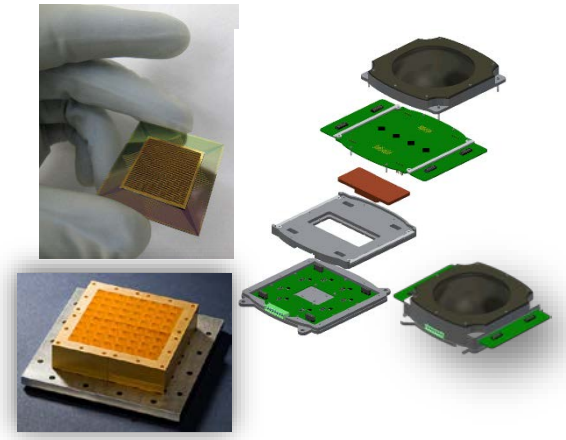

RF GaN transistors, Magnetics, Interconnects, Thermal

***Materials & Devices***



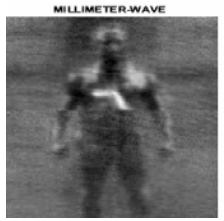
RF MMIC, advanced BEOL, 2.5D & 3D heterogeneous integration

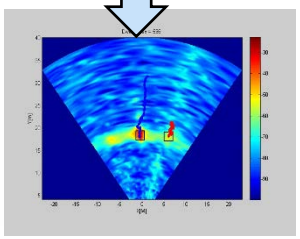
***Circuits & Packaging***



Coded Aperture, Low cost radar, mmW phased arrays

***Signal Processing & Subsystems***





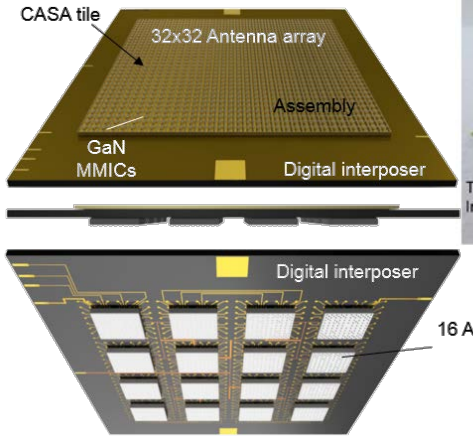
Communications, Radar and EW applications

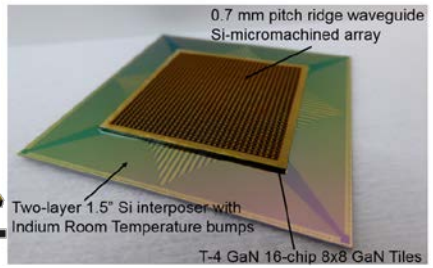
RF/mm-wave Development From Materials to Subsystems

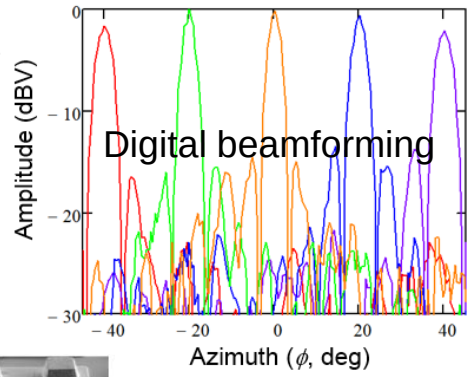
# A Brief Overview of HRL's RF Heterogeneous Integration Capabilities

## 3D-stacked 235GHz Phased Array:

3D wafer / die stacking of micromachined Si antenna array, RF GaN tiles, Dual-sided Si interposer and CMOS ASICs (Demonstrated 1024 element array) – Scalable Tile Architecture




## Interposer fabrication and chiplet assembly:

Interposers with TSVs, RDLs on Si, SiC, Quartz,..

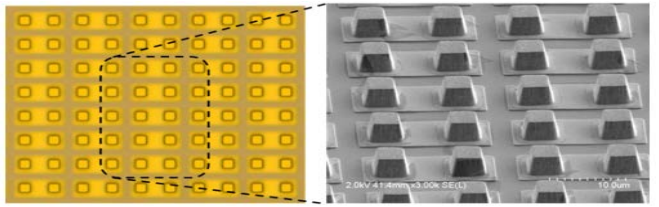
Cu-filled TSV capabilities, Cu CMP,..

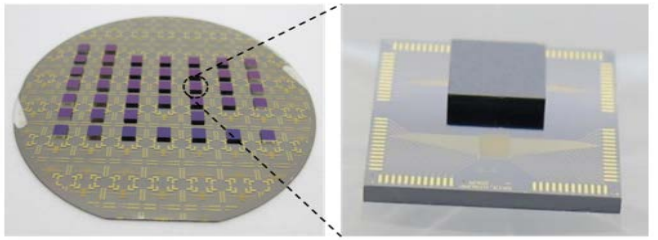
3 um Line and Space multi-layer interconnects

Bumping expertise with Au-Au, In, Sn, Cu pillars, ..

Down to 4 um pitch (Au-Au, In) at high yield

0.5 um flip chip bonding

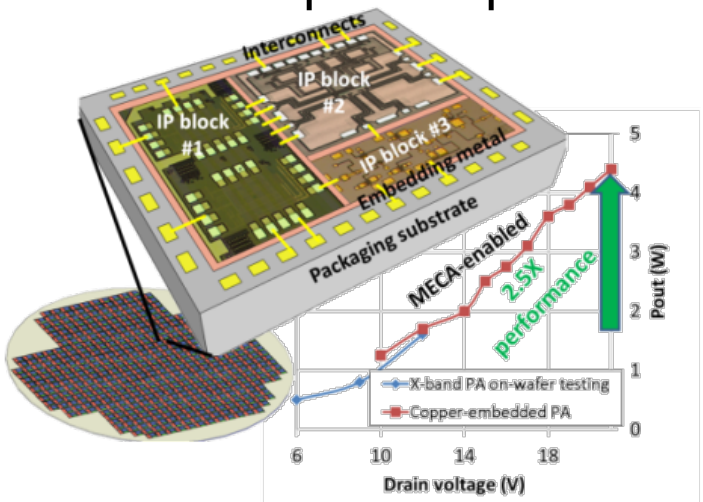


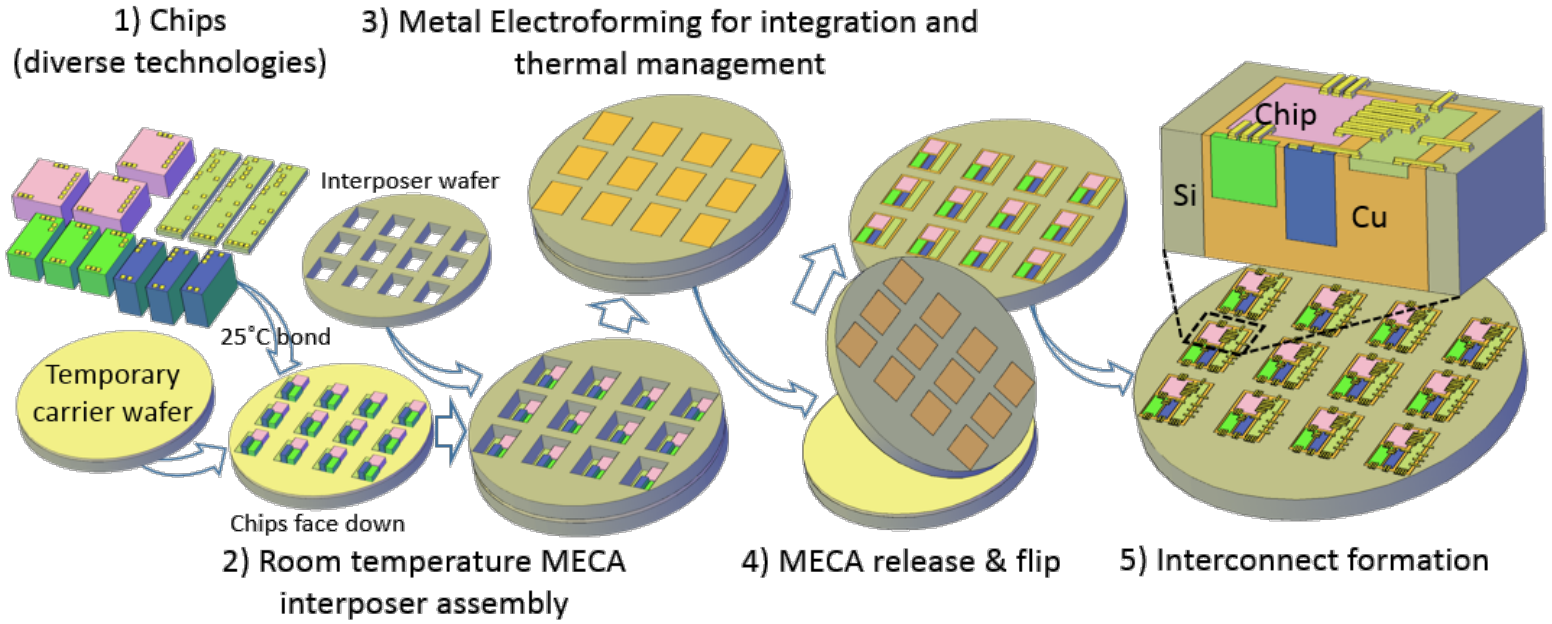


# HRL's MECA Technology for High-Performance Multi-Chip Module Packaging

## HRL's Metal-Embedded Chip Assembly (MECA) technology enables high-density multi-chip 2.5D packaging with fine pitch interconnects

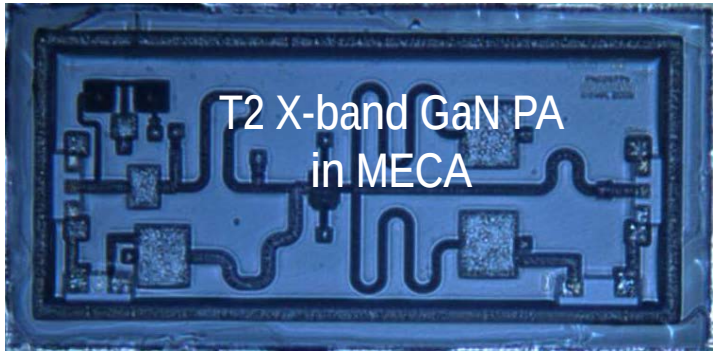
- Die are embedded in metallic heat spreader
- MECA addresses integration AND thermal management
- Low-loss front-side interconnects
- Wafer-level die integration
- COTS and IP re-use compatible
- Reduced chip-to-chip cross talk

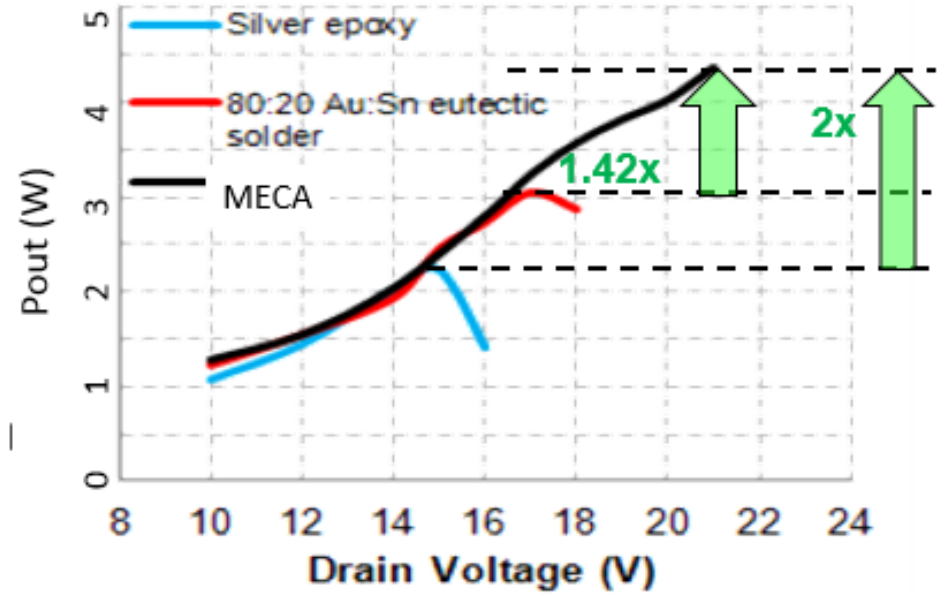


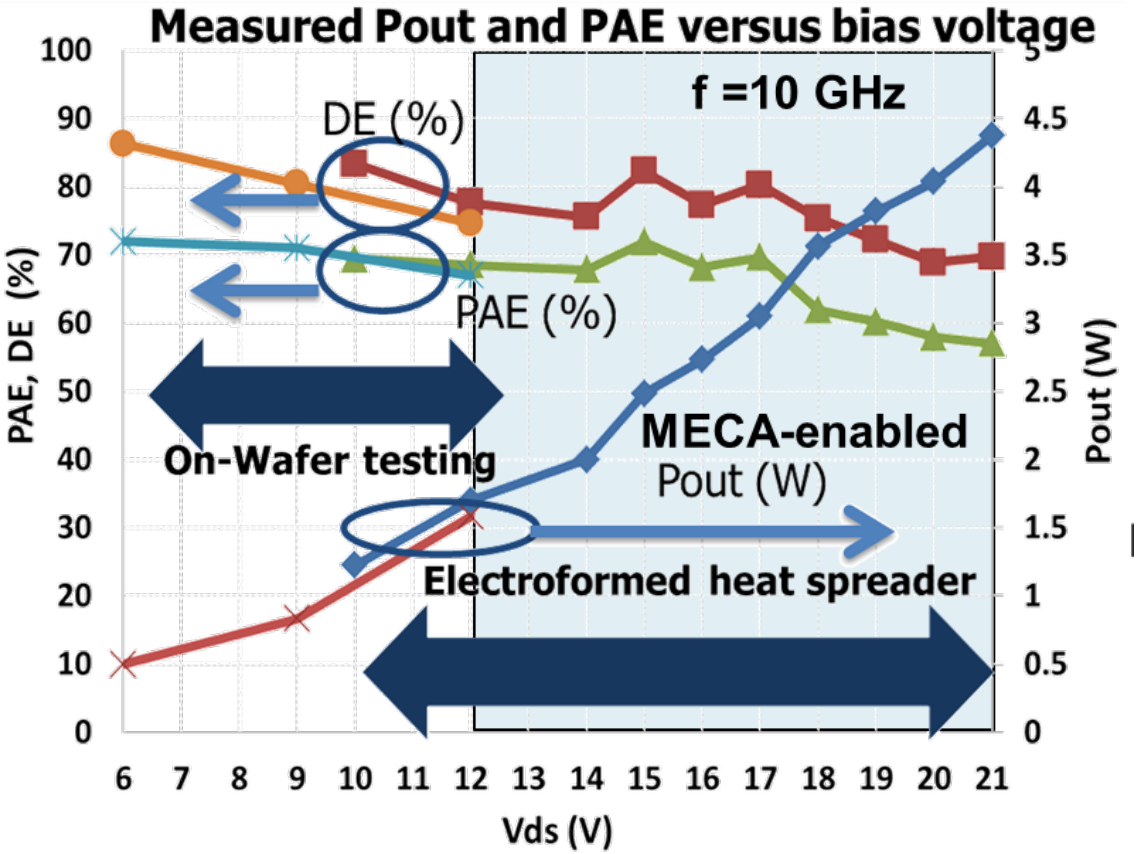

MECA: high-bandwidth integration of diverse microelectronics chips with integrated thermal management

# MECA-Packaged PA Outperforms Conventionally-Packaging Power Amplifiers



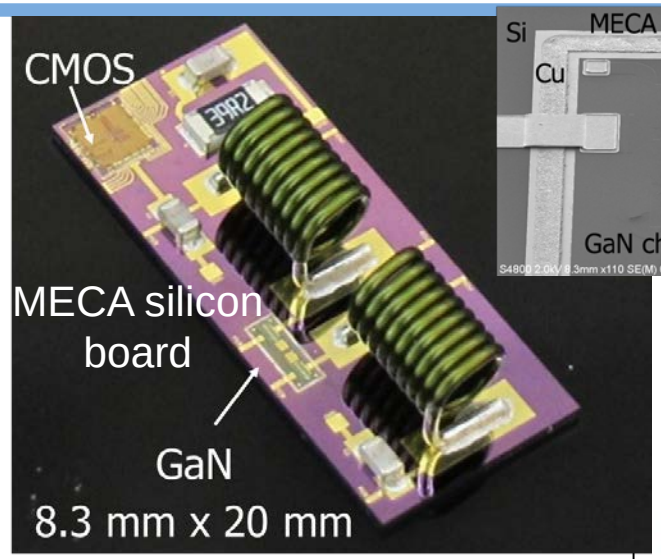




> 40% improvement over solder-attached chip on heat spreader

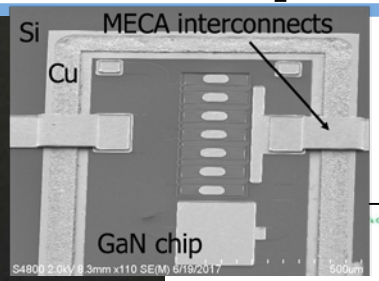


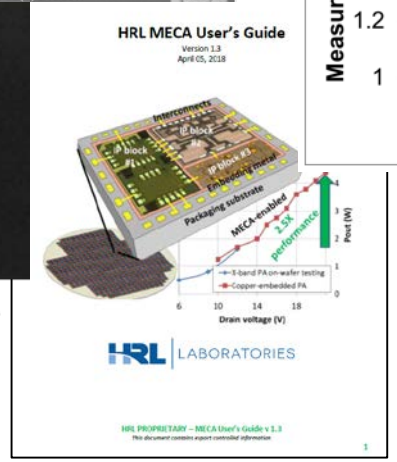

Improved Operational Bandwidth
> 4W, > 60 % PAE at 10 GHz

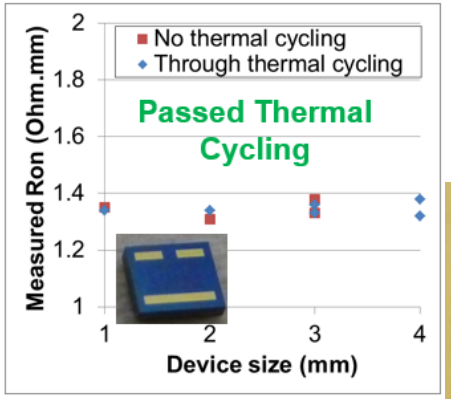
# MECA Spans Multiple Length Scales and Improves Chip Performance



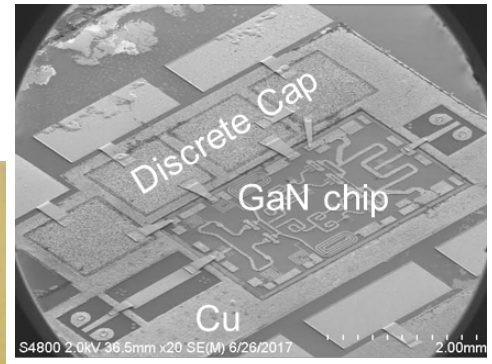

Delivered CMOS/GaN/Passive modules to Maxentric



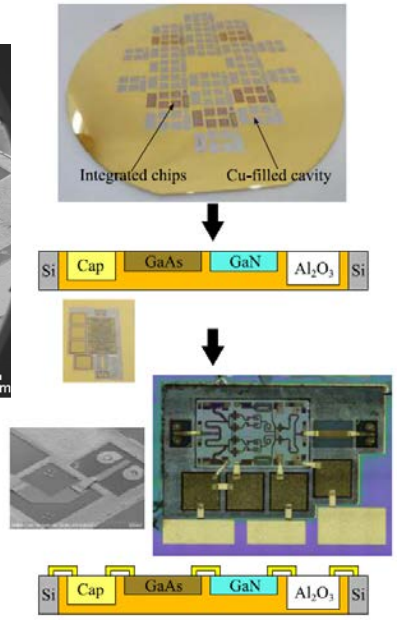



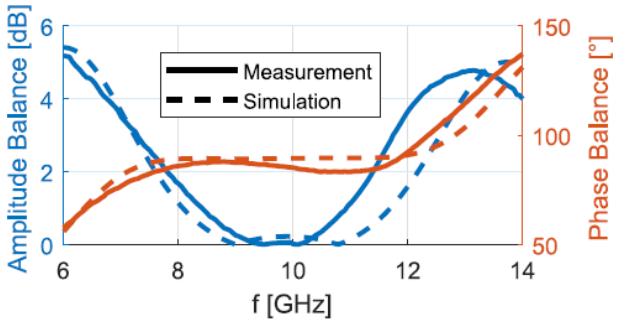

Lange coupler

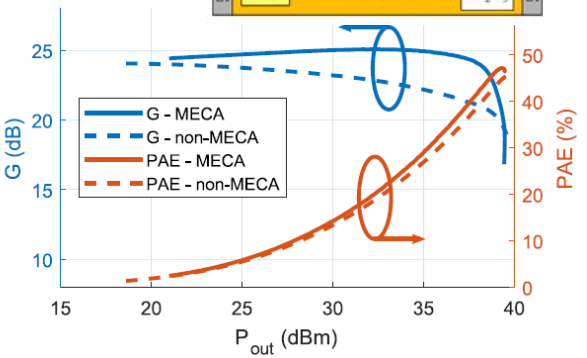



X-band PA module




Delivered modules to UC Boulder




- Design guide
- Integrated GaN, CMOS, GaAs, Alumina, high-k capacitors
- 10 µm L/S MECA interconnects at > 90% yield (intra/inter chips)
- Validated design-to-fab-to-test cycle

MECA compatible with range of chip form factors and materials. Also improves chip performance

# HRL's RF IC Manufacturing Process: "MECAMIC"

MECAMIC uses pre-fabricated Compound Semiconductor (CS) transistor chiplets embedded in low-cost large-scale interposer substrates (e.g., up to 12" silicon) offering advantages of both silicon technology with best high density interconnects and CS technology with best devices


**Compound Semiconductor World**

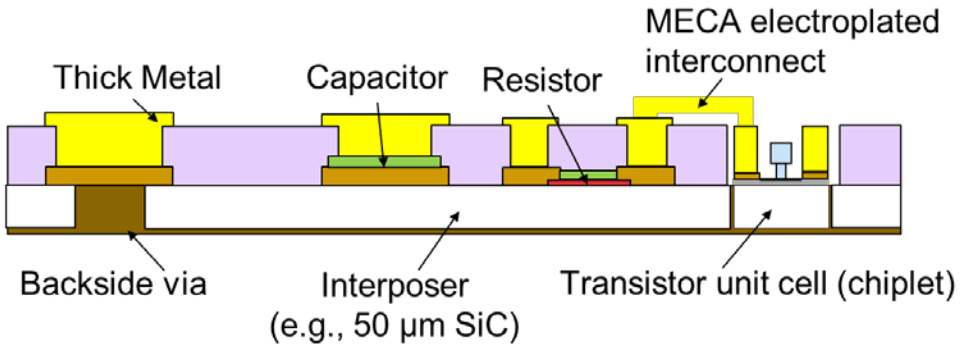
Small wafers but tiny transistor chiplets


**Silicon World**

For low-cost interposer fabrication for passive and interconnects

**HRL MECA-like integration**

High-speed pick and place



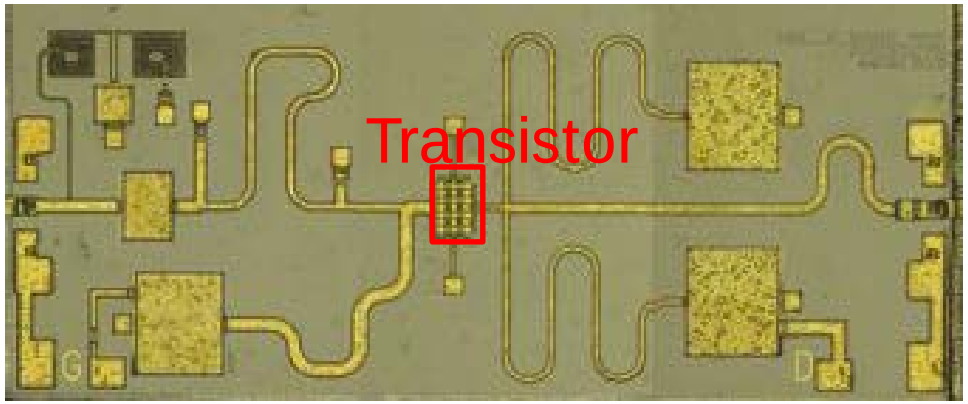

High-performance RF IC at lower cost

Decouples Front-end process from back-end process and makes efficient use of expensive III V material for **low-cost IC manufacturing and rapid maturation of device technology**

# Why is Hybrid Manufacturing a Good Idea for DoD RF ICs?

- **Inefficient use of III-V material**
  - Transistor area for III-V circuits is << 10% of the chip area
  - Passives and interconnects > 90% of area
  - This is true for most RF IC technologies
- **III-V DoD Technology maturation / cycle time**
  - Usually slow qualification and long cycle time
  - Generally uses 2MI / 4MI interconnect processes
- **III-V is expensive**
  - Small wafers (4-6”)
  - Expensive Bill of Materials (substrate, epi, …)
- **III-V is high performance at RF and mm-wave**

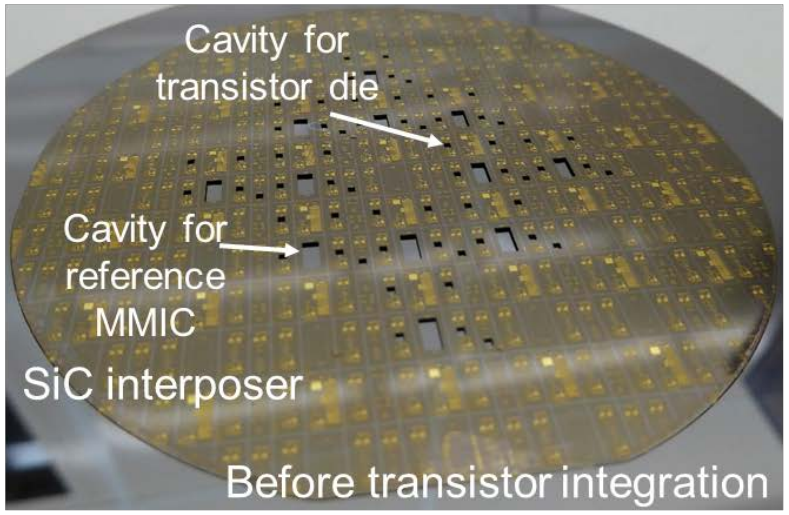
Chip area: 3.7 mm^2
Transistor area: 0.03 mm^2

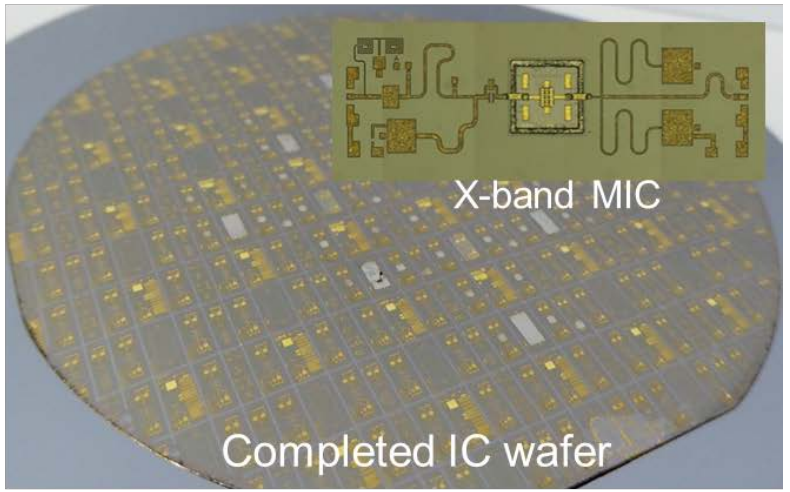



X-band GaN-on-SiC T3 PA (HRL)

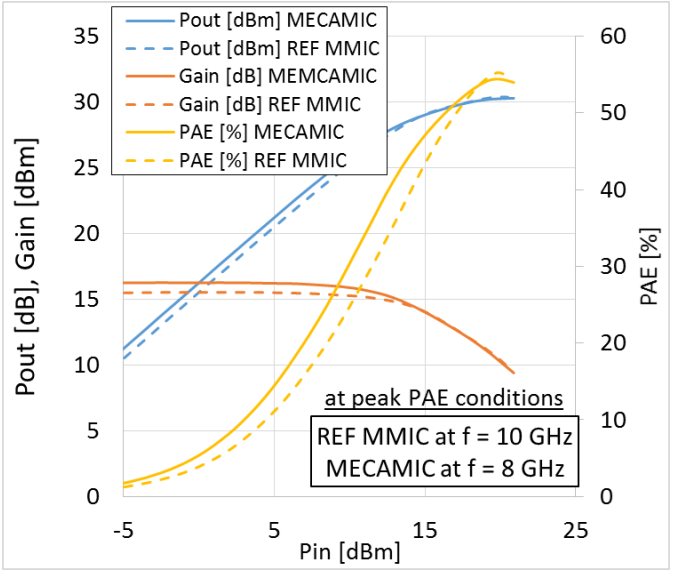
III-V is expensive and less than 1% of RF circuit area is used for devices. 99% is a waste of high-value real estate. **Can hybrid manufacturing techniques change the cost/performance paradigm?**

# MECAMIC Prototyping Demo is a Success




- **> 5X decrease in GaN MMIC cycle time**
- Low cost MMIC run
- 55% peak PAE, 1W Pout at 8 GHz
- **Performed as well as reference MMIC**
- **100% yielded parts**

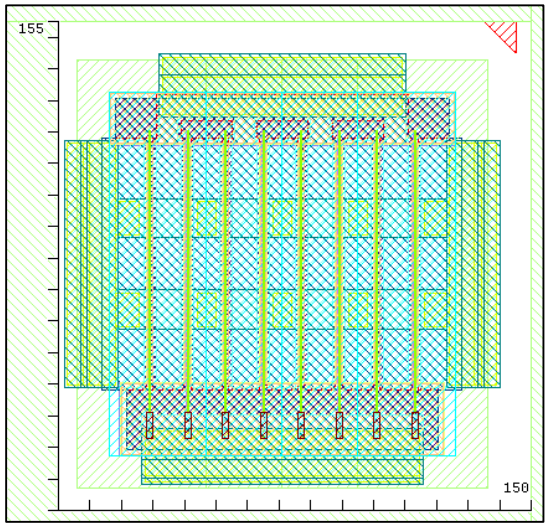


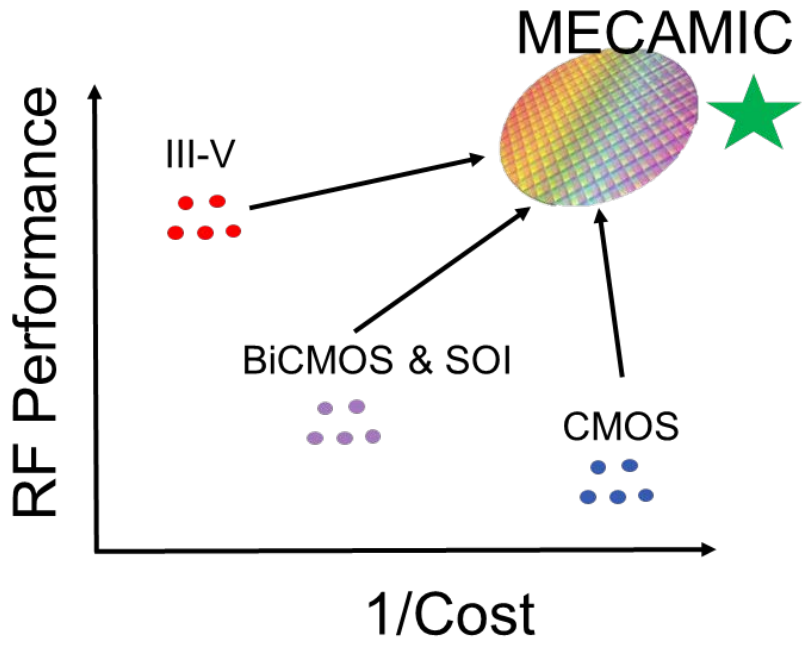

**Metal Embedded Chip Assembly for Microwave Integrated Circuits (MECAMIC)**

# Summary

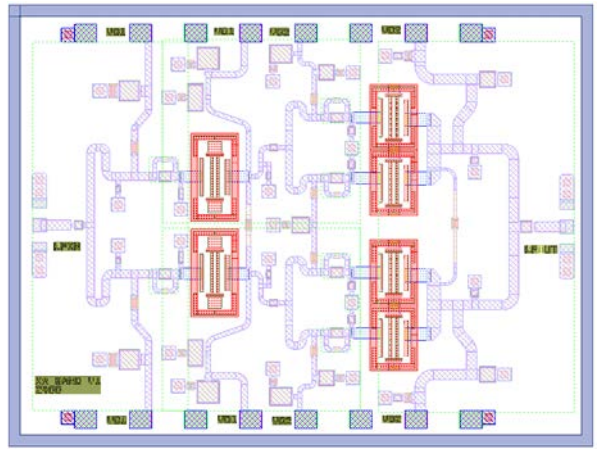
- MECA is a heterogeneous integration platform with embedded thermal management and low loss interconnects
- MECAMIC enables rapid manufacturing of device technologies while maintaining monolithic like performance

**General Purpose GaN chiplets (~150 um / side) >100,000 per wafer**




**Ka-band MECAMIC PA**



| | MMIC | MECAMIC |
|---|---|---|
| Frequency | 31-35 GHz | 31-35 GHz |
| # of stage | 2 | 2 |
| Gain | 16 dB | 15-16 dB |
| $P_{out}$ | 4W | 4W |
| Maximum PAE | 40% | 40% |
| Chip size | 2.5mm x 1.7mm | 2.6mm x 2mm |

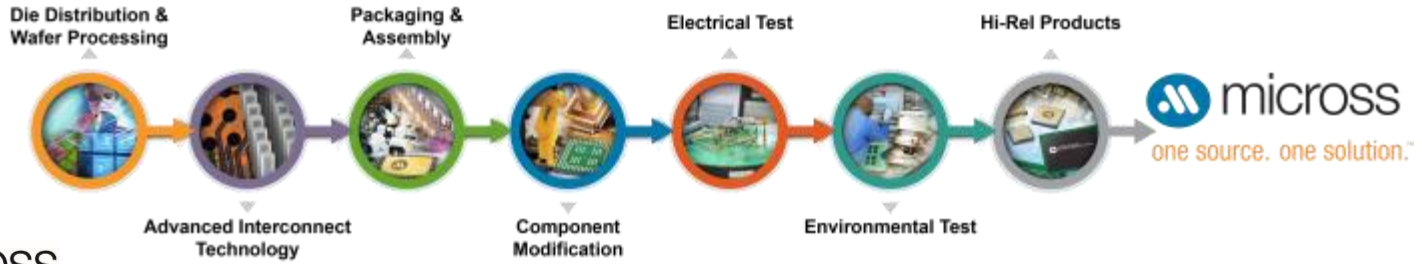

# 2019 ERI Summit: Heterogeneous Integration for RF & Mixed Signal Systems

July 17, 2019

www.micross.com

# Micross Overview

- ***40+*** Years experience serving Aerospace & Defense and Space, Medical and Industrial markets
- ***~ 70%*** of revenue from Aerospace & Defense and Space sectors
- ***400+*** Employees; **>100** STEM Graduates
- **7** Operating Facilities worldwide

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one source. one solution.

# One Source. One Solution.

*Micross supports six value streams; available individually or together as turnkey solutions.*

## Bare Die and Wafers

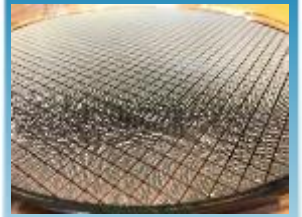
Access to OEM Silicon
30+ Franchised Suppliers

Wafer Processing:
- Saw, Sort & Inspect
- Wafer Probe
- Die Characterization, Qualification, KGD
- Lot Acceptance Test
- EDI

BOM Management:
- Long-Term Die Storage

Orlando, FL | Norwich, UK

## Advanced Interconnect Technology



Advanced Wafer Level Development Prototyping Services & 3D Integration

- Wafer Bumping
- Wafer-level Packaging
- 2.5D & 3D Heterogeneous Integration
- Novel Microfabrication
- CGA Attach

Raleigh, NC

## Packaging and Assembly

Custom solutions for Hi-Reliability Packaging and Modules

- Plastic, Metal, Ceramic
- Flip-Chip & Multi-Chip Module Assembly
- Chip Scale Packaging
- Optoelectronic & Silicon Photonics Assembly

Orlando, FL | Norwich, UK

## Component Modification

Conversion of Finished Devices to required surface finish & footprint

- Lead Attach
- Trim and Form
- BGA (Re)balling,
- Robotic Hot Solder Dipping & Exchange
- Tape & Reel
- 3D Lead Scan
- Counterfeit Mitigation

Hatfield, PA | Clearwater, FL
Crewe, UK

## Electrical Test

Full turnkey space ASIC supply chain management, to include wafer procurement, test, die prep., assembly, package design and qualifications

- Wafer Probe (hot & cold) FPGA, ASIC (28nm), RF (to 10 GHz; PNA-X rated to 67.5 GHz)
- Analytical Services

Milpitas, CA

## Environmental Test

Environmental (Reliability) Testing

- Life Test/Burn-In (ACBI)
- Temp / Power Cycling,
- Temp Humidity Bias, HAST, Fine & Gross Leak
- Thermal and Mechanical Shock & Vibe
- PEM Quals

Milpitas, CA

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one source. one solution.

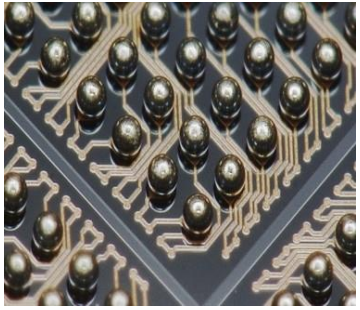
# The Age of Advanced Integration and Interconnect is NOW

- The last decade has seen a decided movement in the semiconductor industry towards advanced packaging and interconnect technologies being implemented to continue the pace of performance improvements that were traditionally provided by CMOS scaling.
  - The entry of major foundries like Intel, TSMC, and Samsung into packaging technologies over the past decade+ is clear evidence of this
- Over the same period of time, the adoption of technologies such as wafer level packaging, flip chip assembly, and silicon interposers has continued to move forward in Aerospace and Defense (A & D) applications, which have unique requirements
  - Lower volumes (compared with commercial electronics sector), high reliability, need for secured/domestic providers, long life cycles
- Forward-looking goals for U.S.-based packaging capability:
  - To support growing volumes as advanced packaging is implemented in more applications
  - Support for multiple device types (digital, RF) and form factors (wafer sizes from 100mm-300mm)
  - To continue to develop and implement new technologies and capabilities
  - To ensure security and trust

# Overview of Key Advanced Packaging and Heterogeneous Integration Technologies

# Bump Interconnect Technologies

- Wafer bumping is a cornerstone technology, providing both electrical and mechanical connections and enabling a compact component outline which is necessary for high density integration
- Flexibility allows use on many different device types (Si, III-V, photonic)
- A & D applications often require Pb-based solder alloys for reliability and legacy device requirements
- Future 300mm wafer demand will mean that multiple wafer format and bumping process options are needed in the long term

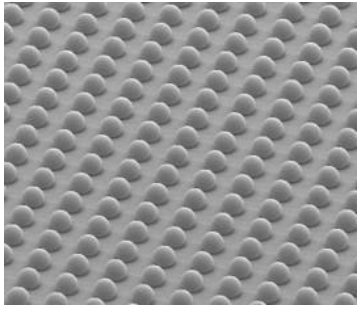


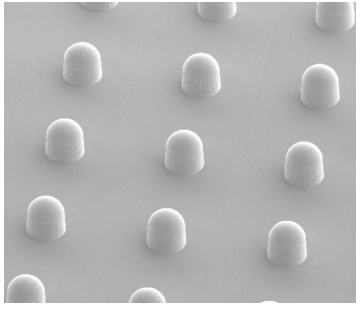
Wafer Level CSP

- ≥ 400µm pitch
- ≥ 250µm bump dia.

Flip Chip

- ≥ 50µm pitch
- ≥ 25µm bump dia.





Cu Pillar

- ≥ 40µm pitch
- ≥ 25µm bump dia.

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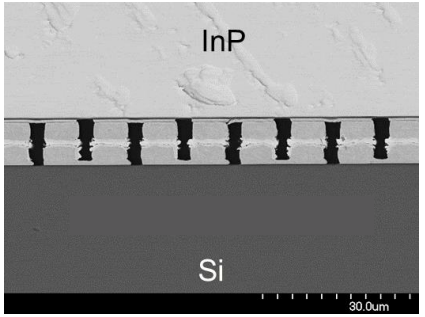
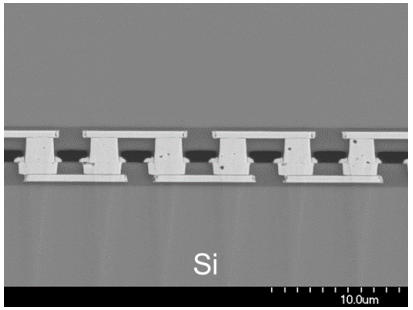
# High Density Interconnect: Microbump Technologies

- Microbump technologies provide extremely high interconnect densities but require thermocompression bonding processes for integration with other devices
  - Use of metallurgies that are non-oxidizing (Au) or enable solid-liquid interdiffusion (SLID) bonding are preferable
  - Thermocompression bonding processes require longer assembly times than collapsible bump assembly

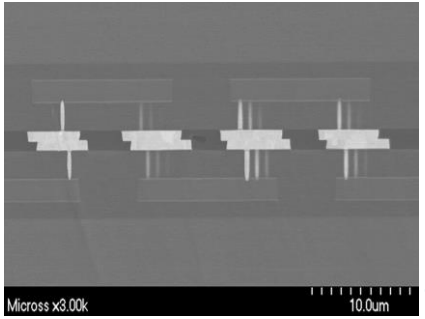
Cu/Sn-Cu Bumps
- ≥ 10µm pitch




Cu-Cu Bumps
- ≥ 5µm pitch

Au Bumps
- ≥ 7µm pitch

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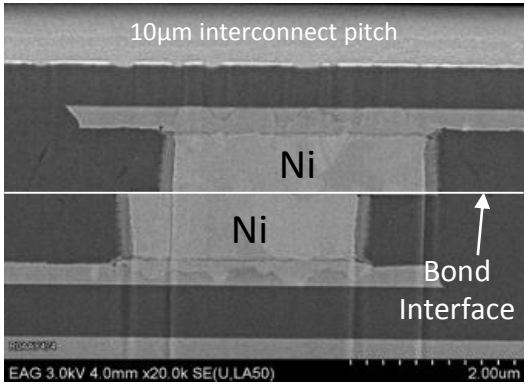
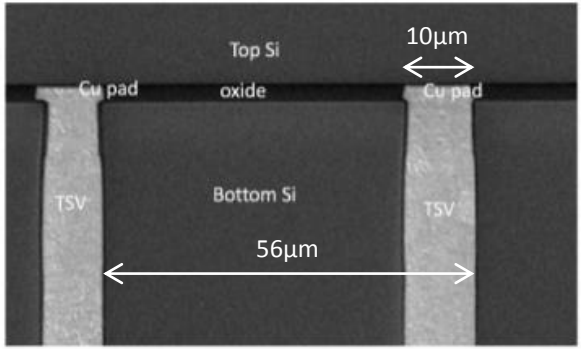
# High Density Interconnect: Direct Bond Interconnect (DBI)

- Originally developed by Ziptronix and now offered through Xperi, DBI started as a wafer-to-wafer bonding technology and is now being demonstrated for die-to-wafer assembly
- Oxide bonding of activated device surfaces provides main mechanical bond between devices. Cu pads provide electrical contacts which are formed after initial oxide bonding
  - Special CMP processes are required to prepare the oxide (Ra < 1nm) and Cu interconnect (slightly recessed below oxide) surfaces for bonding




Wafer-to-Wafer Bond

Image Courtesy: 3DInCites & Ziptronix




Die-to-Wafer Bond

Image Courtesy: Xperi (ECTC 2019)

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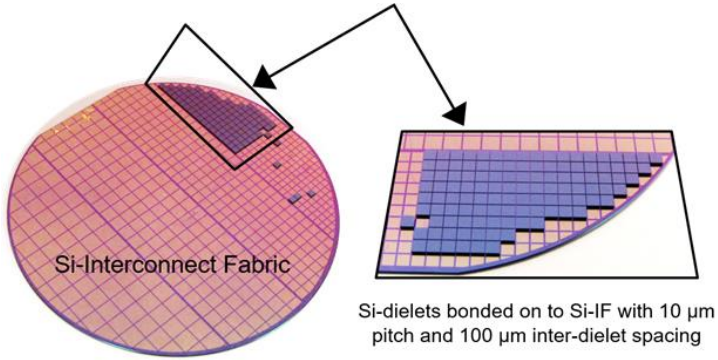
# High Density Interconnect: Silicon Interconnect Fabric

- Developed at UCLA (Subu Iyer's Center for Heterogeneous Integration and Performance Scaling), Si-IF provides a platform for high density integration based on Si wafers with multiple routing layers and thermocompression bonding (Au metal terminals)



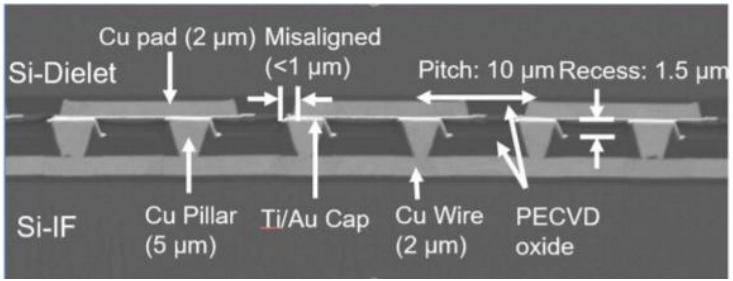




Image Courtesy: UCLA

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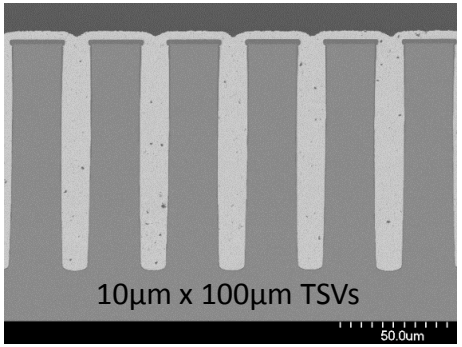
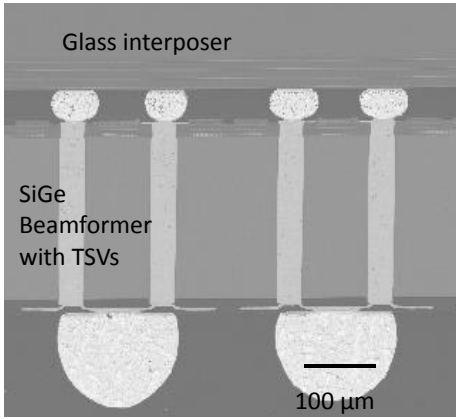
# Through Silicon Via Technologies

- TSVs are a key enabling technology for silicon interposers and 3D integration
- Typical TSV dimensions are in the range of 5-10µm in diameter with depths of 50-100µm (10:1 aspect ratio), typically Cu filled, but poly-Si and W are also used
- Fabrication requires processing of thin wafers through multiple fabrication steps, complicating wafer handling and assembly
- TSV Processes:
  - TSV-First: TSVs are inserted into the wafer prior to or during device fabrication (active device) or routing metal layer deposition (passive device)
  - TSV-Last: TSVs are inserted into the wafer after completion of device fabrication or routing metal layer deposition




TSV First




TSV Last

Heterogeneous 3D Radar Tile-DARPA MFRF

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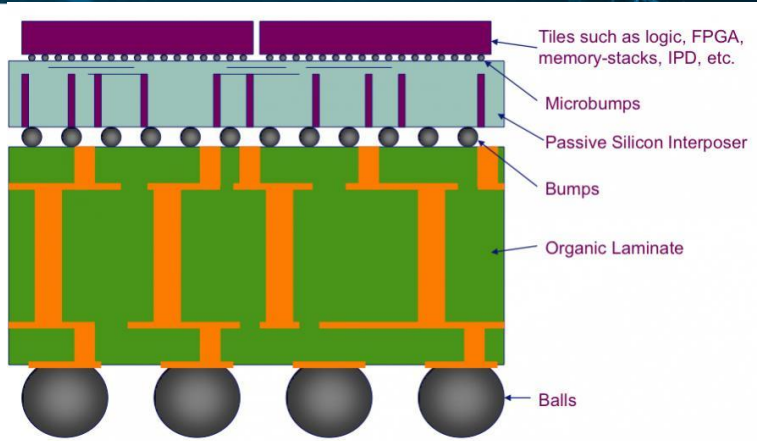
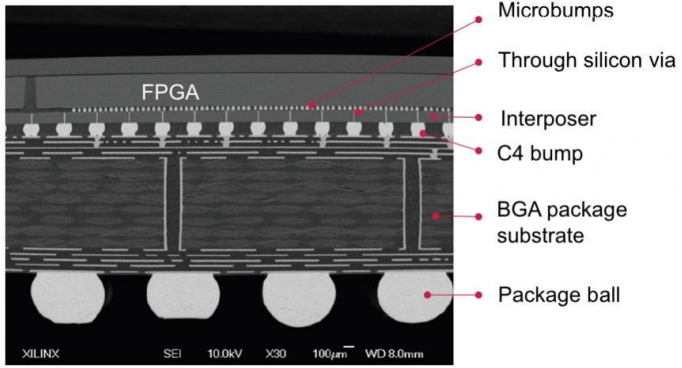
# Silicon Interposers

- Provides high density integration platform for hetero- or homogeneous devices
  - Shorter interconnect lengths (i.e. between memory and logic) increase speed, reduce parasitics, power, and form factor
- Allows for systems to be partitioned into discrete device fabricated in disparate technologies, functionality optimization and cost reduction from use of different technology nodes
- Silicon CTE matching reduces CPI forces applied to devices, allowing for high off chip interconnect density




Images Courtesy: Paul McLellan (SemiWiki)

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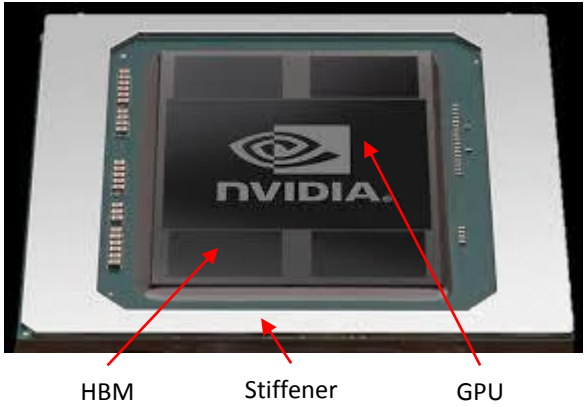
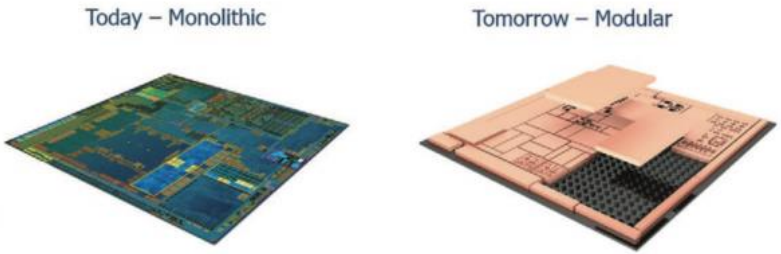
# Silicon Interposers

- Silicon interposers are now key components in heterogeneous integration where partitioned device circuits (chiplets) are integrated together
  - High-end processing and graphics units
  - DARPA Common Heterogeneous Integration and IP Reuse Strategies (CHIPS)
- Domestic production capability is currently limited; availability for A & D applications largely through non-foundry providers with unique process capabilities to support low volume requirements
- Passive interposer fabrication by large foundries is typically TSV-First but limited to major commercial customers
- Domestic interposer supply is typically available through program partnerships that bring front-end MLM processes together with TSV-Last capabilities
  - This can be done for both passive and active interposers

Image Courtesy: NVIDIA



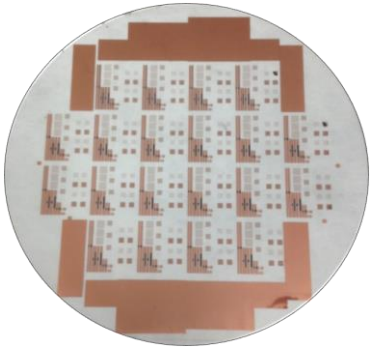



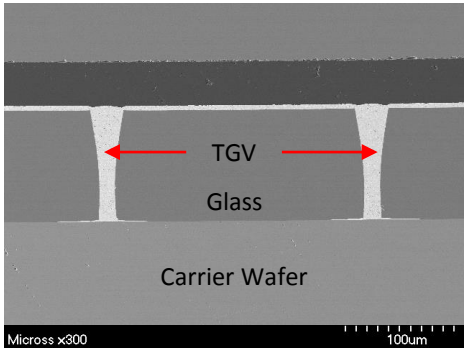

The DARPA CHIPS Concept

Image Courtesy: DARPA

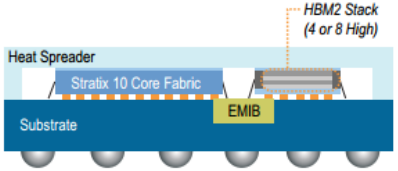
# Silicon Interposer Alternatives

- Glass Interposers
  - Provide better RF performance than Si, but via formation is more difficult, requiring ablative technologies to form via holes
  - TSV filling can be done similarly to Si interposer (electroplating) or with paste filling processes
- Intel Embedded Multi-die Interconnect Bridge (EMIB)
  - Organic-based technology utilizes passive “bridge” chips embedded in the substrate to provide high density interconnection between neighboring devices






MOSAIC microsystems



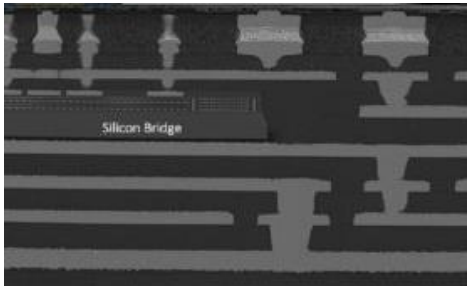




Image Courtesy: Intel

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# Summary

- Domestic A & D companies are increasingly turning to advanced packaging and heterogeneous integration technologies in multiple leading edge applications (radar, communications, data processing, etc.)
- Limited number of on-shore companies with multiple leading edge packaging and integration technology capabilities
  - Economic barriers to accessing full technology capabilities of large globally-oriented companies
  - Smaller U.S.-based companies can meet requirements for security and trust; increasing volume requirements and ability to offer multiple integration technologies under one roof are challenges for the future
- We are now at the point where determining how to fund and implement supply chain solutions for domestic project needs is critical


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