

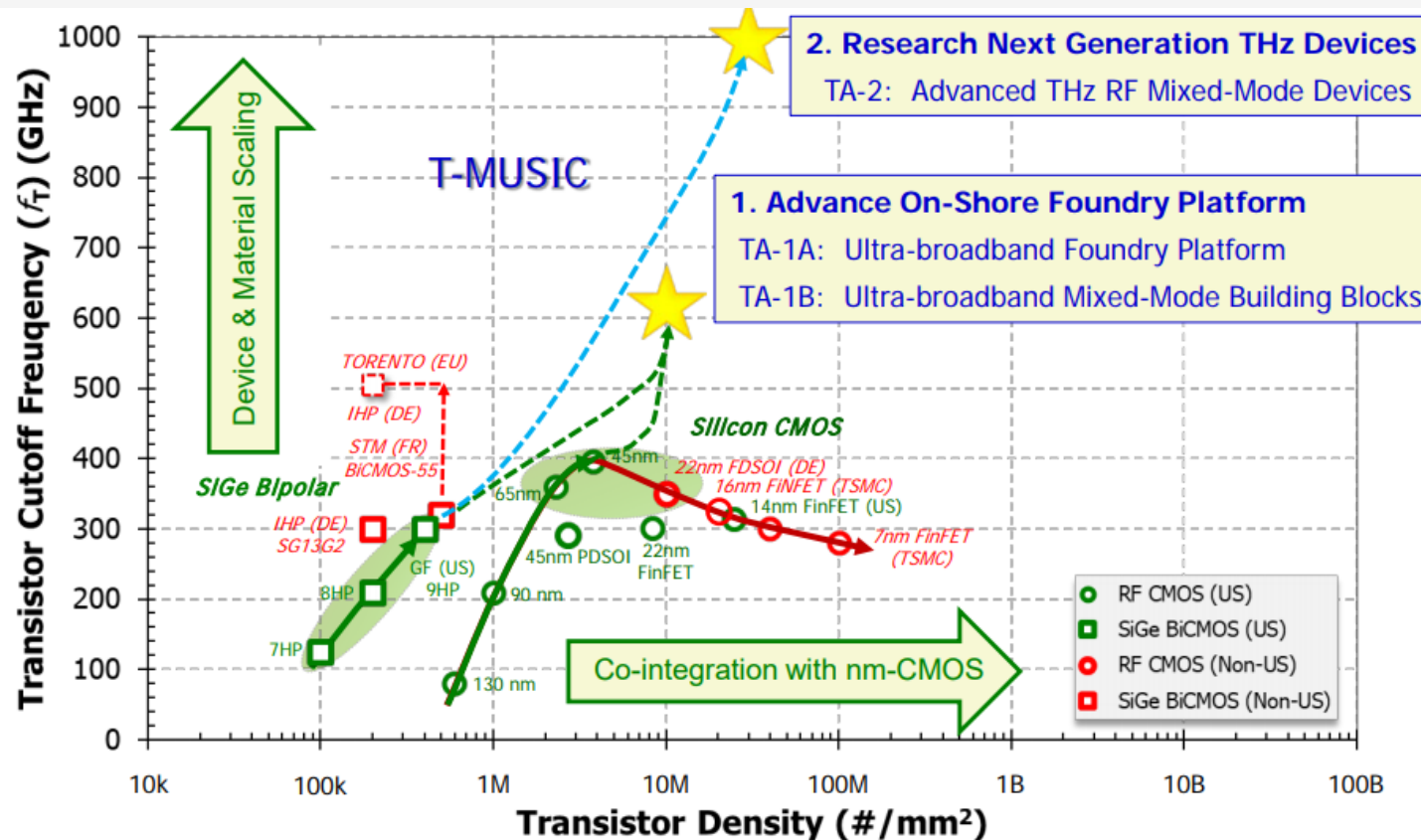
Figure 1 shows a cross-sectional TEM image of the device structure. The image displays a central gate stack with a width labeled $L_g = 50 \text{ nm}$. The gate stack is composed of a TiN layer, a TiAlO_2 layer with a thickness of 2.5 nm , and a Tsi layer with a thickness of 10 nm . Below the gate stack, the T_{ILD} layer has a thickness of 23 nm . The Tsi layer at the bottom has a thickness of 10 nm . Red stars mark the top and bottom surfaces of the gate stack and the Tsi layer.

3D Heterogeneous Integration

DISTRIBUTION A. Approved for public release: distribution unlimited.

TECHNOLOGIES FOR MIXED-MODE ULTRA SCALED INTEGRATED CIRCUITS (T-MUSIC)

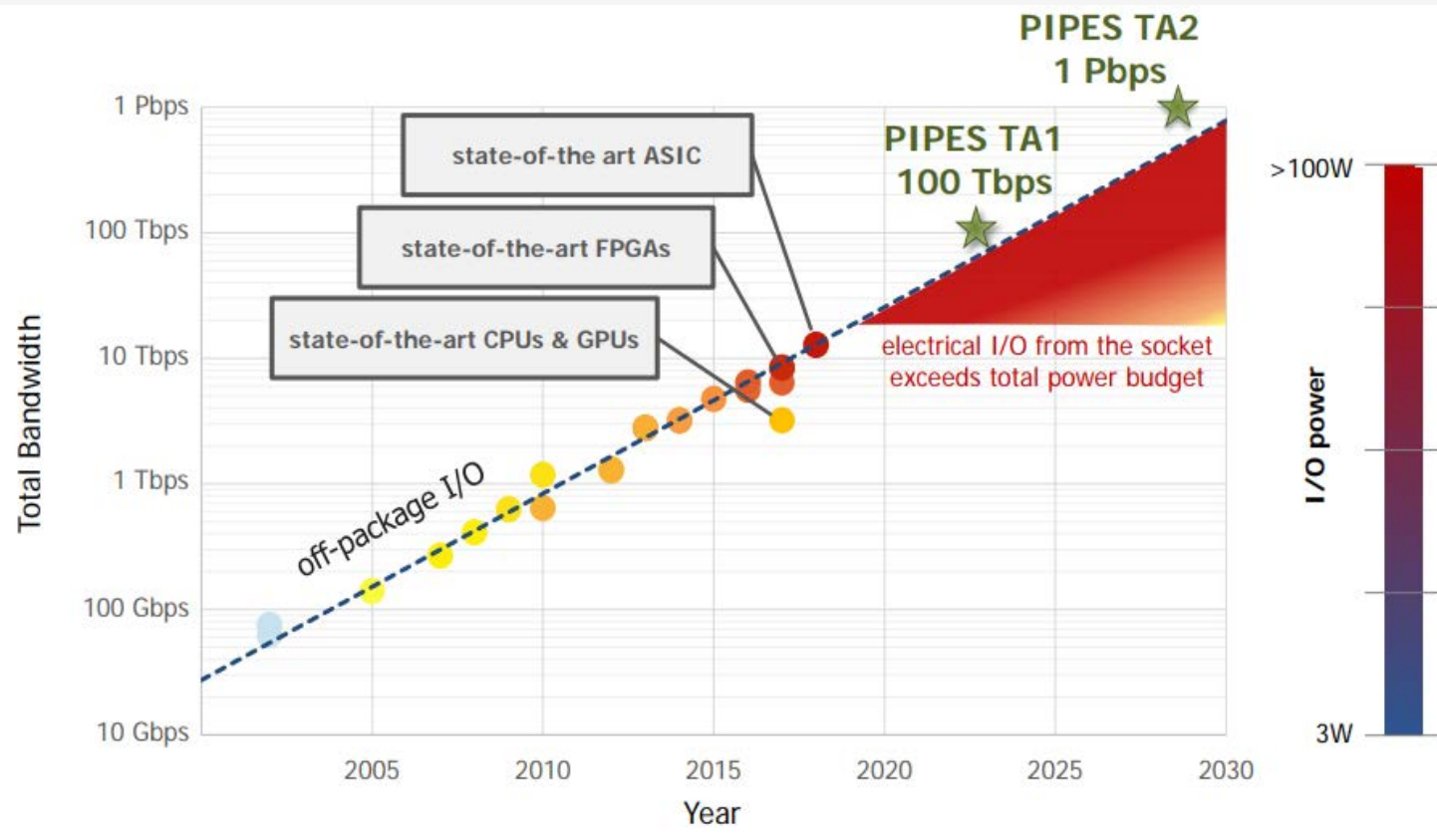
DR. YOUNG-KAI CHEN



- Develop on-shore wafer-scale ultra broadband mixed-mode technologies based on a digital CMOS foundry platform
- Develop next generation THz transistors beyond today's Moore's Law scaling
- Enable disruptive DoD systems with 10x improvement in the bandwidth, dynamic range and operational frequencies of RF analog electronics

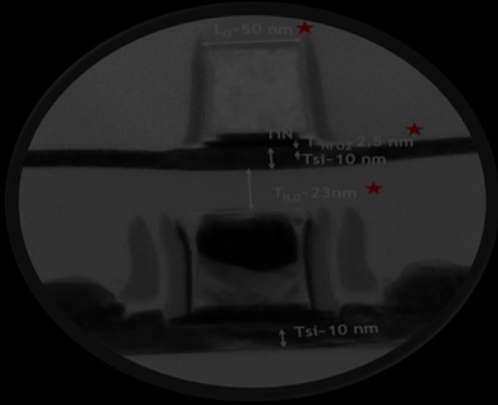
PHOTONICS IN THE PACKAGE FOR EXTREME SCALABILITY (PIPES)

DR. GORDON KEELER

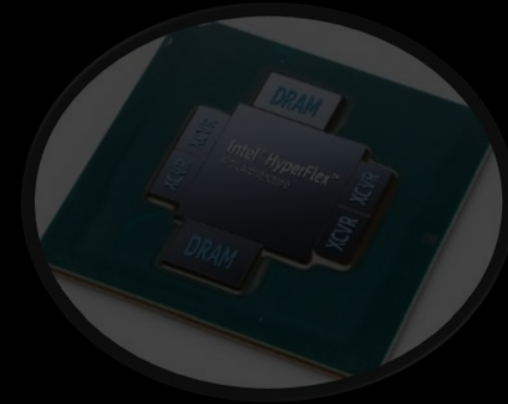


- Remove data locality as a design bottleneck, extending socket-level I/O performance system-wide
- Enable disruptive system scalability through embedded photonic I/O to increase bandwidth, reduce I/O power, and extend reach
- Establish a DoD-accessible ecosystem for photonically-enabled 2.5D microelectronics

JUMP
FRANC
T-MUSIC

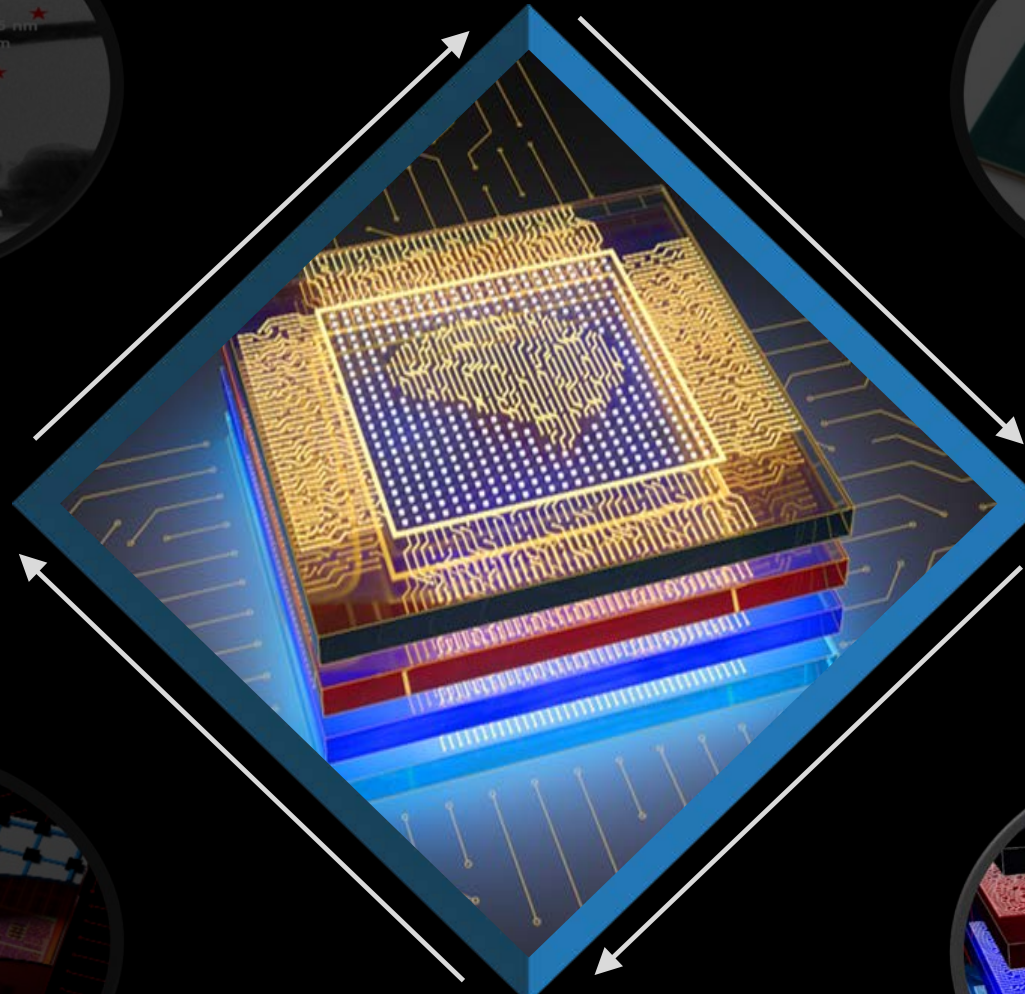


Specialized
Functions



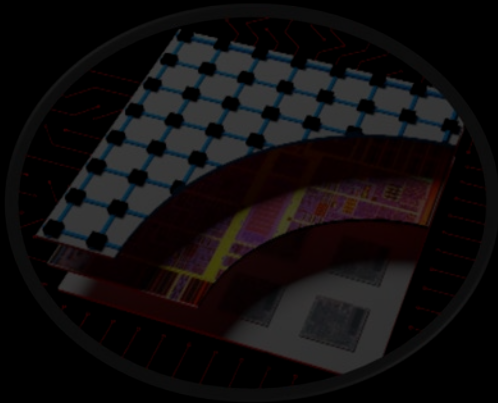
HIVE
L2M
N-ZERO
DSSoC
SDH
DRBE
RTML

New Materials
& Devices

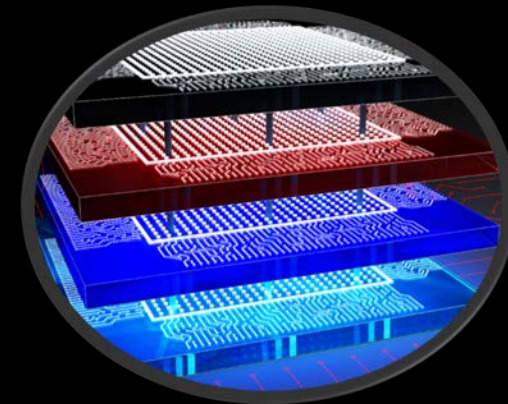


Design &
Security

MIDAS
CHIPS
3DSoC
PIPES



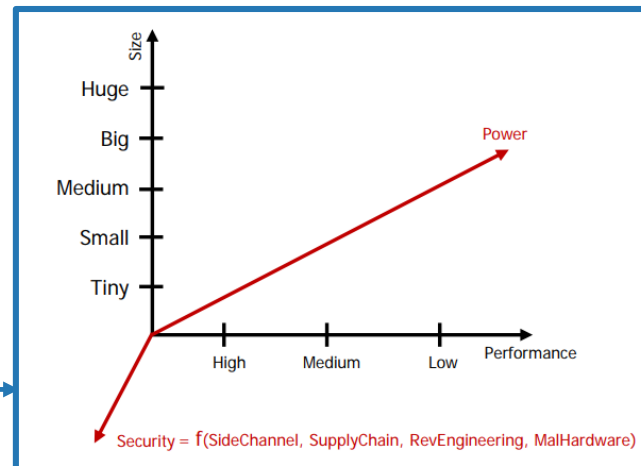
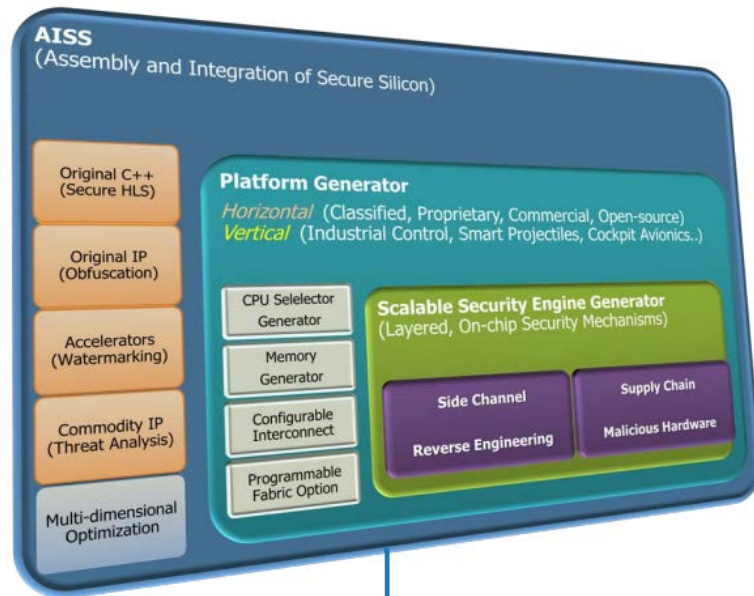
3D Heterogeneous
Integration



CRAFT
SSITH
IDEA
POSH
AISS
GAPS

AUTOMATIC IMPLEMENTATION OF SECURE SILICON (AISS)

MR. SERGE LEEF



- Automate inclusion of scalable defense mechanisms into chip designs to enable security vs. economics optimization
- Enable semi-automated and automatic approaches to assembly and integration that can substantially improve design productivity

GUARANTEED ARCHITECTURES FOR PHYSICAL SECURITY (GAPS)

MR. WALTER WEISS

w/o GAPS

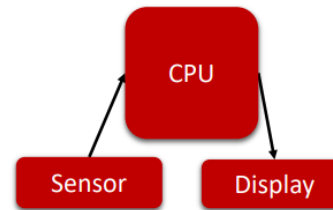
C

```
//Notional sensitive data
#include <stdio.h>
int main() {
    int myInt, mySensitiveInt, result;
    mySensitiveInt = 42;
    scanf("%d", &myInt);
    result = myInt + mySensitiveInt;
    printf("%d", result);
    return 0;
}
```

ASM

```
main:
    ...
    movl 0x2a, eax
    call scanf
    mov -0x04(ebp), edx
    add edx, eax
    mov eax, -x10(ebp)
    call printf
    ...
```

Board Level

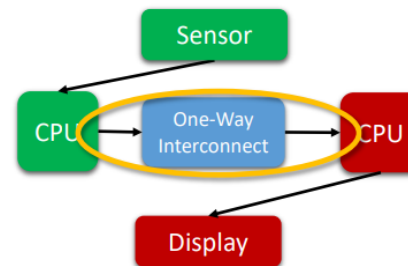


w/ GAPS

```
//Notional multi-level data
#include <stdio.h>
#include <gaps.h>
int main() {
    int myInt, result;
    #classify
    int mySensitiveInt = 42;
    #nclassify
    scanf("%d", &myInt);
    result = myInt + mySensitiveInt;
    printf("%d\n", result);
    return 0;
}
```

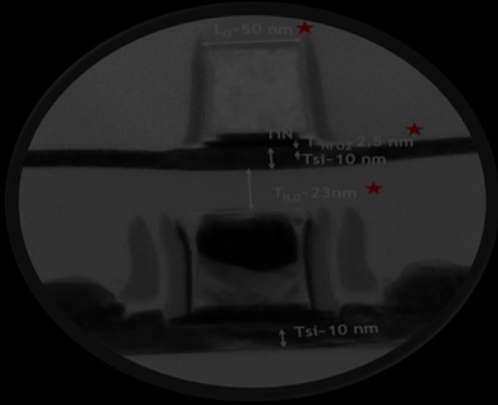
```
main:
    call scanf
    mov -0x04(ebp), eax
    call gapsGlueTransmit
    ret
```

```
main:
    movl 0x2a, ebx
    call gapsGlueReceive
    add eax, ebx
    mov ebx, -0x10(ebp)
    call printf
    ...
```

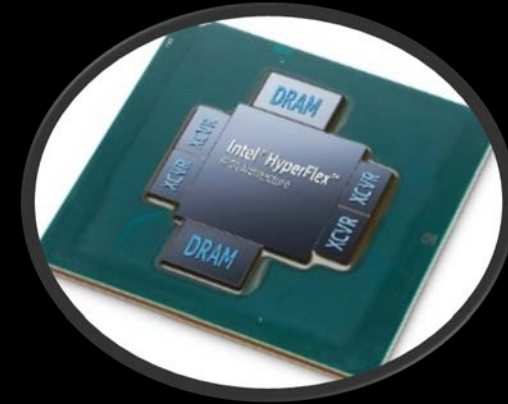


- Develop hardware and software architectures with provable security interfaces to physically isolate high risk transactions
- Enable physical seclusion for security and privacy in a digital age

JUMP
FRANC
T-MUSIC

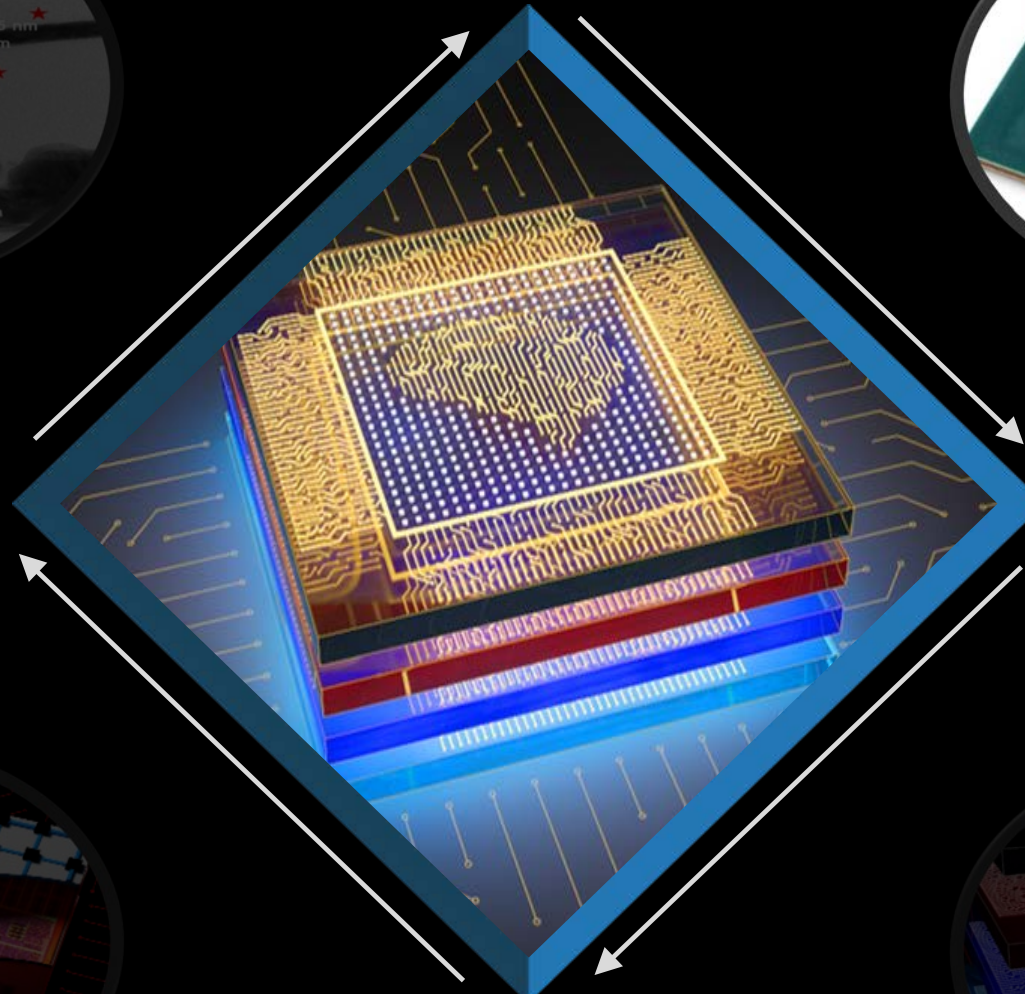


Specialized
Functions



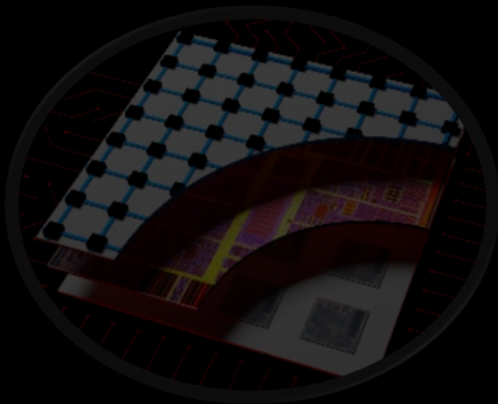
HIVE
L2M
N-ZERO
DSSoC
SDH
DRBE
RTML

New Materials
& Devices

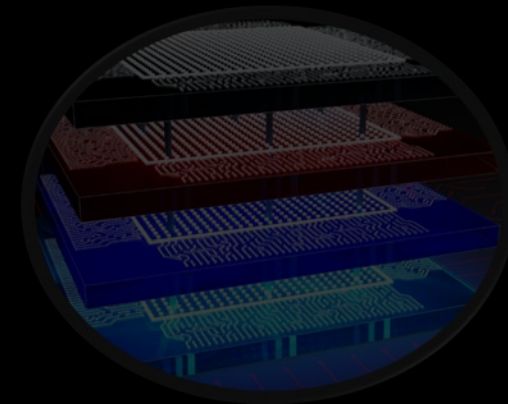


Design &
Security

MIDAS
CHIPS
3DSoC
PIPES



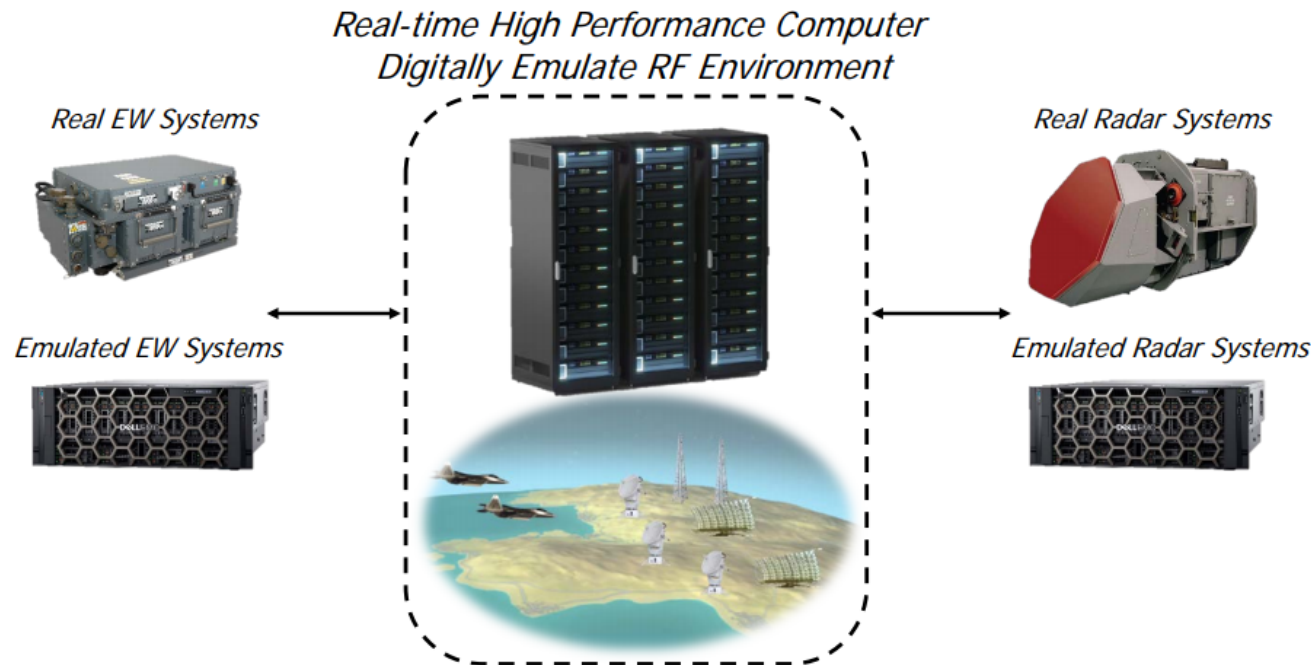
3D Heterogeneous
Integration



CRAFT
SSITH
IDEA
POSH
AISS
GAPS

DIGITAL RF BATTLESPACE EMULATOR (DRBE)

MR. PAUL TILGHMAN



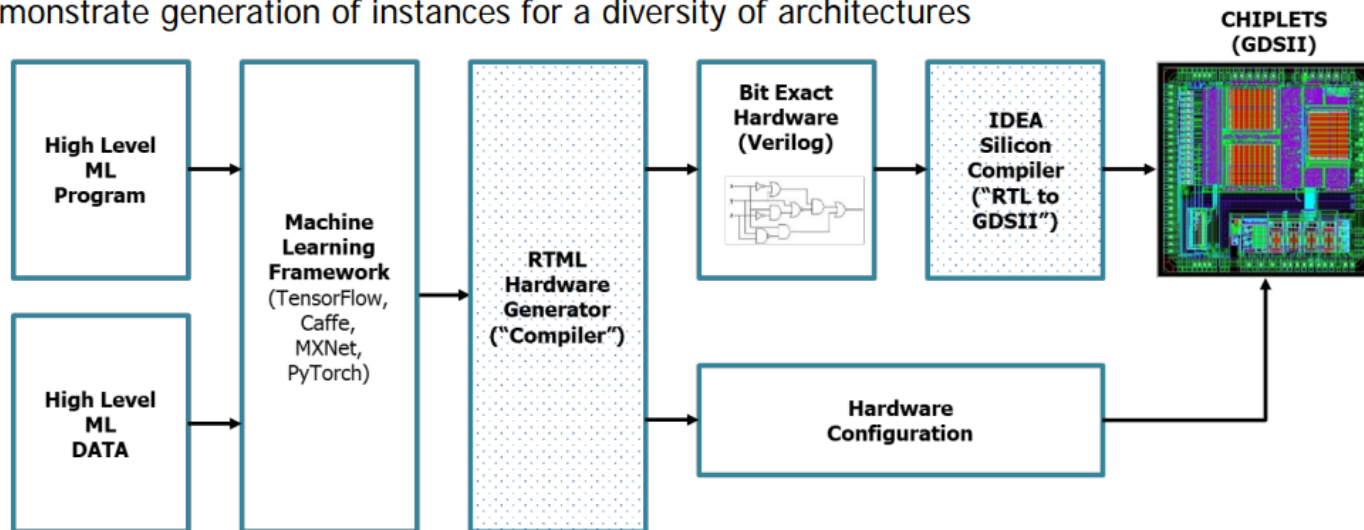
DRBE will allow real EW and radar systems to be interact in real-time on a completely virtual test range.

- Explore new and novel computing architectures, technologies, and methodologies necessary to achieve both low latency and high throughput computation
- Assemble an “array” of these novel computing devices into an HPC
- Integrate the HPC into a tool-suite and architecture which emulates the RF spectrum with high fidelity

REAL TIME MACHINE LEARNING (RTML)

MR. ANDREAS OLOFSSON


Demonstrate generation of instances for a diversity of architectures



- Create no-human-in-the-loop hardware generators and compilers to enable fully automated creation of ML ASICs from high level source code
- Support diverse ML architectures including convolutional neural networks, recurrent networks spike time-dependent neural nets, unsupervised learning, etc.

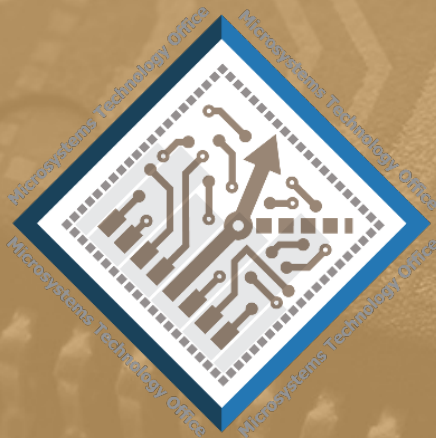
$L_G = 50 \text{ nm}$
 $T_{TiN} = 2.5 \text{ nm}$
 $T_{TiSi} = 10 \text{ nm}$
 $T_{TiSi} = 10 \text{ nm}$
 $T_{TiN} = 23 \text{ nm}$

3D Heterogeneous Integration



A close-up photograph of an Intel HyperFlex SSD module. The module is a dark, rectangular component with a green printed circuit board (PCB) visible around its edges. It features several labels: "Intel HyperFlex" and "3D NAND" in the center, and "DRAM" on two smaller components at the top and bottom. The module is mounted on a larger green PCB, and a yellow arrow points to it from the left.

DISTRIBUTION A. Approved for public release: distribution unlimited.



ERI ELECTRONICS RESURGENCE INITIATIVE

S U M M I T

2019 | Detroit, MI | **July 15 - 17**