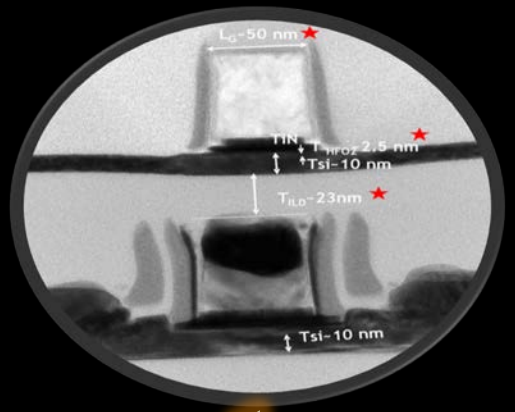
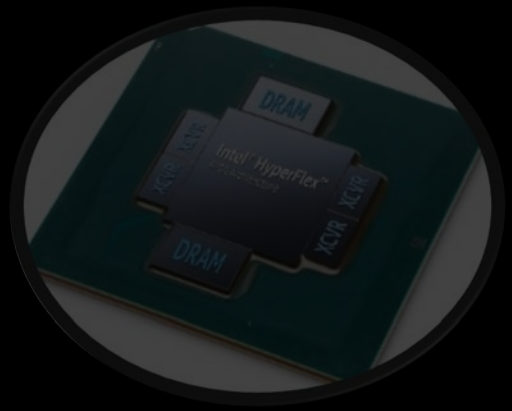
JUMP
FRANC
T-MUSIC

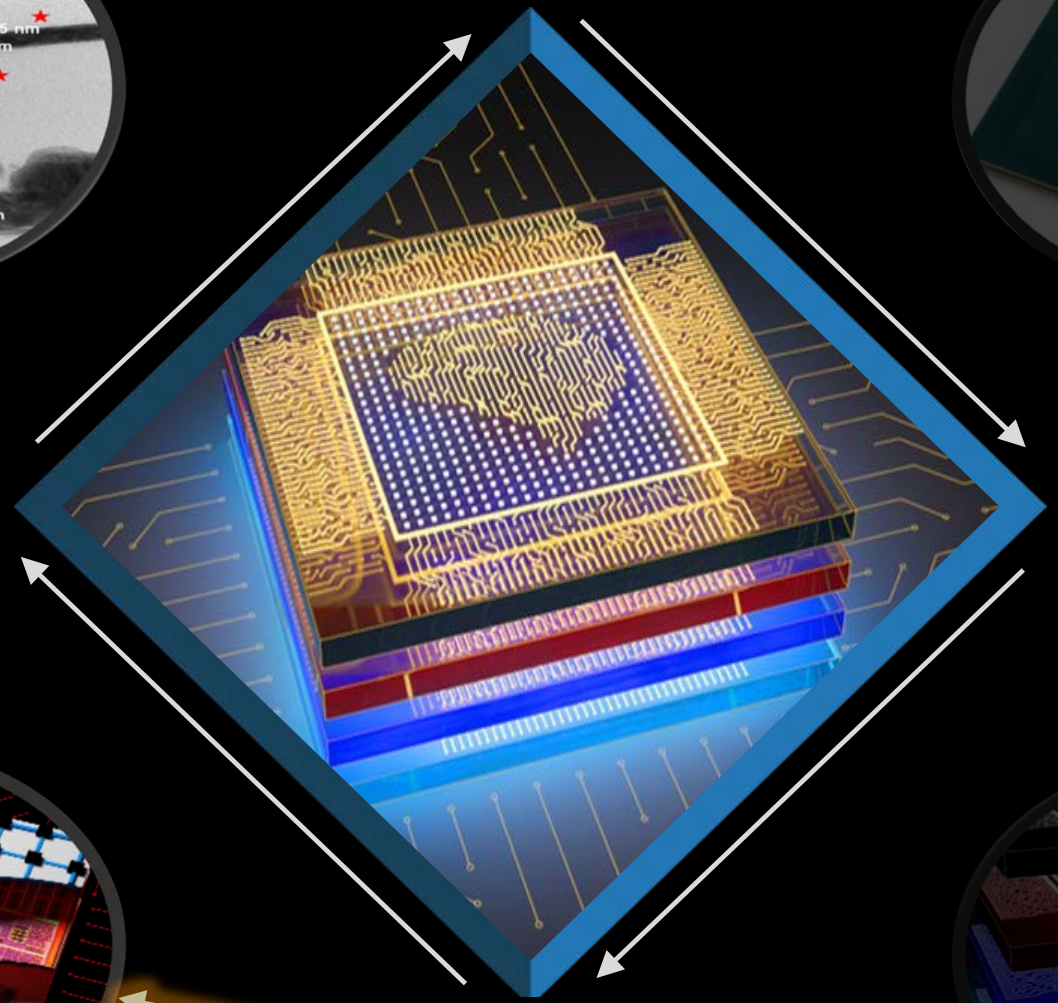


New Materials & Devices

Specialized Functions

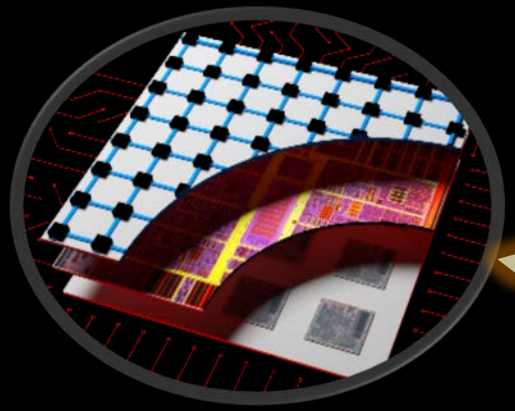


HIVE
L2M
N-ZERO
DSSoC
SDH
DRBE
RTML

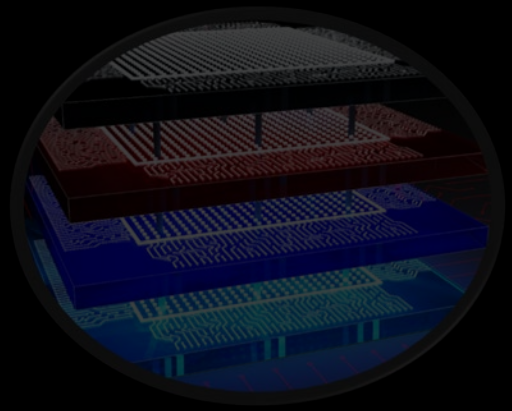


Design & Security

MIDAS
CHIPS
3DSoC
PIPES



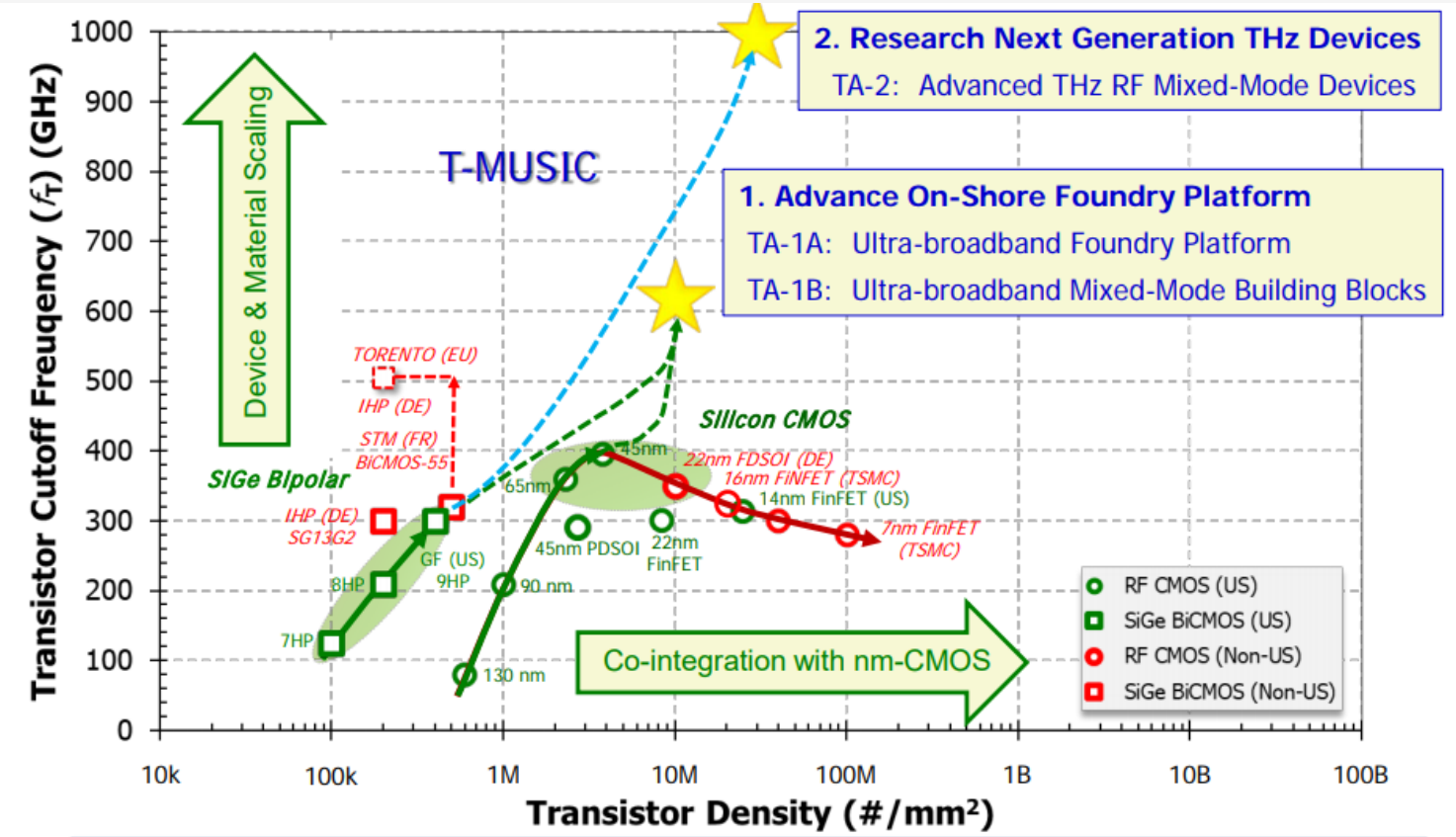
3D Heterogeneous Integration



CRAFT
SSITH
IDEA
POSH
AISS
GAPS

TECHNOLOGIES FOR MIXED-MODE ULTRA SCALED INTEGRATED CIRCUITS (T-MUSIC)

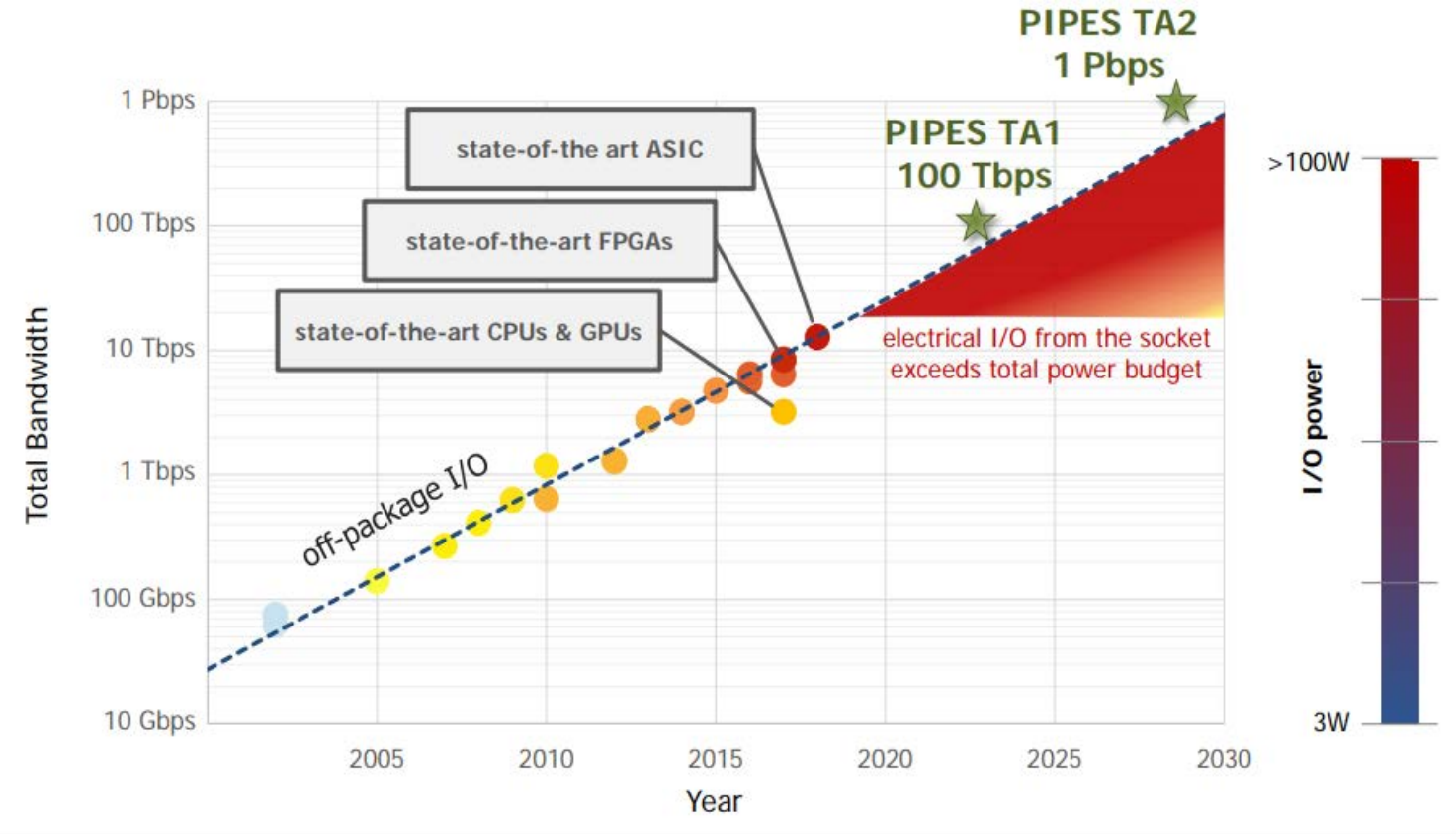
DR. YOUNG-KAI CHEN



- Develop on-shore wafer-scale ultra broadband mixed-mode technologies based on a digital CMOS foundry platform
- Develop next generation THz transistors beyond today's Moore's Law scaling
- Enable disruptive DoD systems with 10x improvement in the bandwidth, dynamic range and operational frequencies of RF analog electronics

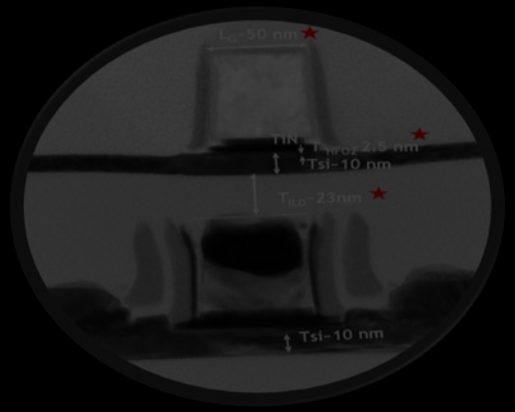
PHOTONICS IN THE PACKAGE FOR EXTREME SCALABILITY (PIPES)

DR. GORDON KEELER

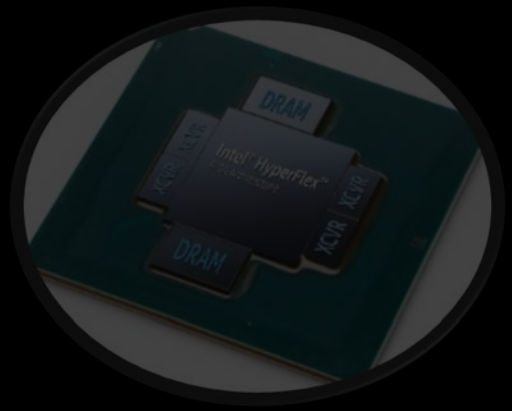


- Remove data locality as a design bottleneck, extending socket-level I/O performance system-wide
- Enable disruptive system scalability through embedded photonic I/O to increase bandwidth, reduce I/O power, and extend reach
- Establish a DoD-accessible ecosystem for photonically-enabled 2.5D microelectronics

JUMP
FRANC
T-MUSIC



Specialized Functions



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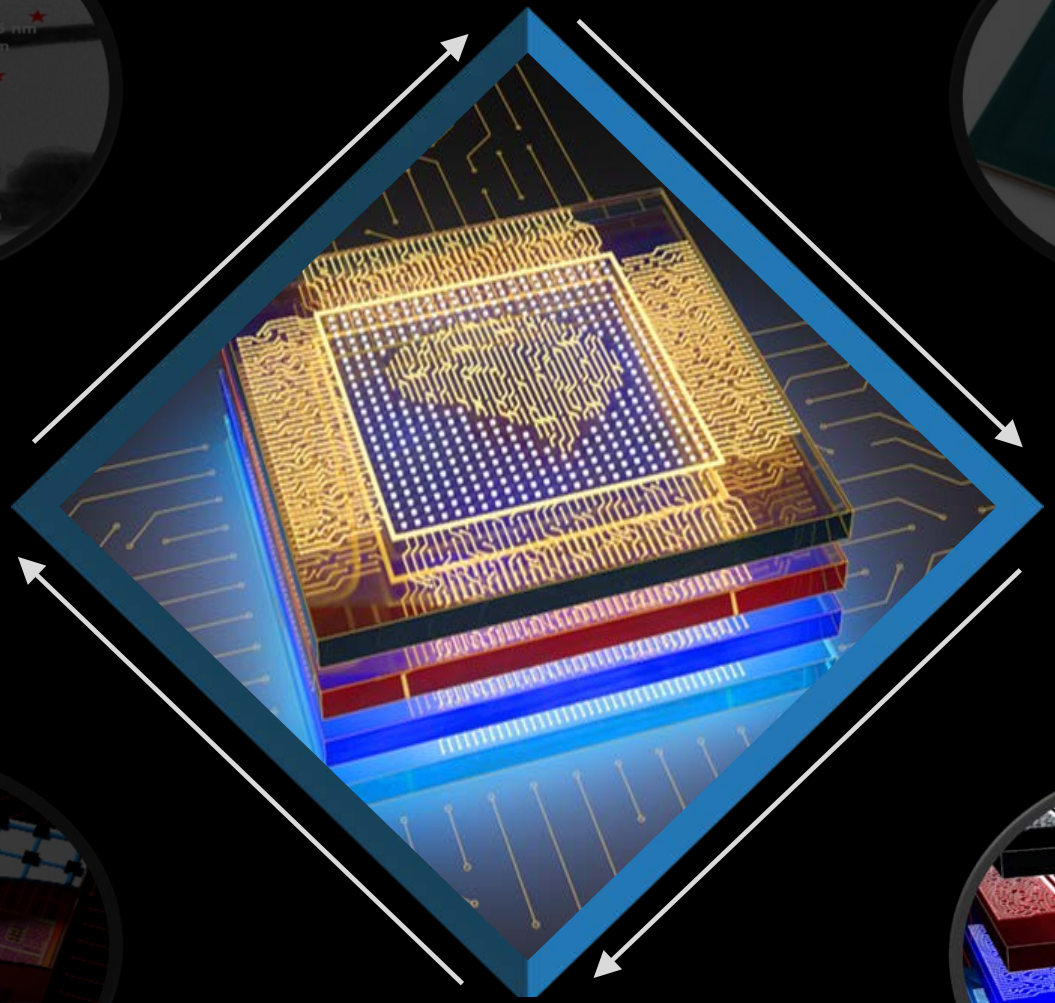
New Materials & Devices



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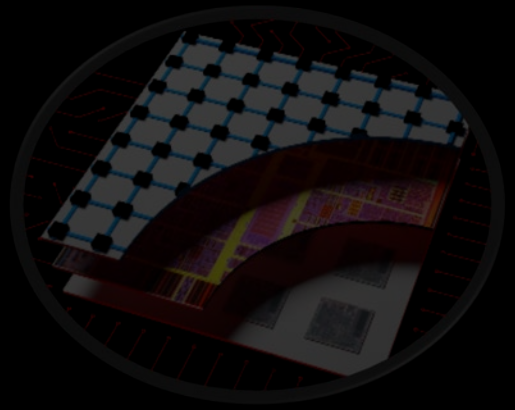

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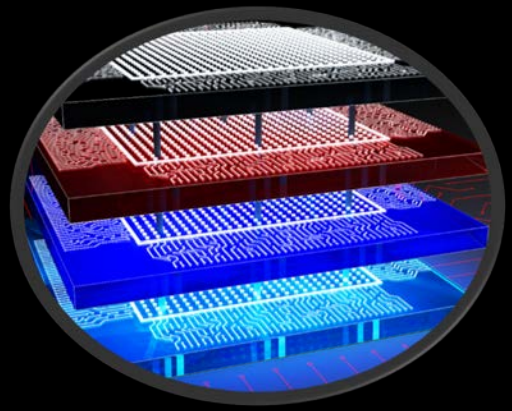

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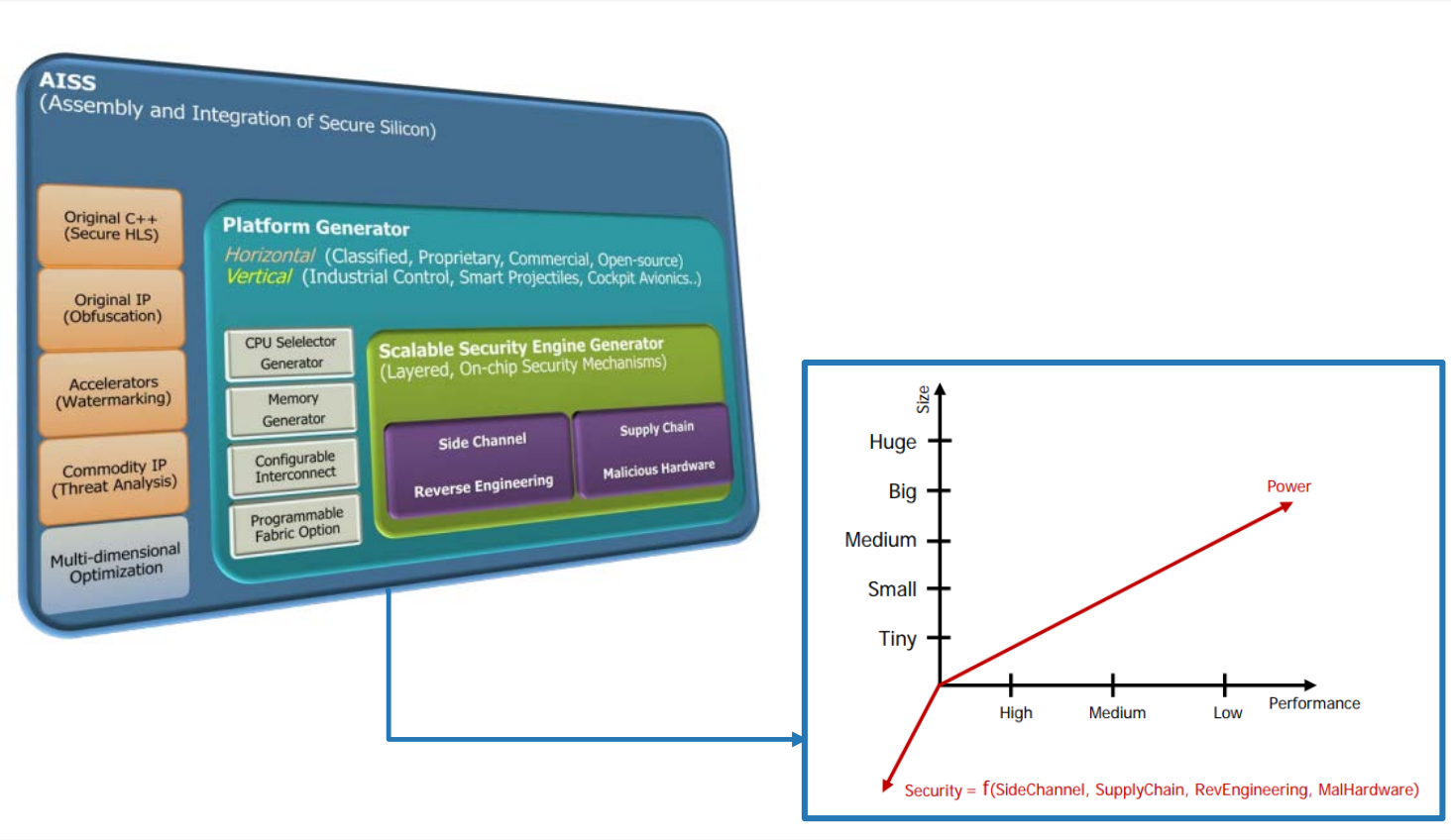
GAPS

AUTOMATIC IMPLEMENTATION OF SECURE SILICON (AISS)

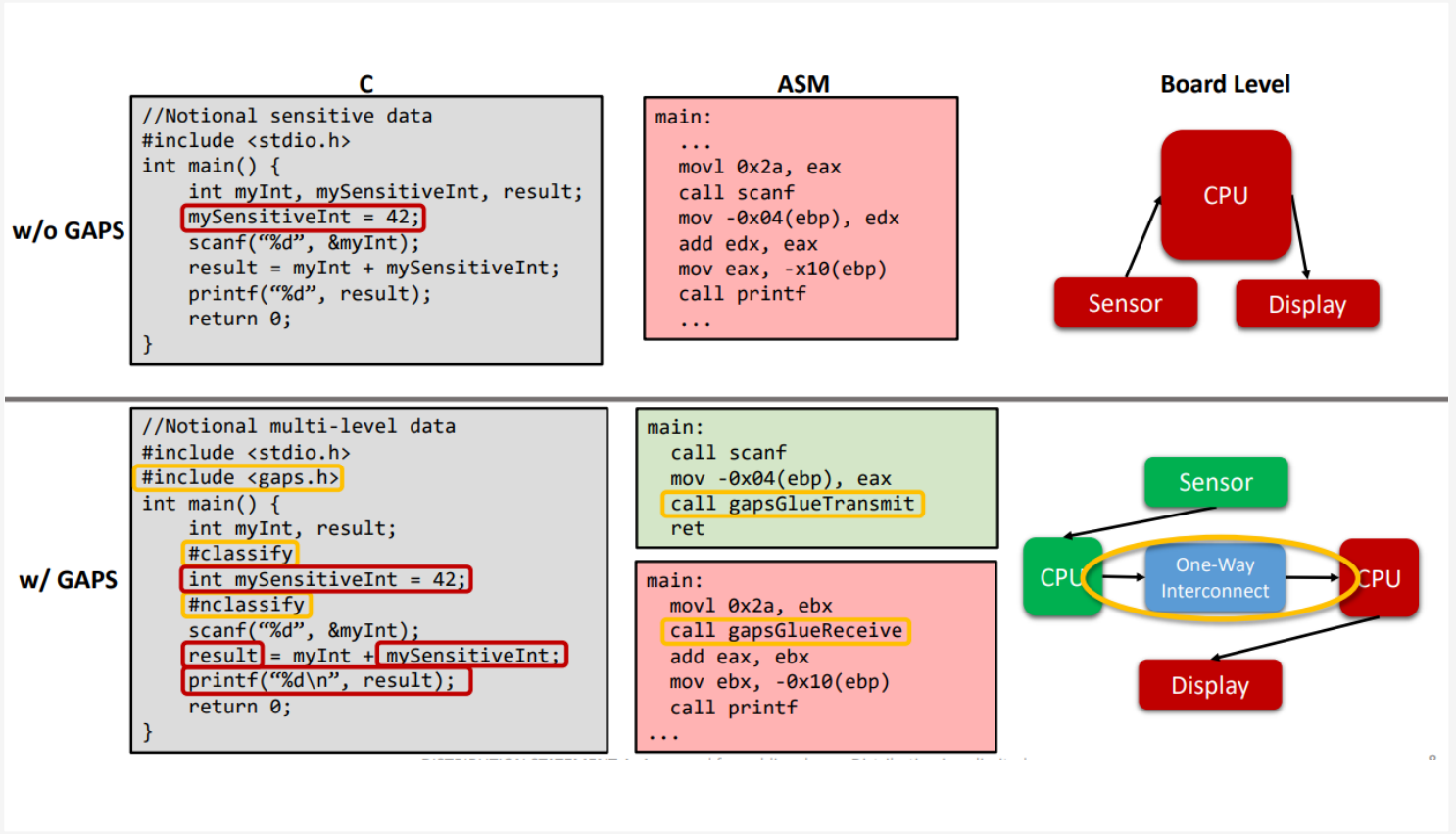
MR. SERGE LEEF



- Automate inclusion of scalable defense mechanisms into chip designs to enable security vs. economics optimization
- Enable semi-automated and automatic approaches to assembly and integration that can substantially improve design productivity

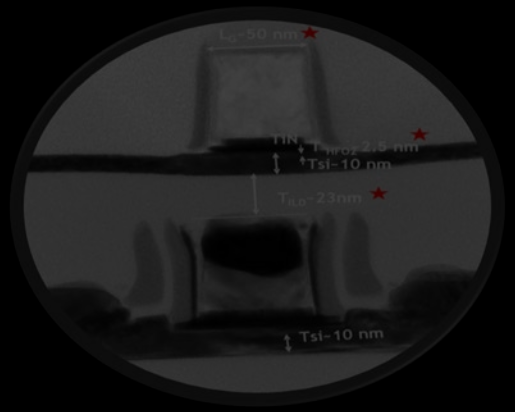
GUARANTEED ARCHITECTURES FOR PHYSICAL SECURITY (GAPS)

MR. WALTER WEISS



- Develop hardware and software architectures with provable security interfaces to physically isolate high risk transactions
- Enable physical seclusion for security and privacy in a digital age

JUMP
FRANC
T-MUSIC



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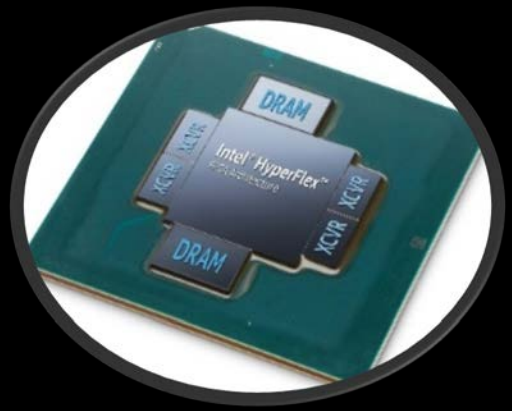

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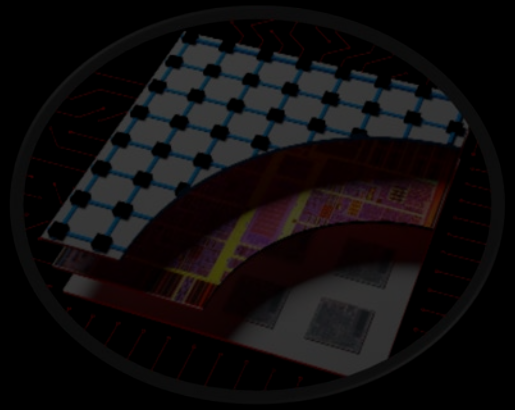
New Materials & Devices

Design & Security



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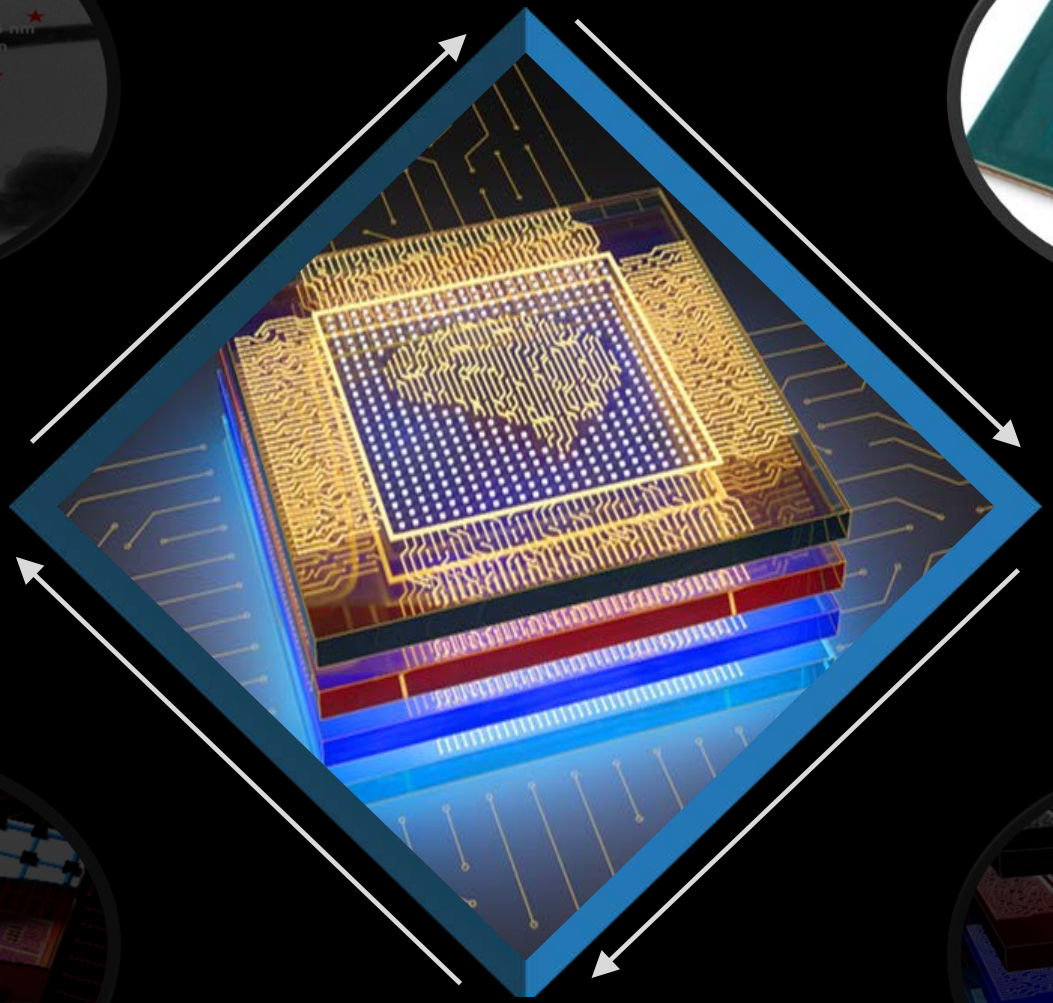

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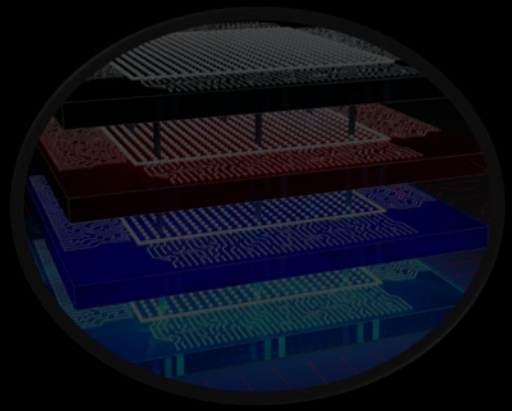

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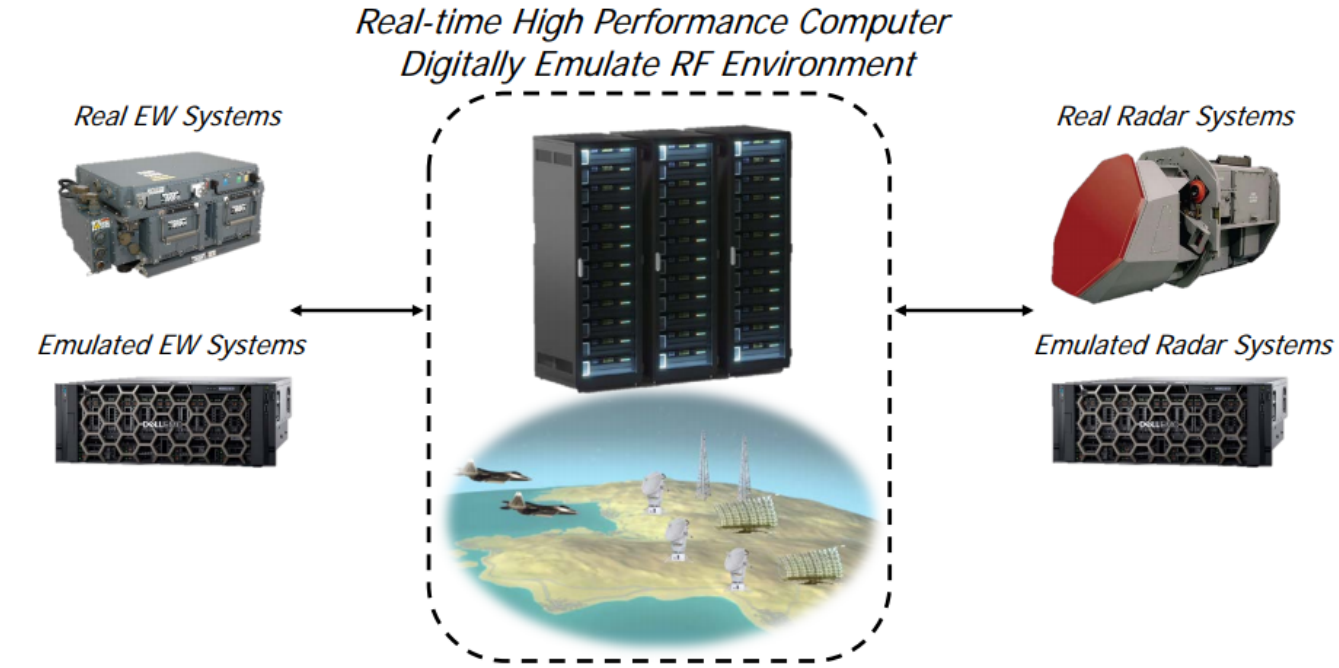
AISS
GAPS

DIGITAL RF BATTLESPACE EMULATOR (DRBE)

MR. PAUL TILGHMAN

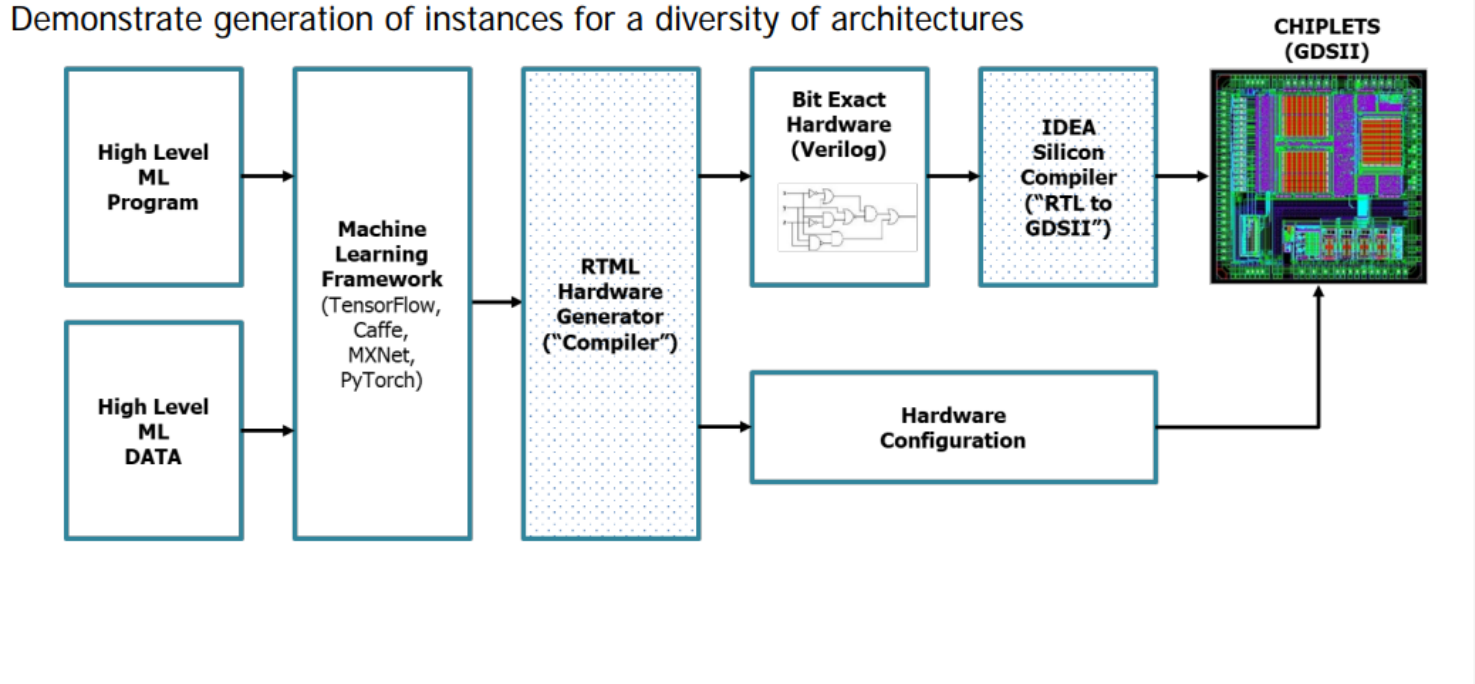


DRBE will allow real EW and radar systems to be interact in real-time on a completely virtual test range.

- Explore new and novel computing architectures, technologies, and methodologies necessary to achieve both low latency and high throughput computation
- Assemble an “array” of these novel computing devices into an HPC
- Integrate the HPC into a tool-suite and architecture which emulates the RF spectrum with high fidelity

REAL TIME MACHINE LEARNING (RTML)

MR. ANDREAS OLOFSSON



- Create no-human-in-the-loop hardware generators and compilers to enable fully automated creation of ML ASICs from high level source code
- Support diverse ML architectures including convolutional neural networks, recurrent networks spike time-dependent neural nets, unsupervised learning, etc.

JUMP
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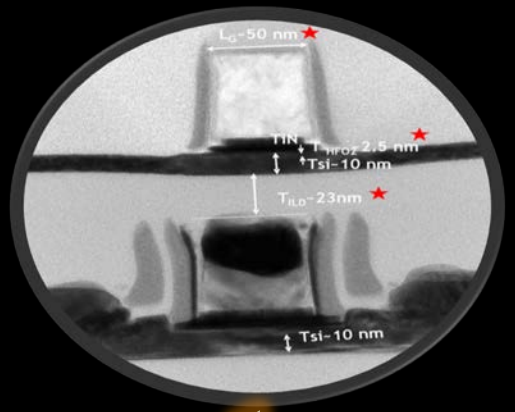

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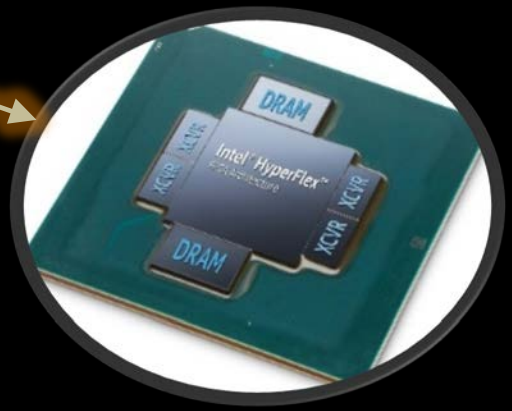

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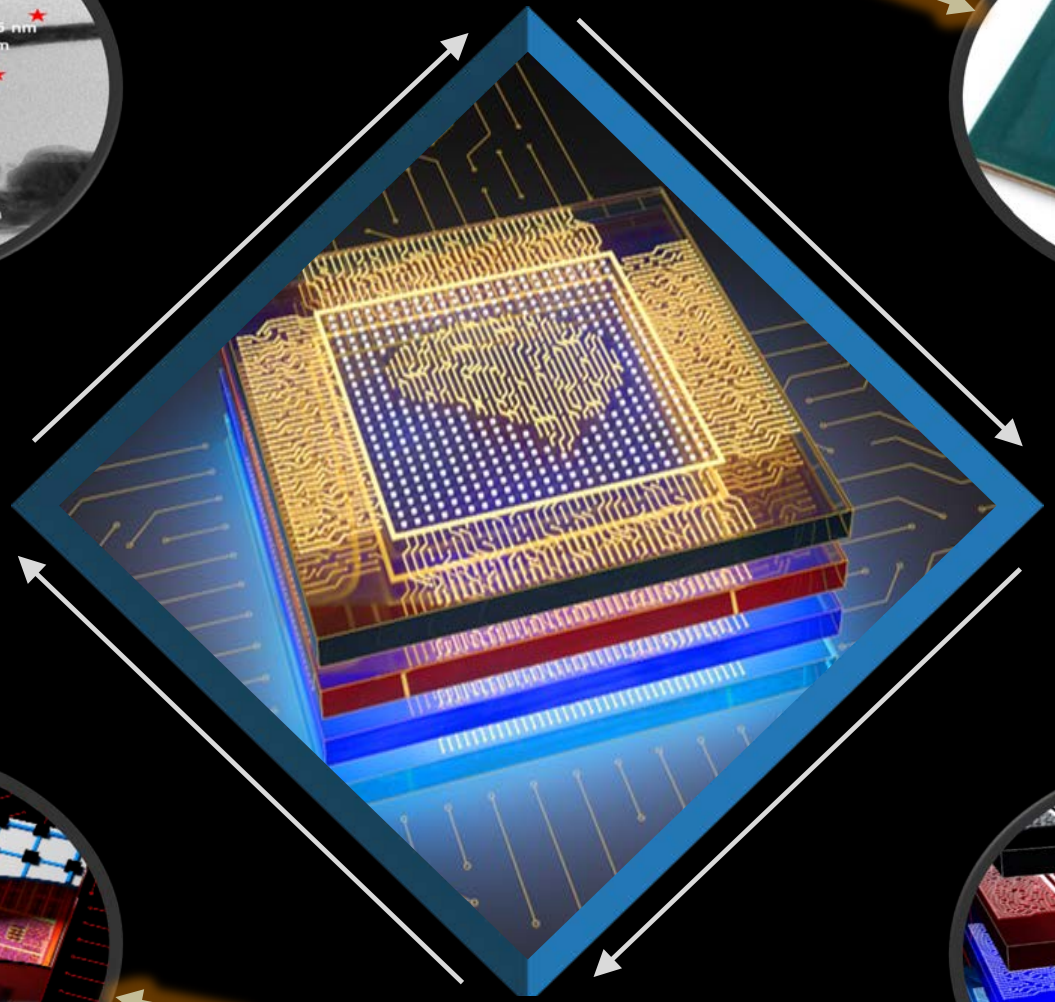

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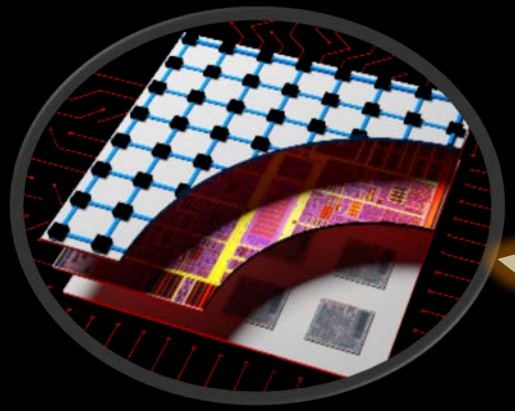

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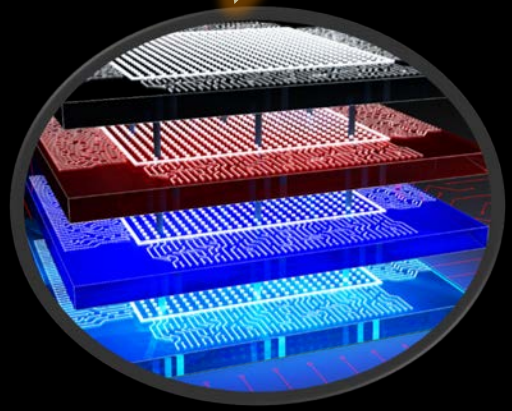

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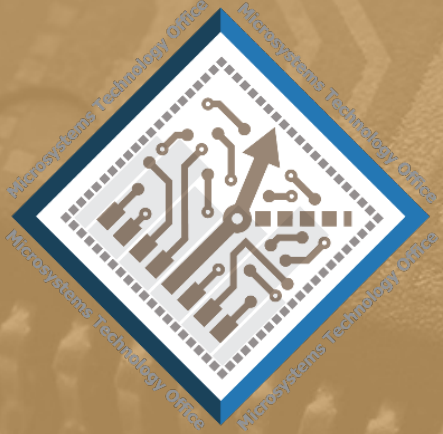

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