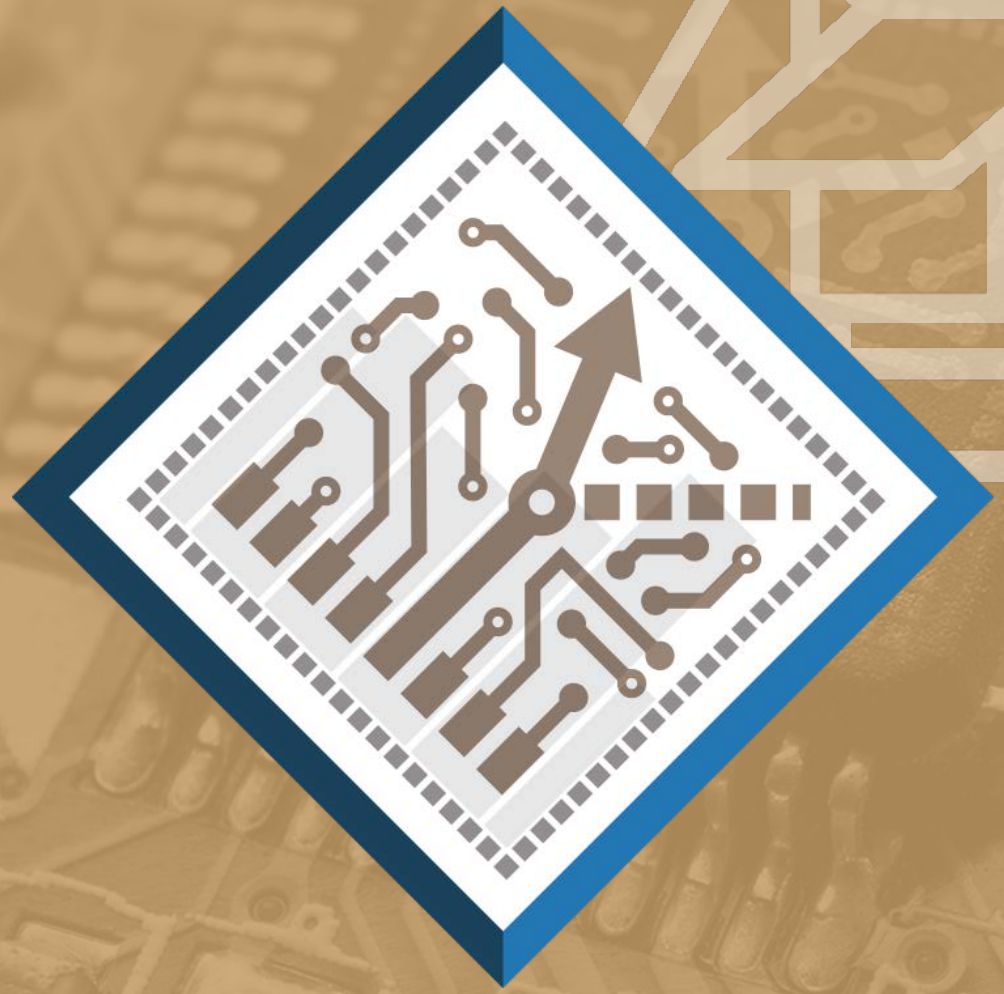
TOM RONDEAU

DARPA
PROGRAM MANAGER

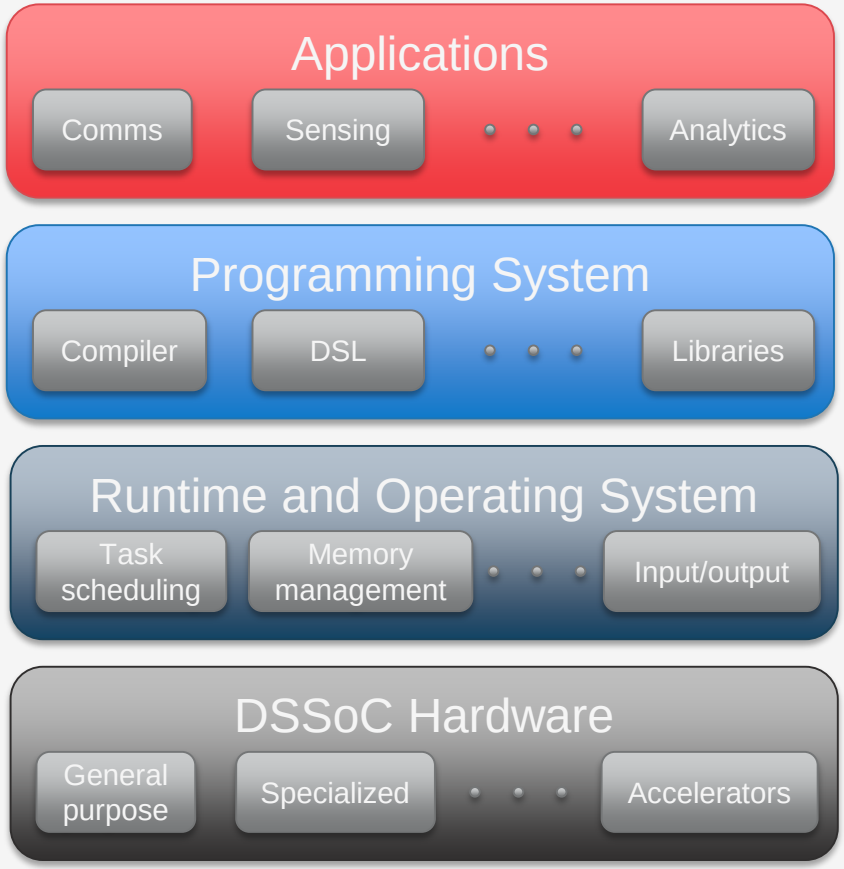


DOMAIN-SPECIFIC SYSTEM ON CHIP (DSSOC)

DSSOC

PROGRAM DESCRIPTION

- Enabling the era of specialization
  - through data-driven discovery of the domain space
  - to build specialized accelerators & math engines
  - that interconnect over a flexible, standard interface
  - with tools to support compiling and debugging
  - and execution of the right processing at the right time
- Programming efficiency *and* computational efficiency

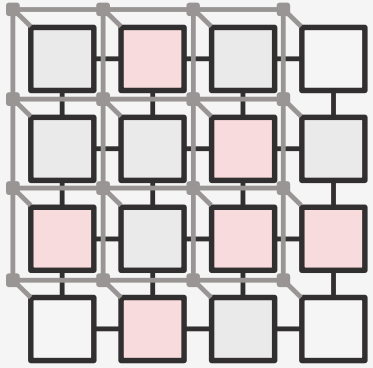


DSSOC

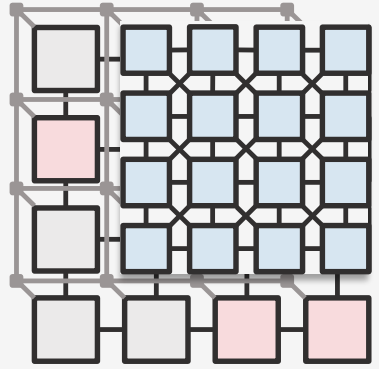
PROGRAM HIGHLIGHTS

- Went from rigid, static, and proprietary interfaces within an SoC to flexible, dynamic, and standardized
- These structures support fast iteration on:
  - Computational efficiency
  - Chip area
  - Communication overhead
  - Power efficiency
- Plus compilers that support heterogeneous targets and approximate computing

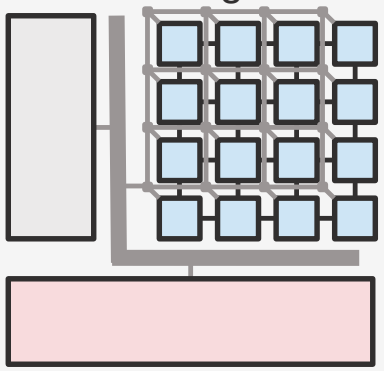
Design 1
Network on Chip



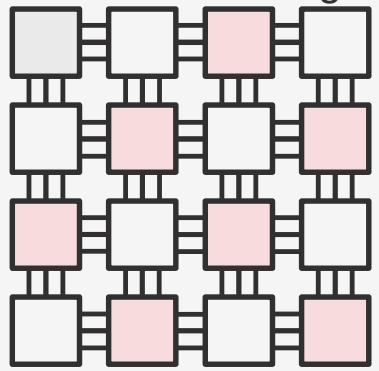
Design 2
Adaptive Processors



Design 3
Math Engines



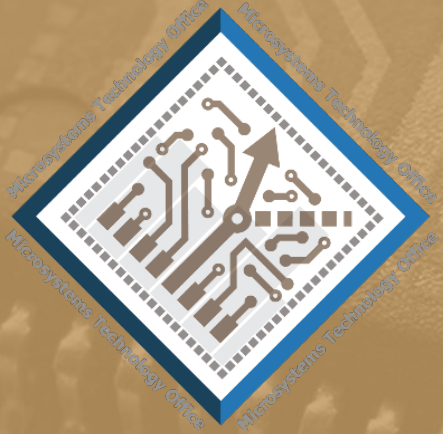
Design 4
Coarse Grain Reconfiguration



DSSOC

PERFORMERS

Arizona State University *PI: Daniel W. Bliss*	**Software Radio** for multifunction tactical communications and sensor systems
IBM T. J. Watson Research Center *PI: Pradip Bose*	**Computer Vision and Software Radio** for autonomous vehicles
Oak Ridge National Laboratory *PI: Jeffrey Vetter*	**Software Radio** for signal analysis and operating with and through electronic warfare
Raytheon Company *PI: Tom Kazior*	**Adaptive Beamforming** for large, software programmable arrays
Stanford University *PI: Mark Horowitz*	**Computer Vision** for improving embedded image and video processing applications



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